P33PCT825A/B
BUS INTERFACE REGISTER

ADVANCE INFORMATION

T-52-09

FEATURES

- 3.3V ±0.2V Power Supply
- Center Power and Ground Pins
- Full CMOS Implementation
- Low Ground Bounce
- Fully TTL Compatible Input and Output Levels
- High Speed Parallel Registers with positive edge-triggered D-type Flip-Flops
- Buffered Common Clock Enable ($\overline{EN}$) and Asynchronous Clear Input ($\overline{CLR}$)
- I_{OL} = 48mA (Commercial) and 32mA (Military)
- Clamp Diodes on all Inputs for Ringing Suppression
- Compact Pinout
  – 28-Pin 300 mil DIP, SOIC

DESCRIPTION

The P33PCT825 bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The P33PCT825 is a 8-bit buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. It is ideal for use as an output port requiring high I_{OL}/I_{OH}.

The P33PCT825 is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The P33PCT825 is manufactured with PACE III Technology™ which is Performance Advanced CMOS Engineered with two-level metal and epitaxial substrates to use 0.4 micron effective channel lengths giving 250 picosecond loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.0V to 3.3V, thus reducing output swings dramatically. This, together with the (lower inductance) center power and ground pins, and the extra power and extra ground pins, significantly reduces noise and ground bounce that would otherwise occur for very high speed circuitry.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 3.3V supply.

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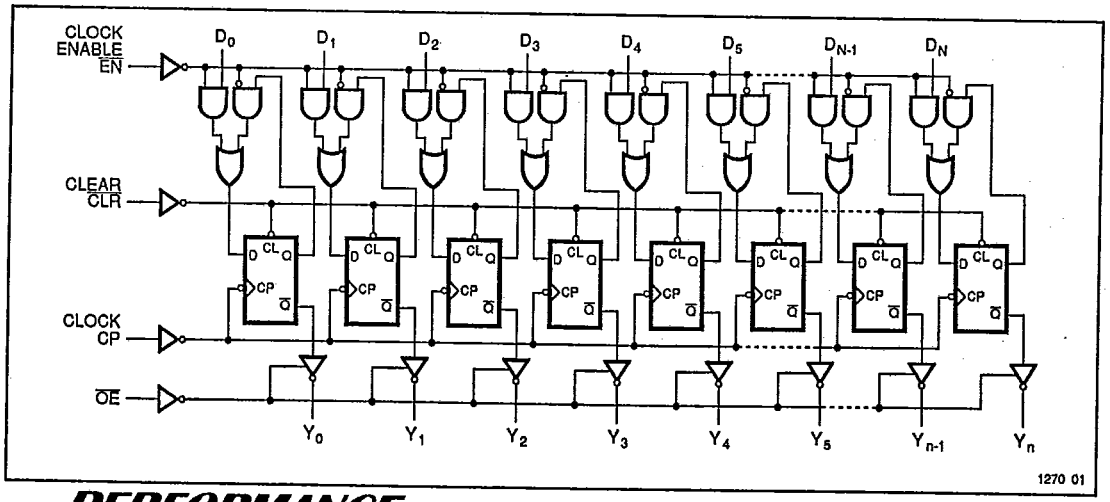
FUNCTIONAL BLOCK DIAGRAM



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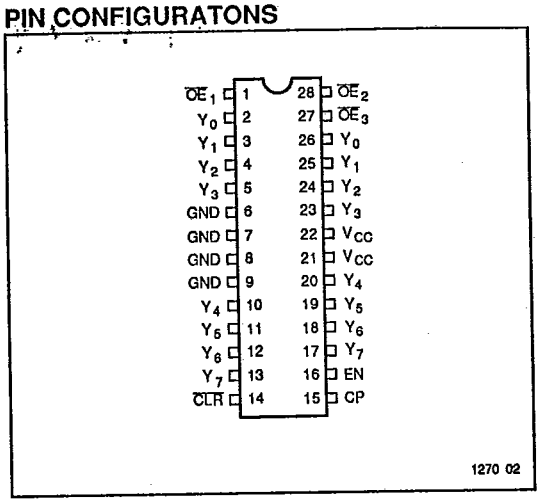
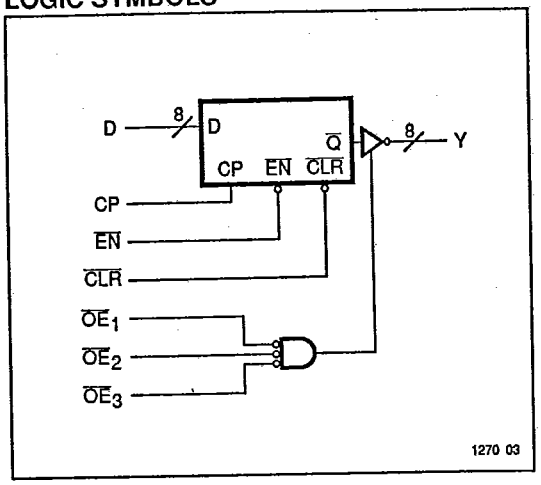
PIN CONFIGURATONS



LOGIC SYMBOLS



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