m i c r o e l e c t r o n i c s g r o u p

Lucent Technologies
Bell Labs Innovations

TLMA0110G 10 Gbits/s Limiting Amplifier

Features

- 8 mV typical input sensitivity, BER $\leq 10^{-10}$
- 32 dB gain, 38 dB differential
- Complementary 50 Ω I/Os
- Adjustable threshold control
- Single –5.2 V power supply
- 24-lead surface-mount package

Applications

- Data/clock main amplifier in SONET/SDH OC-192/ STM-64 transmission systems and DWDM systems
- Digital video transmission
- SONET/SDH test equipment

Functional Description

The Lucent Technologies Microelectronics Group TLMA0110G is a wideband limiting amplifier with differential inputs and outputs. It provides 32dB of gain (38 dB differential) and 9 GHz of bandwidth in a 50 Ω environment. The TLMA0110G consists of a 50 Ω input buffer followed by three gain stages and a 50 Ω output buffer. The threshold level can be adjusted by inserting an external voltage source into the amplifier's positive or negative feedback loops. At input levels below 20 mVp-p (single-ended), the device acts as a linear amplifier. For input levels from 20 mVp-p up to 800 mVp-p, the device operates in its limiting mode, providing a constant typical output of 550 mVp-p (single-ended).

The TLMA0110G is designed for use in SONET OC-192 and SDH STM-64 receiver/regenerator applications. Amplifier operation is from a single –5.2 V power supply. The TLMA0110G is available in a 24-lead, hermetic, surface-mount package.
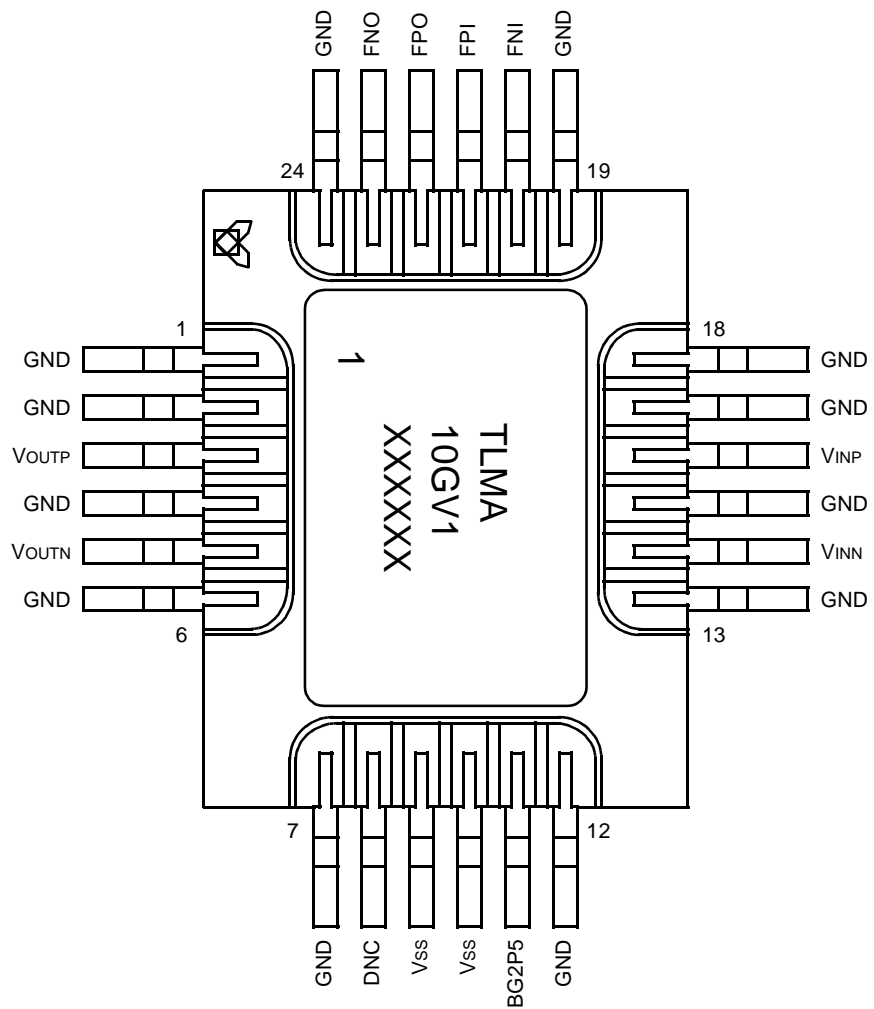
Functional Description (continued)
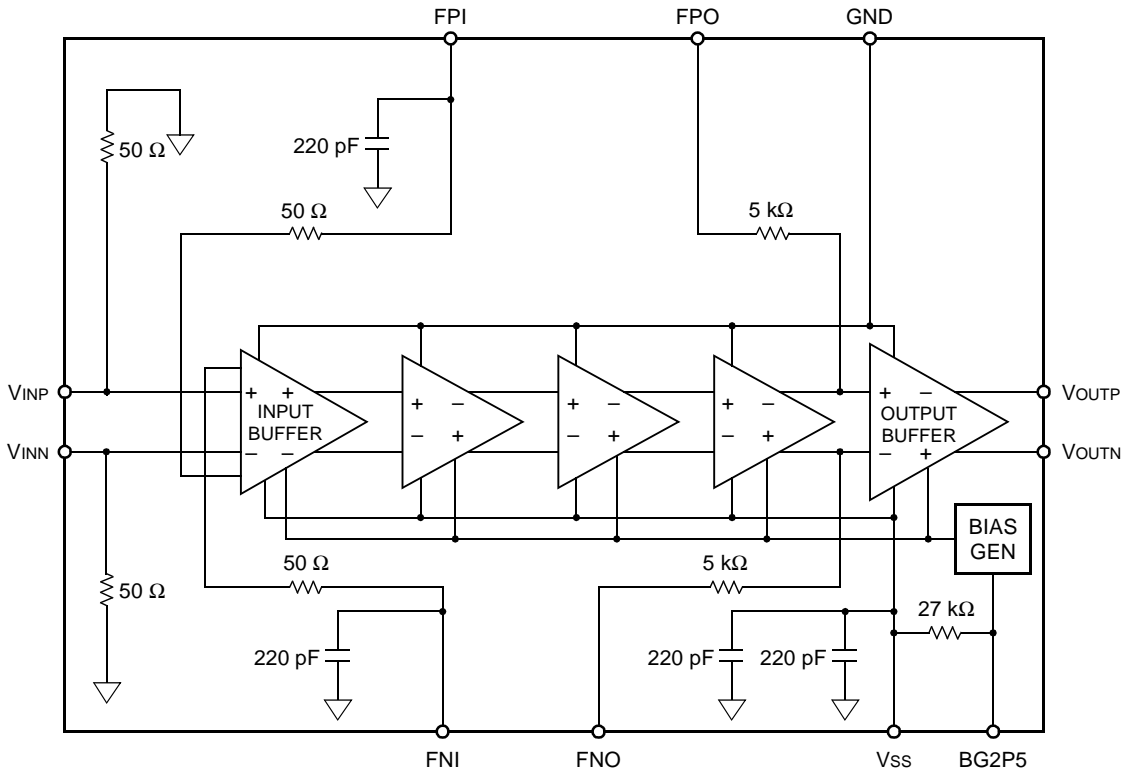
Figure 1. Block Diagram

5-8197(F).a

Pin Information

5-8198(F)r.5

Figure 2. Package Pinout (Top View)

Pin Information (continued)

Table 1. Pin Descriptions

Symbol	Pin	Description
GND	1, 2, 4, 6, 7, 12, 13, 15, 17, 18, 19, 24, Package Bottom	**Ground.** For optimal performance, the package bottom must be soldered to the ground plane.
V$_{OUTP}$	3	**Data Output.** ac couple for optimal performance.
V$_{OUTN}$	5	**Complementary Data Output.** ac couple for optimal performance.
DNC	8	**Do Not Connect.** Reserved for testing or future use.
V$_{SS}$	9, 10	**Power Supply Voltage.** –5.2 V dc nominal supply voltage.
BG2P5	11	**–2.5 V Bandgap Reference.** Connect to Si bandgap reference, such as *National Semiconductor*[*] part number LM4040.
V$_{INN}$	14	**Complementary Data Input.** (ac coupling required.)
V$_{INP}$	16	**Data Input.** (ac coupling required.)
FNI	20	**Feedback Negative Input.** Threshold level control.
FPI	21	**Feedback Positive Input.** Threshold level control.
FPO	22	**Feedback Positive Output.** Threshold level control.
FNO	23	**Feedback Negative Output.** Threshold level control.

* *National Semiconductor* is a registered trademark of National Semiconductor Corporation.

Nodes FPI, FPO, FNI, and FNO complete the positive and negative internal feedback loops that are used to control the threshold level. FPI should be shorted to FPO, and FNI should be shorted to FNO. This configuration will center the threshold level. The threshold level can be shifted by forcing a change in voltage on either side of the feedback loop using a voltage source.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

T_{CASE} = 25 °C unless otherwise specified.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{SS}	–7	0.5	V
Input Voltage	V_{IN}	GND	V_{SS}	V
Power Dissipation	P_D	—	1.0	W
Storage Temperature Range	T_{stg}	–40	125	°C
Case Temperature Range	T_{CASE}	0	100	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely accepted and, therefore, can be used for comparison purposes:

Device	Voltage
TLMA0110G	≥75 V

Operating Conditions

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{SS}	–4.75	–5.5	V
Operating Case Temperature Range	T_{CASE}	0	70	°C

Electrical Characteristics

Table 3. Limiting Amplifier Characteristics

T_{CASE} = 25 °C, V_{SS} = –5.2 V, and R_{LOAD} = 50 Ω. Inputs and outputs are ac-coupled and tested as shown in Figure 3. Bit rate = 9953.28 Mbits/s NRZ and data pattern = $2^{31} - 1$ PRBS, unless otherwise indicated. Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Sensitivity	S_{EN}	Single-ended, BER $\leq 10^{-10}$	—	8	—	mVp-p
Maximum Input Voltage	V_{IN}	Single-ended	—	—	800	mVp-p
		Differential	—	—	1600	mVp-p
Output Voltage	V_{OUT}	Single-ended, $V_{IN} \geq$ 30 mVp-p	400	550	700	mVp-p
Eye Crossing	—	30 mVp-p $\leq V_{IN}$ < 100 mVp-p	35	50	65	%
		100 mVp-p $\leq V_{IN}$ $\leq$ 800 mVp-p	40	50	60	%
Rise/Fall Time 20%—80%	t_R, t_F	V_{IN} = 100 mVp-p	—	20	35	ps
Jitter (rms)	—	V_{IN} = 100 mVp-p	—	2	3	ps
Small Signal Gain	G	Single-ended, P_{IN} = –35 dBm	—	32	—	dB
Small Signal Bandwidth	f_{3dB}	P_{IN} = –35 dBm	—	9	—	GHz
Input Return Loss	S_{11}	50 MHz—7.5 GHz	8	10	—	dB
Output Return Loss	S_{22}	50 MHz—7.5 GHz	8	10	—	dB
Supply Current	I_{SS}	V_{SS} = –5.2 V	—	145	170	mA

Note: Input return loss and output return loss are guaranteed by design or characterization and not production tested.
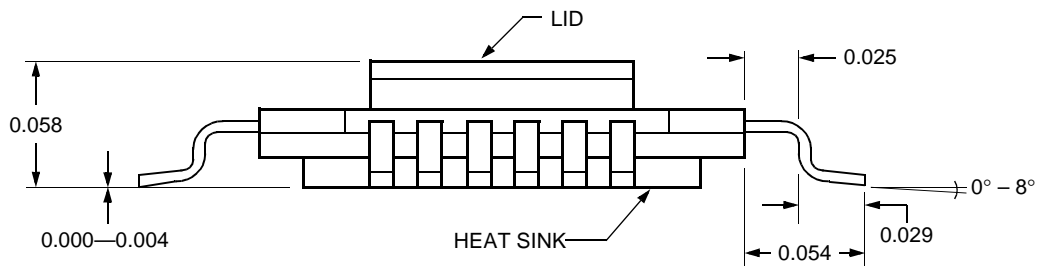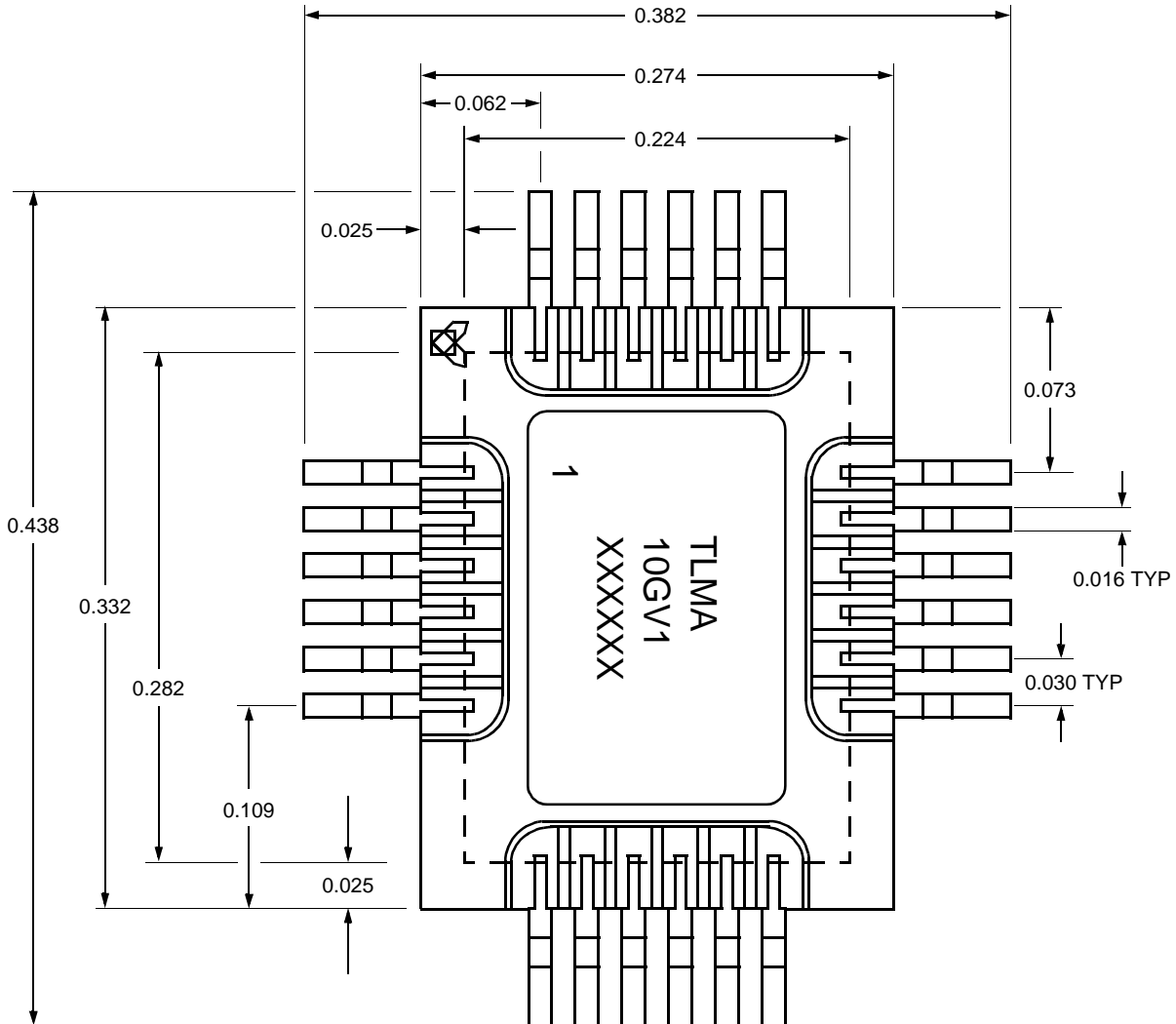
Test Circuit
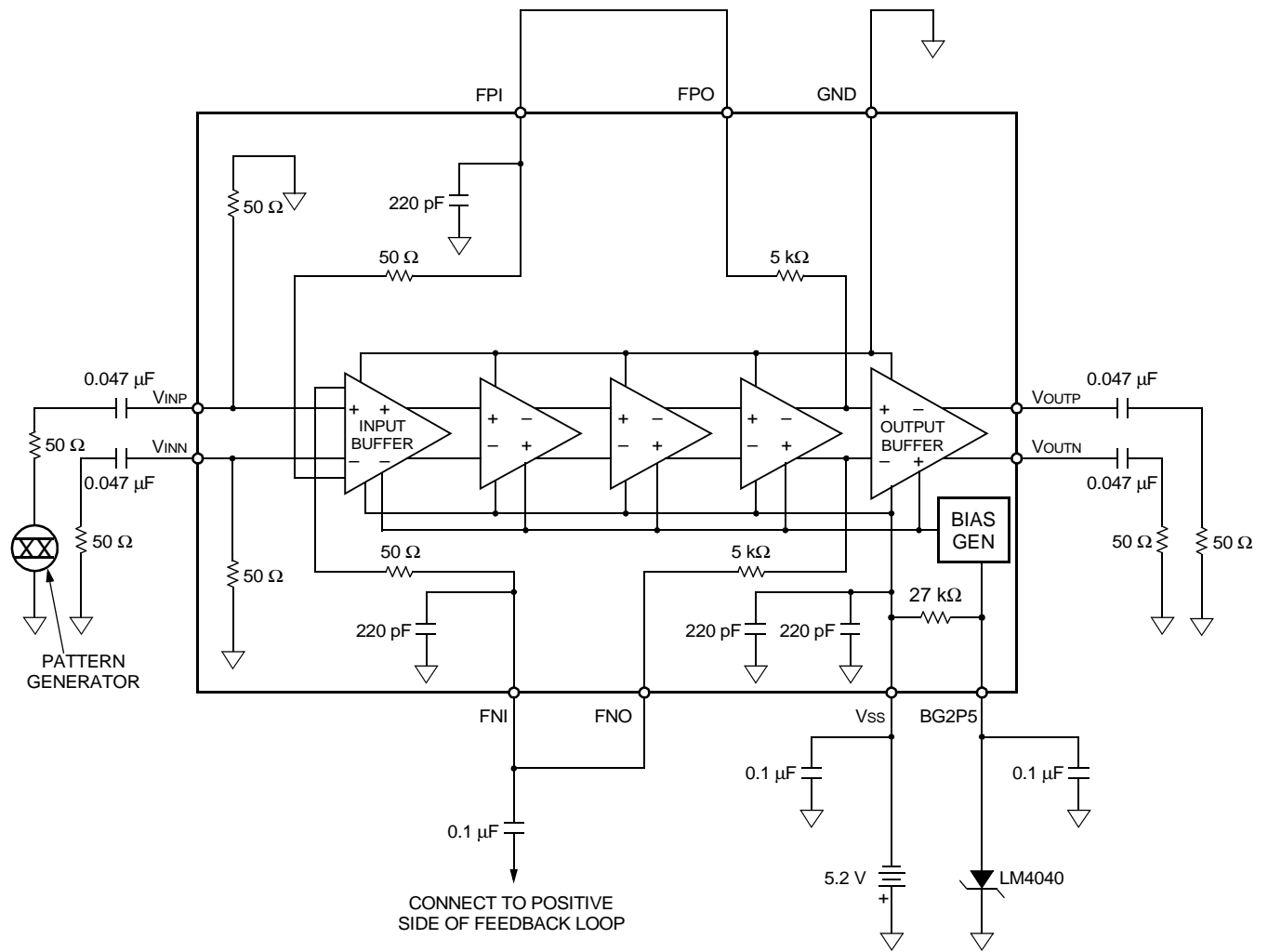
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Figure 3. Test Circuit

Outline Diagram

24-Pin, Surface-Mount Package (Top, Side Views)

Dimensions are in inches.

LID

HEAT SINK

5-8199(F).ar.2

Ordering Information

Device	Type	Comcode
TLMA0110G	24-Pin Package	108499369

m i c r o e l e c t r o n i c s   g r o u p

December 2000
DS00-182HSPL (Replaces DS99-312HSPL)

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