

**SRAM Memory Card 256KB through 8MB**

**General Description**

The WEDC SRAM Series (SRA) memory cards offer a high performance nonvolatile storage solution for code and data storage, disk caching, and write intensive mobile and embedded applications.

Packaged in PCMCIA type I or type II housing (type II for cards with extended battery backup time), the WEDC SRAM SRA series is based on 1 or 4Mbit SRAM memories, providing densities from 256 Kilobytes to 8 Megabytes.

The SRA series of SRAM memory cards requires a 5V power supply and operates at speeds to 150ns. The cards are based on advanced CMOS technology providing very low power and reliable data retention characteristics. WEDC's SRAM cards contain a rechargeable lithium battery and recharge circuitry, eliminating the need for replaceable batteries found in many SRAM cards.

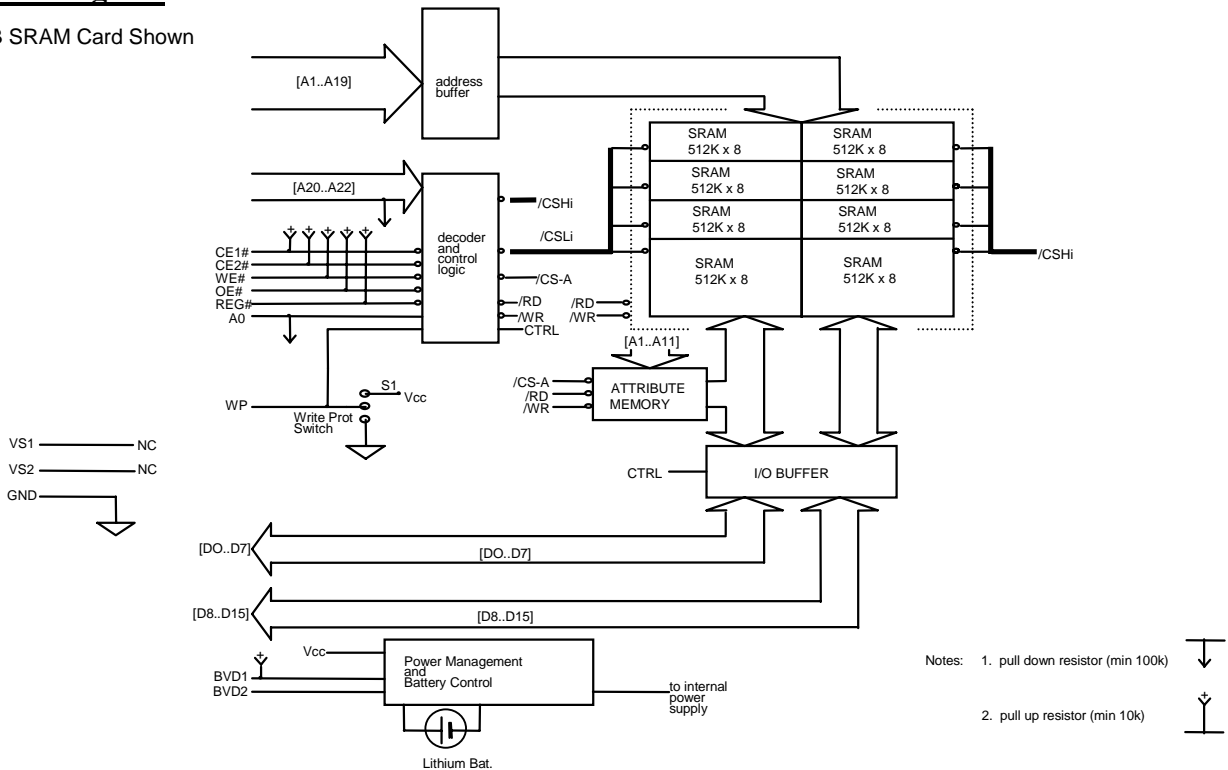
WEDC's standard cards are shipped with WEDC's SRAM Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

**Features**

- High Performance SRAM memory Card
- Single 5 Volt Supply
  - (3.3V/5V operation is available as an option)
- Fast Access times: 150ns
- x8/x16 PCMCIA standard interface
- Low Power CMOS technology provides very low power and reliable data retention characteristics
  - standby current < 100µA typical
- Rechargeable Lithium battery with recharge circuitry
  - eliminates the need for replaceable batteries
  - standby current during recharge typically < 2mA
  - battery backup time
    - 7 months - type I card
    - 18 months - type II card
 typical based on 4MB (lower densities will have greater storage times)
- Unlimited write cycles, no endurance issues
- Optional Features:
  - 2KB EEPROM attribute memory containing CIS
  - Optional Hardware Write Protect switch
- PC Card Standard Type I or Type II Form Factor

**Block Diagram**

4MB SRAM Card Shown





**Pinout**

| Pin | Signal name | I/O | Function       | Active |
|-----|-------------|-----|----------------|--------|
| 1   | GND         |     | Ground         |        |
| 2   | DQ3         | I/O | Data bit 3     |        |
| 3   | DQ4         | I/O | Data bit 4     |        |
| 4   | DQ5         | I/O | Data bit 5     |        |
| 5   | DQ6         | I/O | Data bit 6     |        |
| 6   | DQ7         | I/O | Data bit 7     |        |
| 7   | CE1#        | I   | Card enable 1  | LOW    |
| 8   | A10         | I   | Address bit 10 |        |
| 9   | OE#         | I   | Output enable  | LOW    |
| 10  | A11         | I   | Address bit 11 |        |
| 11  | A9          | I   | Address bit 9  |        |
| 12  | A8          | I   | Address bit 8  |        |
| 13  | A13         | I   | Address bit 13 |        |
| 14  | A14         | I   | Address bit 14 |        |
| 15  | WE#         | I   | Write Enable   | LOW    |
| 16  | RDY/BSY#    | O   | Ready/Busy     | N.C.   |
| 17  | Vcc         |     | Supply Voltage |        |
| 18  | Vpp1        |     | Prog. Voltage  | N.C.   |
| 19  | A16         | I   | Address bit 16 |        |
| 20  | A15         | I   | Address bit 15 |        |
| 21  | A12         | I   | Address bit 12 |        |
| 22  | A7          | I   | Address bit 7  |        |
| 23  | A6          | I   | Address bit 6  |        |
| 24  | A5          | I   | Address bit 5  |        |
| 25  | A4          | I   | Address bit 4  |        |
| 26  | A3          | I   | Address bit 3  |        |
| 27  | A2          | I   | Address bit 2  |        |
| 28  | A1          | I   | Address bit 1  |        |
| 29  | A0          | I   | Address bit 0  |        |
| 30  | DQ0         | I/O | Data bit 0     |        |
| 31  | DQ1         | I/O | Data bit 1     |        |
| 32  | DQ2         | I/O | Data bit 2     |        |
| 33  | WP          | O   | Write Potect   | HIGH   |
| 34  | GND         |     | Ground         |        |

| Pin | Signal name | I/O | Function            | Active   |
|-----|-------------|-----|---------------------|----------|
| 35  | GND         |     | Ground              |          |
| 36  | CD1#        | O   | Card Detect 1       | LOW      |
| 37  | DQ11        | I/O | Data bit 11         |          |
| 38  | DQ12        | I/O | Data bit 12         |          |
| 39  | DQ13        | I/O | Data bit 13         |          |
| 40  | DQ14        | I/O | Data bit 14         |          |
| 41  | DQ15        | I   | Data bit 15         |          |
| 42  | CE2#        | I   | Card Enable 2       | LOW      |
| 43  | VS1         | O   | Voltage Sense 1     | N.C.     |
| 44  | N.C.        |     |                     |          |
| 45  | N.C.        |     |                     |          |
| 46  | A17         | I   | Address bit 17      | 256KB(2) |
| 47  | A18         | I   | Address bit 18      | 512KB(2) |
| 48  | A19         | I   | Address bit 19      | 1MB(2)   |
| 49  | A20         | I   | Address bit 20      | 2MB(2)   |
| 50  | A21         | I   | Address bit 21      | 4MB(2)   |
| 51  | Vcc         |     | Supply Voltage      |          |
| 52  | Vpp2        |     | Prog. Voltage       | N.C.     |
| 53  | A22         |     | Address bit 22      | 8MB(2,4) |
| 54  | A23         |     | N.C.                |          |
| 55  | A24         |     | N.C.                |          |
| 56  | A25         |     | N.C.                |          |
| 57  | VS2         | O   | Voltage Sense 2     | N.C.     |
| 58  | N.C.        |     |                     |          |
| 59  | Wait#       | O   | Extended Bus Cycle  | Low      |
| 60  | N.C.        |     |                     |          |
| 61  | REG#        | I   | Attrib Mem Select   | Low      |
| 62  | BVD2        | O   | Bat. Volt. Detect 2 |          |
| 63  | BVD1        | O   | Bat. Volt. Detect 1 | (3)      |
| 64  | DQ8         | I/O | Data bit 8          |          |
| 65  | DQ9         | I/O | Data bit 9          |          |
| 66  | DQ10        | O   | Data bit 10         |          |
| 67  | CD2#        | O   | Card Detect 2       | LOW      |
| 68  | GND         |     | Ground              |          |

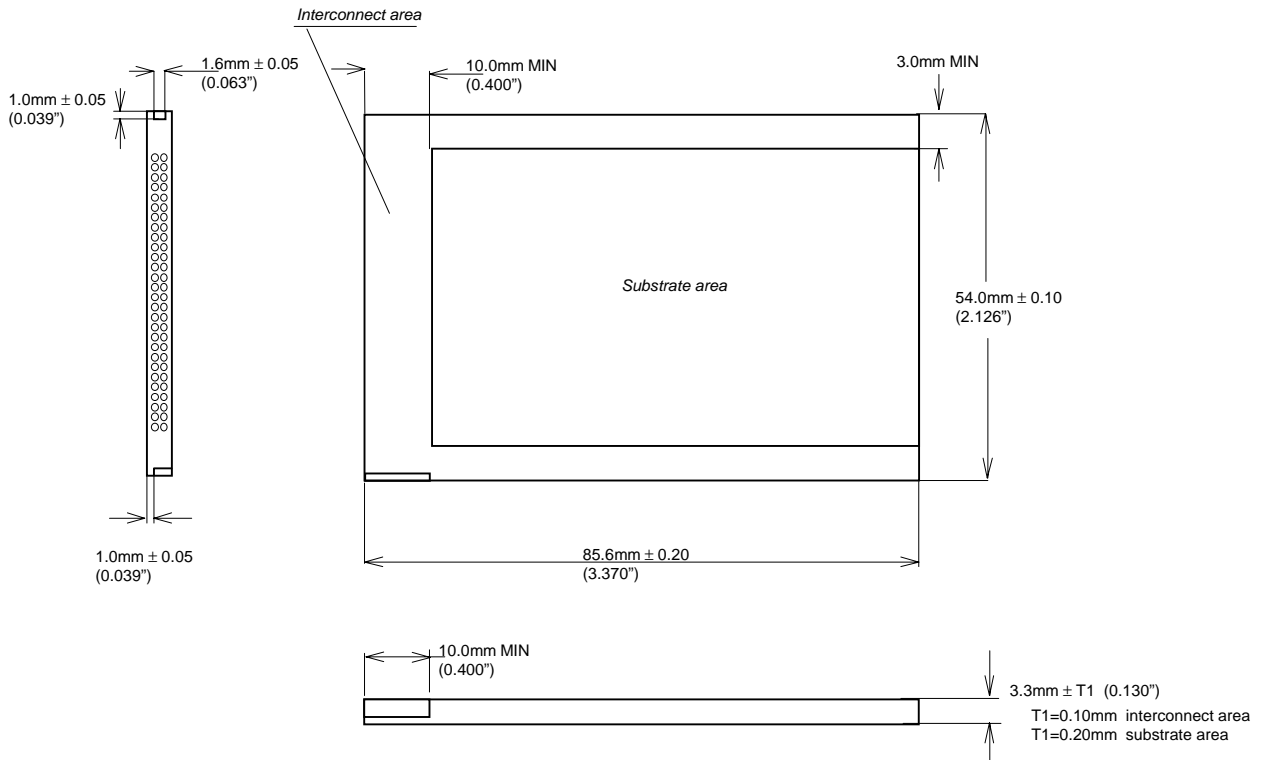
**Notes:**

1. CD1# and CD2# are grounded internal to PC Card.
2. Shows density for which specified address bit is MSB. Higher order address bits are no connects (i.e., 1MB A19 is MSB, A20 - A21 are NC).
3. BVD1 is an open drain output with a 10K ohm internal pull-up resistor.
4. Address bit 22 is used for the 8MB cards as well as the 6MB Cards.

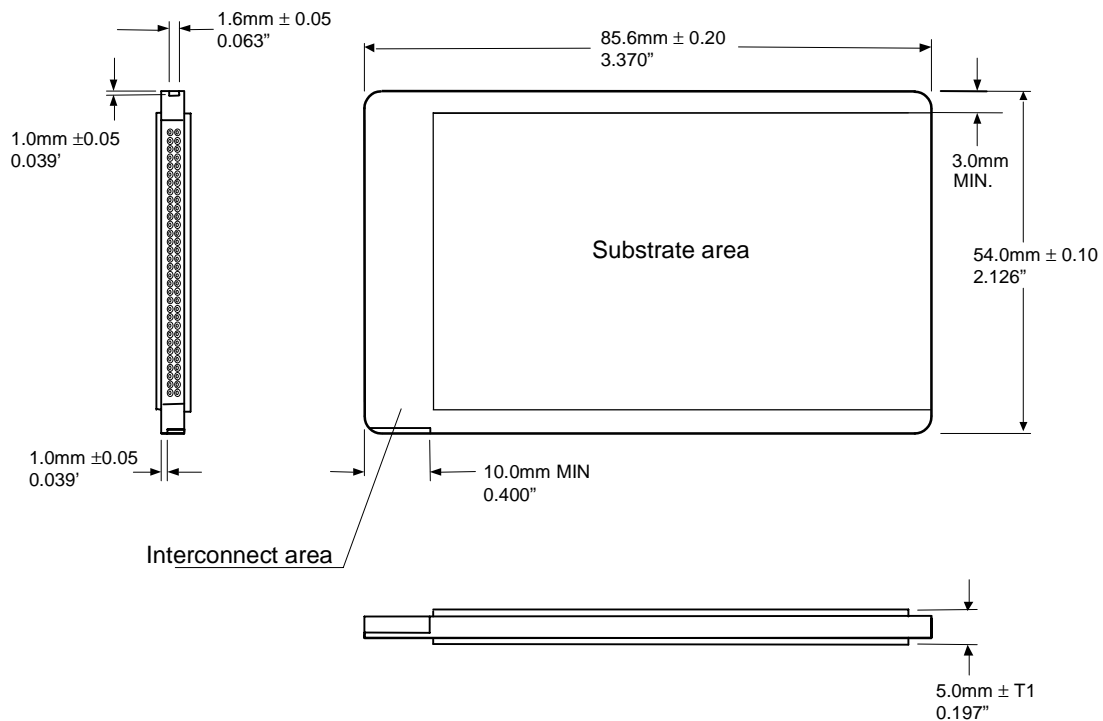


**Mechanical**

**Type I**



**Type II**





**Card Signal Description**

| Symbol     | Type         | Name and Function   |
|------------|--------------|---|
| A0 - A25   | INPUT        | <b>ADDRESS INPUTS:</b> A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit. (address pins used are based on card density, see pinout for highest used address pin)                      |
| DQ0 - DQ15 | INPUT/OUTPUT | <b>DATA INPUT/OUTPUT:</b> DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ0 - DQ7 constitute the lower (even) byte and DQ8 - DQ15 the upper (odd) byte. DQ15 is the MSB.  |
| CE1#, CE2# | INPUT        | <b>CARD ENABLE 1 AND 2:</b> CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.   |
| OE#        | INPUT        | <b>OUTPUT ENABLE:</b> Active low signal enabling read data from the memory card.  |
| WE#        | INPUT        | <b>WRITE ENABLE:</b> Active low signal gating write data to the memory card.  |
| RDY/BSY#   | OUTPUT       | <b>READY/BUSY OUTPUT:</b> Not used for SRAM cards   |
| CD1#, CD2# | OUTPUT       | <b>CARD DETECT 1 and 2:</b> Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.   |
| WP         | OUTPUT       | <b>WRITE PROTECT:</b> Follows hardware Write Protect Switch. When Switch is placed in on position, signal is pulled high (10K ohm). When switch is off signal is pulled low.  |
| VPP1, VPP2 | N.C.         | <b>PROGRAM/ERASE POWER SUPPLY:</b> Not used for SRAM cards.   |
| VCC        |              | <b>CARD POWER SUPPLY:</b> 5.0V for all internal circuitry.  |
| GND        |              | <b>GROUND:</b> for all internal circuitry.  |
| REG#       | INPUT        | <b>ATTRIBUTE MEMORY SELECT :</b> only used with cards built with optional attribute memory.   |
| RST        | INPUT        | <b>RESET:</b> Not used for SRAM cards   |
| WAIT#      | OUTPUT       | <b>WAIT:</b> This signal is pulled high internally for compatibility. No wait states are generated.   |
| BVD1, BVD2 | OUTPUT       | <b>BATTERY VOLTAGE DETECT:</b> Provides status of Battery voltage.<br>BVD2 = Voh (battery voltage is guaranteed to retain data)<br>BVD2 = Vol, BVD1 = Voh (data is valid, battery recharge required)<br>BVD2 = BVD1 = Vol (data may no longer be valid, battery requires extended recharge) |
| VS1, VS2   | OUTPUT       | <b>VOLTAGE SENSE:</b> Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V, 16 bit card has been inserted.  |
| RFU        |              | <b>RESERVED FOR FUTURE USE</b>  |
| N.C.       |              | <b>NO INTERNAL CONNECTION TO CARD:</b> pin may be driven or left floating   |

**FUNCTIONAL TRUTH TABLE**

| <i>READ function</i>  |      |      |    |     |     | <i>Common Memory</i> |          |           | <i>Attribute Memory</i> |           |           |
|-----------------------|------|------|----|-----|-----|----------------------|----------|-----------|-------------------------|-----------|-----------|
| Function Mode         | /CE2 | /CE1 | A0 | /OE | /WE | /REG                 | D15-D8   | D7-D0     | /REG                    | D15-D8    | D7-D0     |
| Standby Mode          | H    | H    | X  | X   | X   | X                    | High-Z   | High-Z    | X                       | High-Z    | High-Z    |
| Byte Access (8 bits)  | H    | L    | L  | L   | H   | H                    | High-Z   | Even-Byte | L                       | High-Z    | Even-Byte |
|                       | H    | L    | H  | L   | H   | H                    | High-Z   | Odd-Byte  | L                       | High-Z    | Not Valid |
| Word Access (16 bits) | L    | L    | X  | L   | H   | H                    | Odd-Byte | Even-Byte | L                       | Not Valid | Even-Byte |
| Odd-Byte Only Access  | L    | H    | X  | L   | H   | H                    | Odd-Byte | High-Z    | L                       | Not Valid | High-Z    |
| <i>WRITE function</i> |      |      |    |     |     |                      |          |           |                         |           |           |
| Standby Mode          | H    | H    | X  | X   | X   | X                    | X        | X         | X                       | X         | X         |
| Byte Access (8 bits)  | H    | L    | L  | H   | L   | H                    | X        | Even-Byte | L                       | X         | Even-Byte |
|                       | H    | L    | H  | H   | L   | H                    | X        | Odd-Byte  | L                       | X         | X         |
| Word Access (16 bits) | L    | L    | X  | H   | L   | H                    | Odd-Byte | Even-Byte | L                       | X         | Even-Byte |
| Odd-Byte Only Access  | L    | H    | X  | H   | L   | H                    | Odd-Byte | X         | L                       | X         | X         |



**Absolute Maximum Ratings** <sup>(2)</sup>

|                                    |                       |
|------------------------------------|-----------------------|
| Operating Temperature TA (ambient) |                       |
| Commercial                         | 0°C to +60 °C         |
| Industrial                         | -40°C to +85 °C       |
| Storage Temperature                |                       |
| Commercial                         | 0°C to +60 °C         |
| Industrial                         | -40°C to +85 °C       |
| Voltage on any pin relative to VSS | -0.5V to VCC+0.5V (1) |
| VCC supply Voltage relative to VSS | -0.5V to +7.0V        |

**Notes:**

(1) During transitions, inputs may undershoot to -2.0V or overshoot to VCC +2.0V for periods less than 20ns.

(2) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Characteristics** <sup>(1)</sup>

CMOS Test Conditions: VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

| Sym  | Parameter              | Density    | Notes | Min       | Typ <sup>(3)</sup> | Max      | Units | Test Conditions                      |
|------|------------------------|------------|-------|-----------|--------------------|----------|-------|--------------------------------------|
| ICC  | VCC Active Current     | 64KB       | 1     |           | 90                 | 180      | mA    | VCC = 5.25V<br>tcycle = 150ns        |
|      |                        | 128KB      |       | 90        | 180                |          |       |                                      |
|      |                        | 256KB      |       | 90        | 180                |          |       |                                      |
|      |                        | 512KB      |       | 90        | 180                |          |       |                                      |
|      |                        | 1MB to 8MB |       | 110       | 190                |          |       |                                      |
| ICCS | VCC Standby Current    | All        | 2,4   | < 0.1     | < 1                | 10       | mA    | VCC = 5.25V<br>Control Signals = VCC |
| ILI  | Input Leakage Current  | All        | 5,6   |           |                    | ±20      | µA    | VCC = VCCMAX<br>Vin = VCC or VSS     |
| ILO  | Output Leakage Current | All        | 6     |           |                    | ±20      | µA    | VCC = VCCMAX<br>Vout = VCC or VSS    |
| VIL  | Input Low Voltage      | All        | 6     | 0         |                    | 0.8      | V     |                                      |
| VIH  | Input High Voltage     | All        | 6     | 3.85      |                    | VCC +0.5 | V     |                                      |
| VOL  | Output Low Voltage     | All        | 6     |           |                    | 0.4      | V     | IOL = 3.2mA                          |
| VOH  | Output High Voltage    | All        | 6     | VCC - 0.4 |                    | VCC      | V     | IOH = -2.0mA                         |

**Notes:**

- All currents are for x16 mode and are RMS values unless otherwise specified.
- Control Signals: CE<sub>1</sub>#, CE<sub>2</sub>#, OE#, WE#, REG#.
- Typical: VCC = 5V, T = +25C.
- ICCS includes battery recharge current. Value depends on battery discharge level. ICCS min is specified for fully charged battery. ICCS typical value is specified for battery discharge to 2.7V. ICCS max is specified for a fully discharged battery (0V). Battery will recharge to 1.5V in 20 sec.
- Values are the same for byte and word wide modes for all card densities.
- Exceptions: Leakage currents on CE<sub>1</sub>#, CE<sub>2</sub>#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors.

**Battery Characteristics**

| Parameter           | Density    | Notes | SRA11-14 |        | SRA01-04 |                  | Units   | Conditions              |
|---------------------|------------|-------|----------|--------|----------|------------------|---|-------------------------|
|                     |            |       | Type I   | Type I | Type II  |                  |   |                         |
| Battery Life        | All        | (1)   | min 10   |        | min 10   |                  | years   | Normal operation, T=25C |
| Battery Backup Time | 256KB      | (2)   | -        | 24     | 60       | months (typical) | T=25C<br>Battery backup time is a calculated value and is not guaranteed. This should not be used to schedule battery recharging. |                         |
|                     | 512KB, 1MB |       | 32       | 18     | 45       |                  |   |                         |
|                     | 2MB        |       | 22       | 12     | 30       |                  |   |                         |
|                     | 4MB        |       | 12       | 7      | 17       |                  |   |                         |
|                     | 6MB        |       | 12       | 7      | 17       |                  |   |                         |
|                     | 8MB        |       | -        | -      | 12       |                  |   |                         |

**Notes:**

- Battery Life refers to functional lifetime of battery.
- Battery backup time is density and temperature dependent.



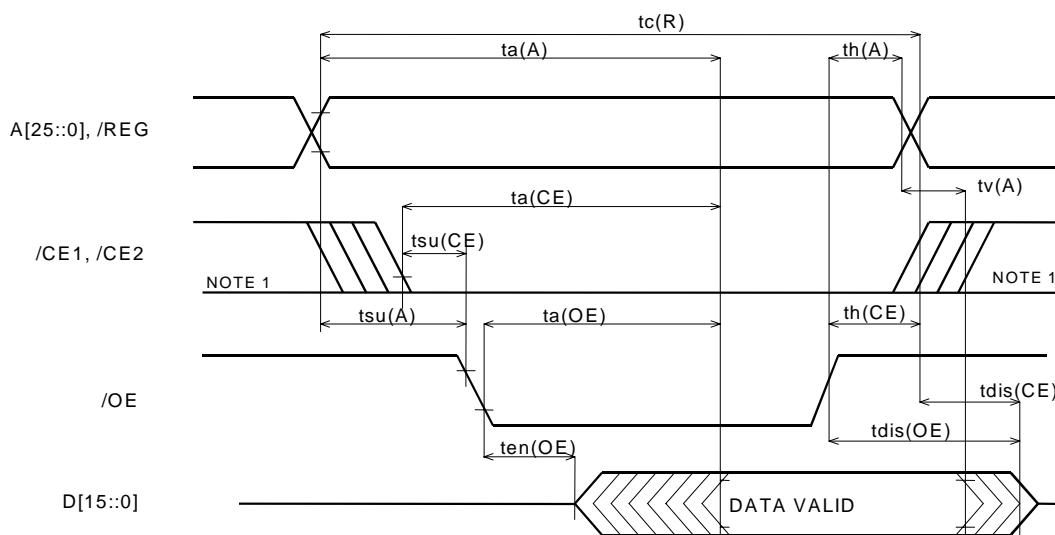
**AC Characteristics**

Read Timing Parameters

| SYM<br>(PCMCIA) | Parameter                       | 150ns |     | Unit |
|-----------------|---------------------------------|-------|-----|------|
|                 |                                 | Min   | Max |      |
| $t_{RC}$        | Read Cycle Time                 | 150   |     | ns   |
| $t_a(A)$        | Address Access Time             |       | 150 | ns   |
| $t_a(CE)$       | Card Enable Access Time         |       | 150 | ns   |
| $t_a(OE)$       | Output Enable Access Time       |       | 75  | ns   |
| $t_{su}(A)$     | Address Setup Time              | 20    |     | ns   |
| $t_{su}(CE)$    | Card Enable Setup Time          | 0     |     | ns   |
| $t_h(A)$        | Address Hold Time               | 20    |     | ns   |
| $t_h(CE)$       | Card Enable Hold Time           | 20    |     | ns   |
| $t_v(A)$        | Output Hold from Address Change | 0     |     | ns   |
| $t_{dis}(CE)$   | Output Disable Time from CE#    |       | 75  | ns   |
| $t_{dis}(OE)$   | Output Disable Time from OE#    |       | 75  | ns   |
| $t_{dis}(CE)$   | Output Enable Time from CE#     | 5     |     | ns   |
| $t_{dis}(OE)$   | Output Enable Time from OE#     | 5     |     | ns   |

**Note:** AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram



**Note:** Signal may be high or low in this area.

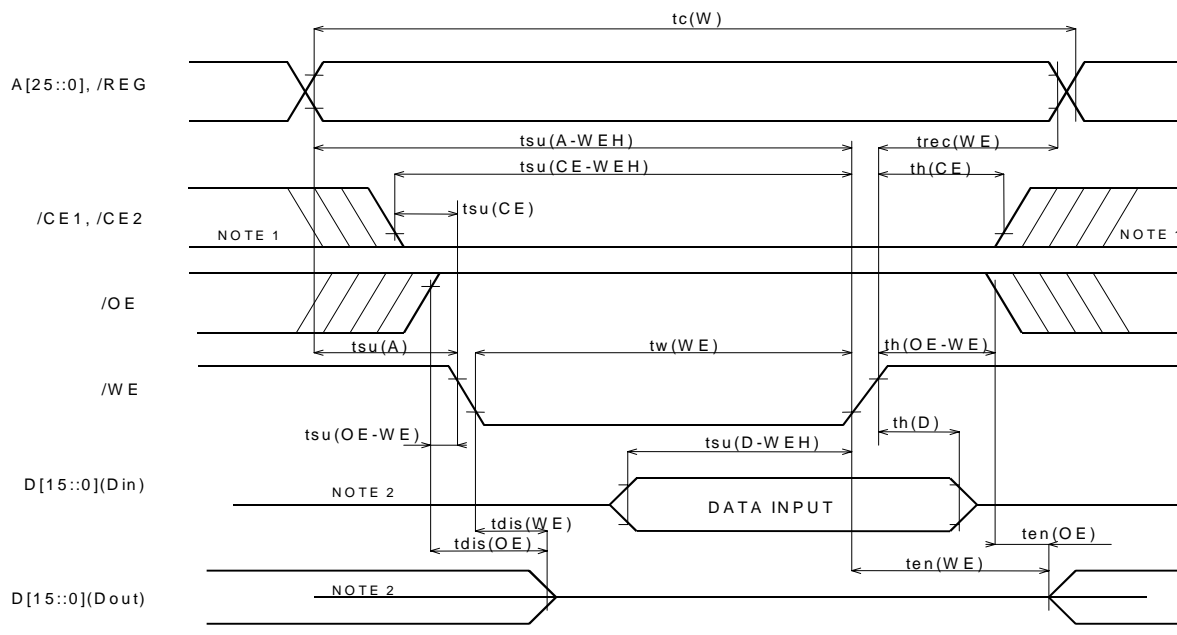


Write Timing Parameters

|                  |                                 | 150ns |     |      |
|------------------|---------------------------------|-------|-----|------|
| SYM (PCMCIA)     | Parameter                       | Min   | Max | Unit |
| $t_{cW}$         | Write Cycle Time                | 150   |     | ns   |
| $t_w(WE)$        | Write Pulse Width               | 80    |     | ns   |
| $t_{su}(A)$      | Address Setup Time              | 20    |     | ns   |
| $t_{su}(A-WEH)$  | Address Setup Time for WE#      | 100   |     | ns   |
| $t_{su}(CE-WEH)$ | Card Enable Setup Time for WE#  | 100   |     | ns   |
| $t_{su}(D-WEH)$  | Data Setup Time for WE#         | 50    |     | ns   |
| $t_h(D)$         | Data Hold Time                  | 20    |     | ns   |
| $t_{rec}(WE)$    | Write Recover Time              | 20    |     | ns   |
| $t_{dis}(WE)$    | Output Disable Time from WE#    |       | 75  | ns   |
| $t_{dis}(OE)$    | Output Disable Time from OE#    |       | 75  | ns   |
| $t_{en}(WE)$     | Output Enable Time from WE#     | 5     |     | ns   |
| $t_{dis}(OE)$    | Output Enable Time from OE#     | 5     |     | ns   |
| $t_{su}(OE-WE)$  | Output Enable Setup from WE#    | 10    |     | ns   |
| $t_h(OE-WE)$     | Output Enable Hold from WE#     | 10    |     | ns   |
| $t_{su}(CE)$     | Card Enable Setup Time from OE# | 0     |     | ns   |
| $t_h(CE)$        | Card Enable Hold Time           | 20    |     | ns   |

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



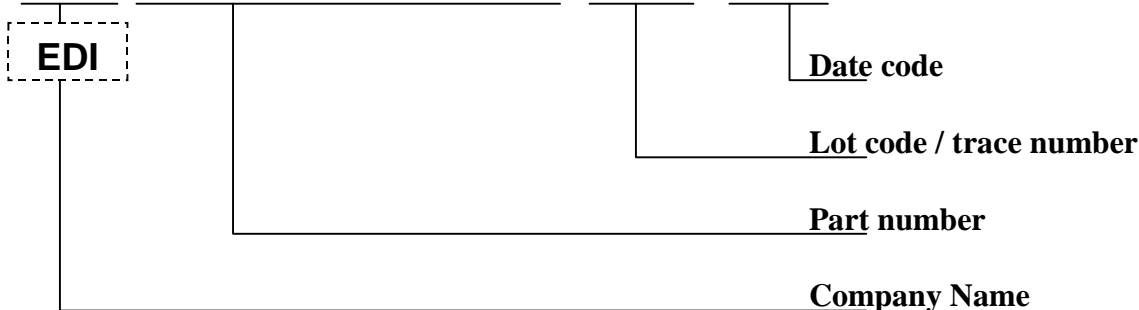
Notes:

- Signal may be high or low in this area.
- When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.



## PRODUCT MARKING

**WED 8P512SRA0100C15 C995 9915**

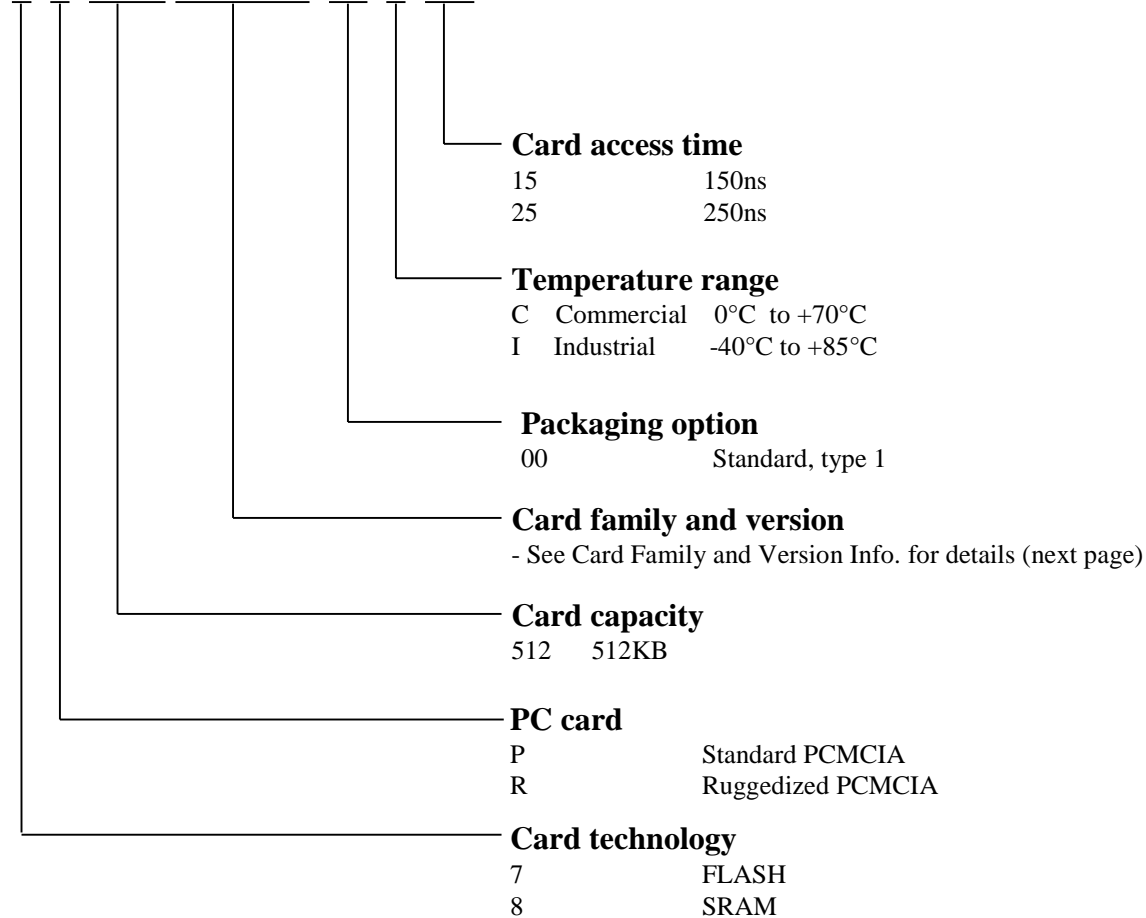


**Note:**

Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2001 all PCMCIA products will be marked only with the WED prefix.

## PART NUMBERING

**8 P 512 SRA01 00 C 15**







**Ordering Information**

**8P XXX SRA YY SS T ZZ**

where

|             |             |              |
|-------------|-------------|--------------|
| <b>XXX:</b> | <b>256*</b> | <b>256KB</b> |
|             | <b>512*</b> | <b>512KB</b> |
|             | <b>001</b>  | <b>1MB</b>   |
|             | <b>002</b>  | <b>2MB</b>   |
|             | <b>004</b>  | <b>4MB</b>   |
|             | <b>006</b>  | <b>6MB</b>   |
|             | <b>008*</b> | <b>8MB</b>   |

\* = Capacities available only in SRA01-SRA04

|            |           |   |
|------------|-----------|---|
| <b>YY:</b> | <b>01</b> | <b>no attribute memory, no Write Protect Switch</b>                                   |
|            | <b>02</b> | <b>with attribute memory, no Write Protect Switch</b>                                 |
|            | <b>03</b> | <b>with Write Protect Switch, no attribute memory</b>                                 |
|            | <b>04</b> | <b>with attribute memory, with Write Protect Switch</b>                               |
|            | <b>11</b> | <b>Extended Battery Backup Time, no attribute memory, no Write Protect Switch</b>     |
|            | <b>12</b> | <b>Extended Battery Backup Time, with attribute memory, no Write Protect Switch</b>   |
|            | <b>13</b> | <b>Extended Battery Backup Time, with Write Protect Switch, no attribute memory</b>   |
|            | <b>14</b> | <b>Extended Battery Backup Time, with attribute memory, with Write Protect Switch</b> |

|            |           |   |
|------------|-----------|---|
| <b>SS:</b> | <b>00</b> | <b>WEDC SRAM Logo Type I</b>  |
|            | <b>01</b> | <b>Blank Housing, Type I</b>  |
|            | <b>02</b> | <b>Blank Housing, Type I Recessed</b>   |
|            | <b>03</b> | <b>WEDC SRAM Logo, Type II (8MB and extended battery backup time)</b>         |
|            | <b>04</b> | <b>Blank Housing, Type II (8MB and extended battery backup time)</b>          |
|            | <b>05</b> | <b>Blank Housing, Type II Recessed (8MB and extended battery backup time)</b> |

|           |          |                   |
|-----------|----------|-------------------|
| <b>T:</b> | <b>C</b> | <b>Commercial</b> |
|           | <b>I</b> | <b>Industrial</b> |

|            |           |              |
|------------|-----------|--------------|
| <b>ZZ:</b> | <b>15</b> | <b>150ns</b> |
|------------|-----------|--------------|



| REVISION HISTORY |         |   |
|------------------|---------|---|
| Date of revision | Version | Description   |
| 23-Dec-98        | -001    | Initial release   |
| 7-Feb-99         | -002    | page 5: 10 years to: min 10 years   |
| May-99           | -003    | Company/Logo change   |
| 28-Sep-99        | -004    | Revised capacities and Edited Pinout  |
| 1-Jun-00         | -005    | Added Page 8, Changed Page Header<br>Added SRA11-14 to Ordering Info, Added<br>SRA11-14 to Battery Info |
| 6-Feb-02         | -006    | Changed Page Header   |
|                  |         |   |
|                  |         |   |

Filename: SRA Dsht Rev 6.ppt

**White Electronic Designs Corporation**

One Research Drive, Westborough, MA 01581, USA

tel: (508) 366 5151

fax: (508) 836 4850

[www.whiteedc.com](http://www.whiteedc.com)



WHITE ELECTRONIC DESIGNS