20W Stereo Digital Class-D Audio Power Amplifier with EQ, DRC and 2.1 Mode

Features

- **Operating Voltage: 8.0V-24V for PVDD – 3.0V~3.6V for DVDD and AVDD**
- **High Efficiency Class D Operation Eliminate the Need of Heatsinks**
- **Digital Serial Audio Input (Stereo Output)**
- **2.1 Mode (2SE + 1BTL)**
- **2.0 Mode (2BTL)**
- **Single-Filter PBTL Mode Support**
- **I²C Address Selection Pin (Chip Select)**
- **I²C Control Interface**
- **Sampling Rate Support from 32kHz to 192kHz**
- **Separated Volume Control from 24dB to Mute**
- **Soft Mute (50% Duty Cycle)**
- **Separate Dynamic Range Control for Satellite and Subchannels**
- **18 Programmable Biquads for Speaker EQ and Other Audio Processing Features**
- **Programmable Coefficients for DRC Filters**
- **DC Blocking Filters, De-emphasis Filters**
- **Support for 3D Effects**
- **Shutdown and Mute Function**
- **Thermal and Over-Current Protections with Auto-Recovery**
- **Space Saving Package TQFP7x7-48P**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD TV**
- **iPod Dock**
- **Sound Bar**

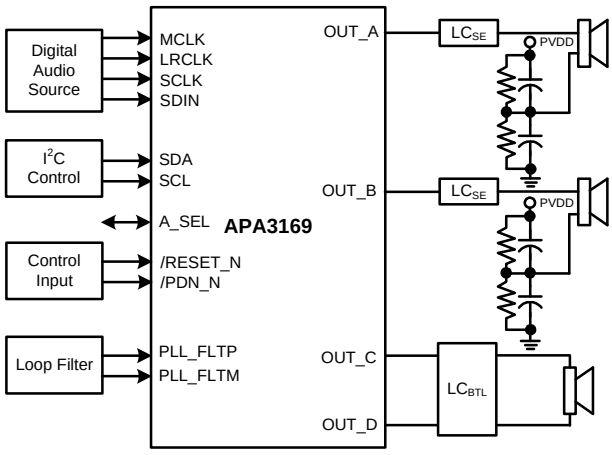
General Description

The APA3169 is a digital input, stereo, high efficiency, Class-D audio amplifier available in a TQFP7x7-48P package.

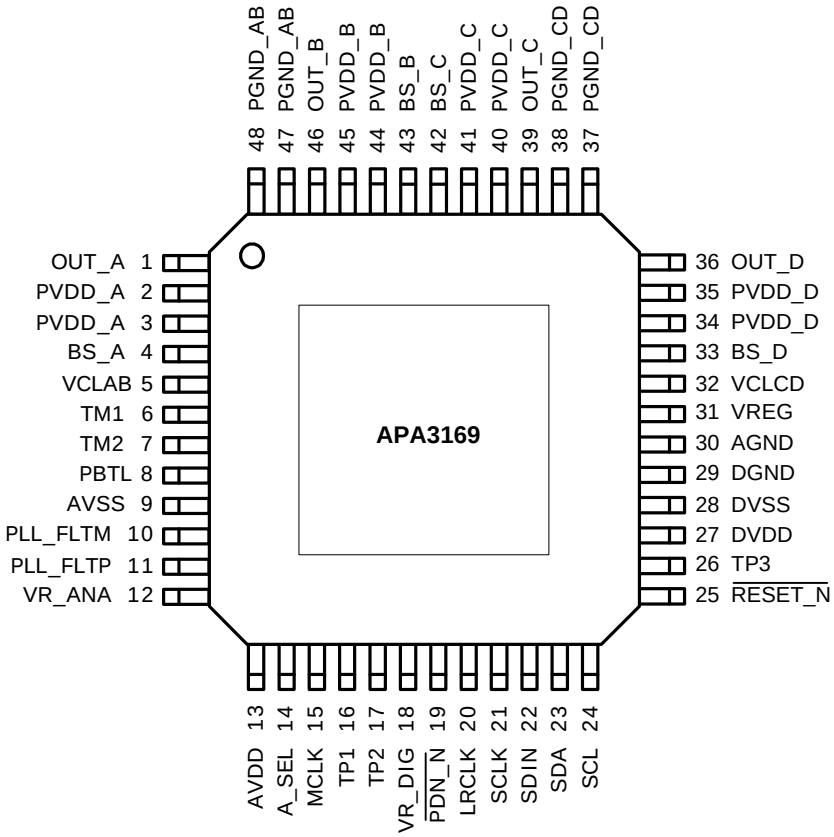
The APA3169 accepts the digital serial audio data and using the digital audio processor to convert the audio data becomes the stereo Class-D output speaker amplifier. This provides the seamless integration between the codec and the speaker amplifier.

The APA3169 is a slave device receiving clocks from external source, and the Class-D's PWM switching frequency is 352.8kHz for the sampling rate 44.1kHz or 384 kHz for sampling 48kHz, depend on the input signal's sampling rate.

Simplified Application Circuit



Pin Configuration



TQFP7x7-48P
(TOP VIEW)

Ordering and Marking Information

APA3169 □□□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code QCA : TQFP7x7-48P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA3169 QCA : 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{PVDD}	Supply Voltage (PVDD_X to PGND_XX)	-0.3 to 26	V
V_{DVDD}	Supply Voltage (DVDD to DVSS)	-0.3 to 6	
V_{AVDD}	Supply Voltage (AVDD to AVSS)	-0.3 to 6	
Input Voltage	Input Voltage (MCLK to AVSS)	-0.5 to 6	
	Input Voltage (PDN, RESET, LRCLK, SCLK, SDIN, SDA, SCL to DVSS)	-0.5 to 6	
	Input Voltage (AVSS, DVSS, AGDN to PGND_XX)	-0.3 to +0.3	
V_{OUT_X}	OUT_X to PGND_XX	-0.3 to +26	
V_{BS_X}	BS_X to PGND_XX	-0.3 to +31	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Soldering Temperature Range, 10 seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TQFP7x7-48P	25	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFP7X7-48P is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{AVDD}, V_{DVDD}	Analog/Digital Supply Voltage (AVDD,DVDD)		3	3.6	V
V_{PVDD}	Full Bridge Stage Supply Voltage (PVDD_X)		8	24	
V_{IH}	High Level Threshold Voltage	$\overline{PDN}$, MCLK, LRCLK, SCLK, SDIN, SDA, SCL, $\overline{RESET}$	2	5	
V_{IL}	Low Level Threshold Voltage	$\overline{PDN}$, MCLK, LRCLK, SCLK, SDIN, SDA, SCL, $\overline{RESET}$	0	0.8	
T_A	Ambient Temperature Range		-40	85	°C
T_J	Junction Temperature Range		-40	125	
R_L(BTL)	Speaker Resistance		6	-	Ω
L_O(BTL)	Output Low Pass Filter Inductance		10	47	μH

Electrical Characteristics

T_A=25°C, V_{PVDD}=18V, V_{AVDD} = V_{DVDD} = 3.3V, R_L=8Ω, BD Mode, f_S=48kHz (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3169			Unit
			Min.	Typ.	Max.	
PWM Operating Conditions						
f_S	Output Sample Rate	32 kHz Data Rate ±2%		256		kHz
		44.1k/88.2k/176.4 kHz Data Rate ±2%		352.8		
		48k/96k/192 kHz Data Rate ± 2%		384		
PLL Input Parameters and External Filter Components						
f_{MCLK}	MCLK Frequency		2.8224	-	24.576	MHz
	MCLK Duty Cycle		40	50	60	%
$tr/tf_{(MCLK)}$	Rise/Fall Time for MCLK		-	-	5	ns
	LRCLK Allowable Drift before LRCLK Reset		-	-	4	MCLKs
	External PLL Filter Capacitor C1	SMD 0603 Y5V	-	47	-	nF
	External PLL Filter Capacitor C2	SMD 0603 Y5V	-	4.7	-	
	External PLL Filter Resistor R		-	470	-	Ω
DC CHARACTERISTICS						
V_{OH}	High Level output voltage(A_SEL and SDA)	I_{OH}=-4mA, DVDD=AVDD=3V	2.4	-	-	V
V_{OL}	Low Level output voltage(A_SEL and SDA)	I_{OL}=4mA, DVDD=AVDD=3V	-	-	0.5	V
I_{IL}	Low Level Input Current	V_I<V_{IL}, DVDD=AVDD=3.6V	-	-	75	μA
I_{IH}	High Level Input Current	V_I>V_{IH}, DVDD=AVDD=3.6V	-	-	75	μA
I_{DD}	3.3V Supply Current (AVDD+DVDD)	Normal Mode (No LC, No load)	-	14	20	mA
		Reset (No LC, No load)	-	14	20	
I_{PVDD}	Full Bridge Stage Supply Current (PVDD_X)	Normal Mode (No LC, No load)	-	18	36	
		Reset (No LC, No load)	-	0.5	1.6	
$r_{DS(ON)}$	Drain to source resistance,LS	T_J=25°C, includes metallization resistance	-	180	-	mΩ
	Drain to source resistance,HS	T_J=25°C, includes metallization resistance	-	180	-	mΩ
V_{UVP}	Undervoltage protection limit	PVDD falling	-	6.8	-	V
$V_{UVP,hyst}$	Undervoltage protection limit	PVDD rising	-	7.2	-	V
T_{TP}	Thermal Protection Threshold		-	150	-	°C
	Thermal Protection Threshold Hysteresis		-	30	-	

Electrical Characteristics (Cont.)

T_A=25°C, V_{PVDD}=18V, V_{AVDD} = V_{DVDD} = 3.3V, R_L=8Ω, BD Mode, f_S=48kHz (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA3169			Unit
				Min.	Typ.	Max.	
DC CHARACTERISTICS (CONT.)							
OLPC	Overload protection counter	f_{PWM}=384kHz		-	0.63	-	ms
I_{OC}	Overcurrent limit protection	Resistor - programmable, max. current		-	4.5	-	A
I_{OCT}	Overcurrent response time			-	150	-	ns
R_{OUT}	Internal pull-down resistance at each OUT_X	Ccaopnanceitcoter dchwahrgeen. drivers are tristated to provide bootstrap		-	3	-	kΩ
AC CHARACTERISTICS							
P_O	Output Power	BTL,THD+N=1%, f_{in}=1kHz,R_L=8Ω	V_{PVDD}=18V	14.5	16	-	W
			V_{PVDD}=12V	6.5	7.2	-	
			V_{PVDD}=8V	2.9	3.2	-	
		BTL,THD+N=10 %,f_{in}=1kHz,R_L=8 Ω	V_{PVDD}=18V	-	20	-	
			V_{PVDD}=12V	-	9	-	
			V_{PVDD}=8V	-	4	-	
		PBTL,THD+N=1 %,f_{in}=1kHz,R_L=4 Ω	V_{PVDD}=18V	-	30.5	-	
			V_{PVDD}=12V	-	13.7	-	
		PBTL,THD+N=1 0%,f_{in}=1kHz,R_L= 4Ω	V_{PVDD}=18V	-	37.1	-	
			V_{PVDD}=12V	-	16.9	-	
		SE,THD+N=1%,f_{in}=1kHz,R_L=4Ω	V_{PVDD}=18V	-	7.5	-	
			V_{PVDD}=12V	-	3.4	-	
		SE,THD+N=10% ,f_{in}=1kHz,R_L=4Ω	V_{PVDD}=18V	-	9.5	-	
			V_{PVDD}=12V	-	4.3	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz,R_L=8Ω	V_{PVDD}=18V, Po=1W	-	0.06	-	%
			V_{PVDD} =12V, Po=1W	-	0.13	-	
			V_{PVDD}=8V, Po=1W	-	0.2	-	
Vn	Noise Output Voltage	With A-Weighting Filter (Volume=0dB)		-	200	-	μVms
Crosstalk	Channel Separation	P_O=0.25W, R_L=8Ω, f_{in}=1kHz		-	-72	-	dB
SNR	Signal to Noise Ratio	R_L=8Ω, Po=16W, A-Weighting Filter (Volume =0dB)		-	95	-	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_O=1V_{rms}		-	-70	-	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_O=1V_{rms}		-	-110	-	

Serial Audio Ports Slave Mode

Over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3169			Unit
			Min.	Typ.	Max.	
f_{SCLK}	Frequency, SCLK 32xf_S, 48xf_S, 64xf_S	C_L=30pF	1.024	-	12.288	MHz
t_{Setup1}	Setup Time, LRCLK to SCLK Rising Edge		10	-	-	ns
t_{Hold1}	Hold Time, LRCLK to SCLK Rising Edge		10	-	-	
t_{Setup2}	Setup Time, SDIN to SCLK Rising Edge		10	-	-	
t_{Hold}	Hold Time, SDIN to SCLK Rising Edge		10	-	-	
	LRCLK Frequency		32	48	192	kHz
	LRCLK Duty Cycle		40	50	60	%
	SCLK Duty Cycle		40	50	60	
	SCLK Rising Edges Between LRCLK Riding Edges		32	-	64	SCLK edges
$t_{(edge)}$	LRCLK Clock Edge With Respect To The Falling Edge of SCLK		-1/4	-	1/4	SCLK period
tr/tf (SCLK/LRCLK)	Rise/Fall Time for SCLK/LRCLK		-	-	8	ns

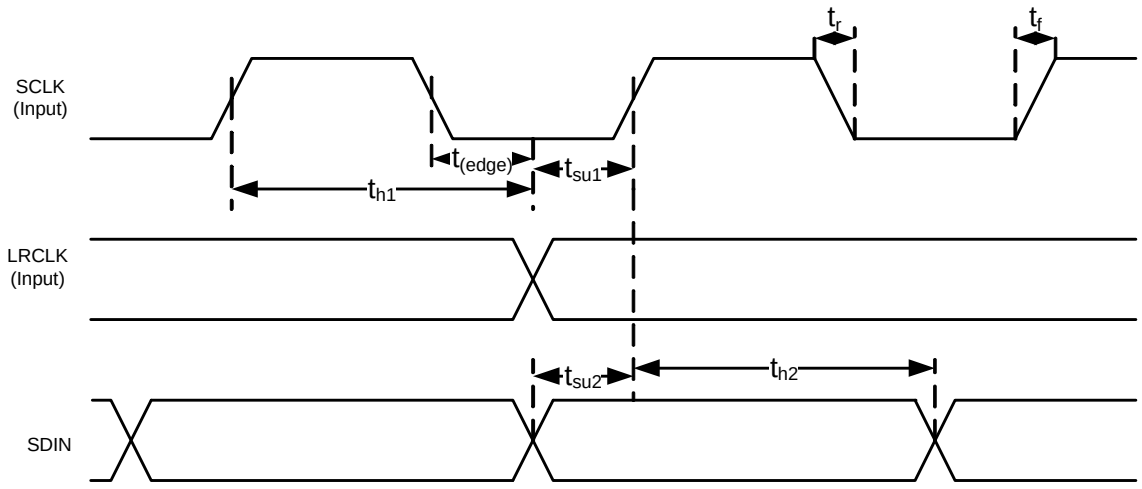


Figure 1. Slave Mode Serial Data Interface Timing

I²C Serial Control Port Operation

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3169			Unit
			Min.	Typ.	Max.	
f_{SCL}	Frequency, SCL	No Wait States	-	-	400	kHz
$t_{W(H)}$	Pulse Duration, SCL High		0.6	-	-	µs
$t_{W(L)}$	Pulse Duration, SCL Low		1.3	-	-	
t_r	Rise Time, SCL and SDA		-	-	300	ns
t_f	Fall Time, SCL and SDA		-	-	300	
t_{setup1}	Setup Time, SCL to SDA		100	-	-	
t_{hold1}	Hold Time, SCL to SDA		0	-	-	
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition		1.3	-	-	µs
t_{setup2}	Setup Time, SCL to Start Condition		0.6	-	-	
t_{hold2}	Hold Time, Start condition to SCL		0.6	-	-	
t_{setup3}	Setup Time, SCL to Stop Condition		0.6	-	-	
C_L	Load Capacitance for Each Bus Line		-	-	400	pF

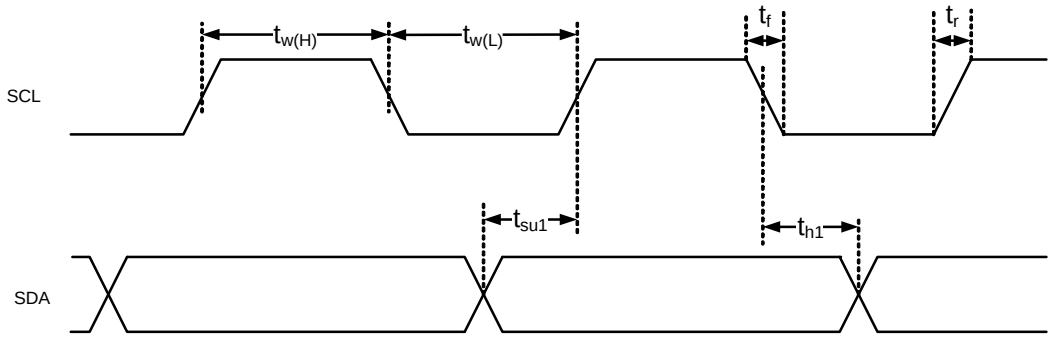


Figure 2. SCL and SDA Timing

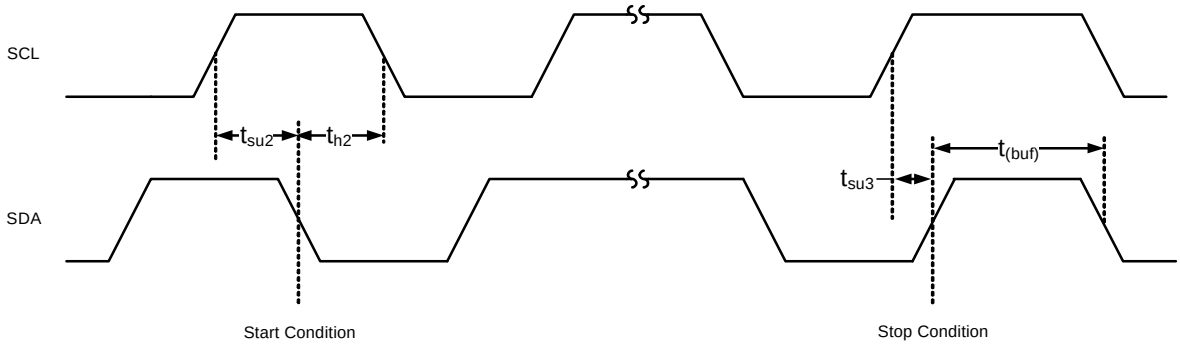


Figure 2. SCL and SDA Timing

Reset Timing

Control signal parameters over recommended operating conditions (unless otherwise noted). Please refer to “Recommended Use Model” section on usage of all terminals.

Symbol	Parameter	Test Conditions	APA3169			Unit
			Min.	Typ.	Max.	
$t_{p(\overline{RST})}$	Pulse Duration, RESET Active.	No Load	100	-	-	µs
$t_{d(12C\_Ready)}$	Time to Enable I^2C		-	-	13.5	ms

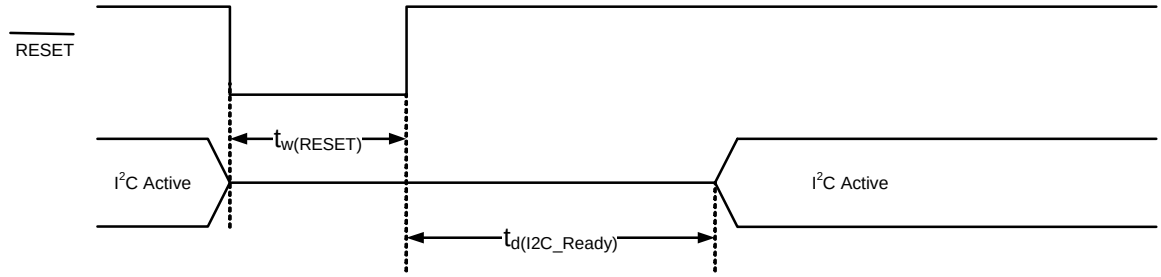
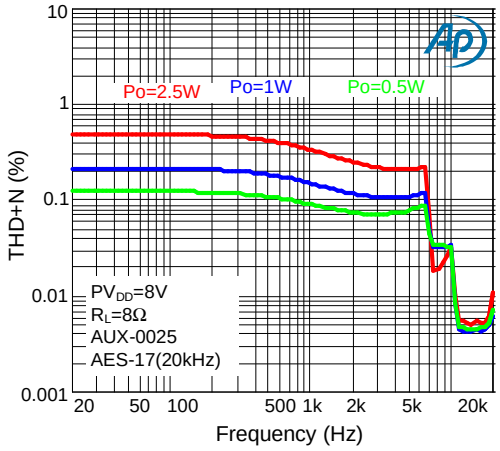


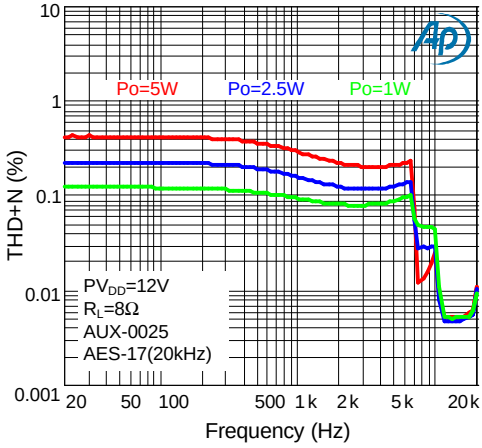
Figure 4. Reset Timing

Typical Operating Characteristics, BTL Configuration

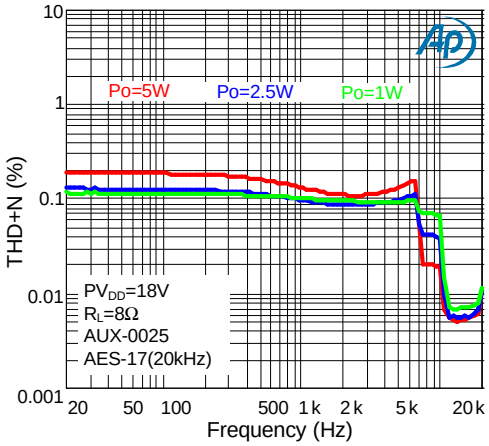
THD+N vs. Frequency



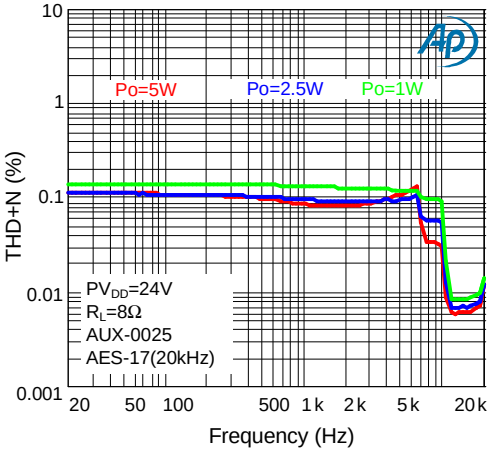
THD+N vs. Frequency



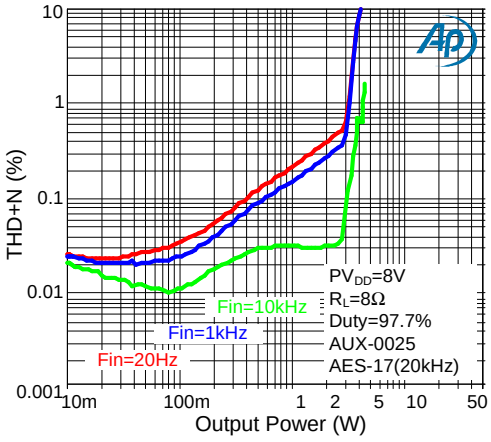
THD+N vs. Frequency



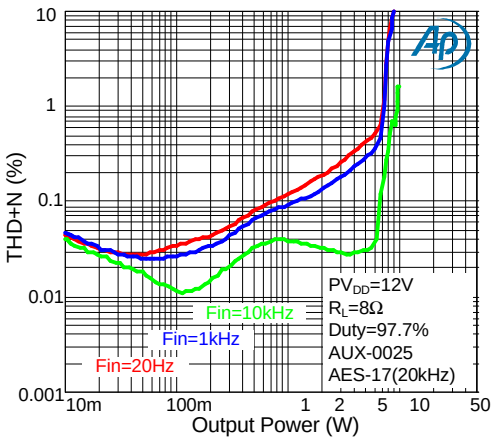
THD+N vs. Frequency



THD+N vs. Output Power

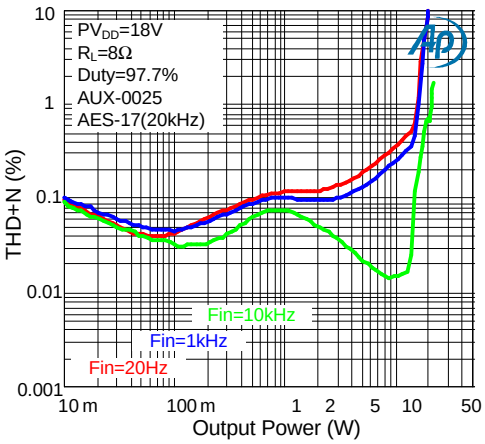


THD+N vs. Output Power

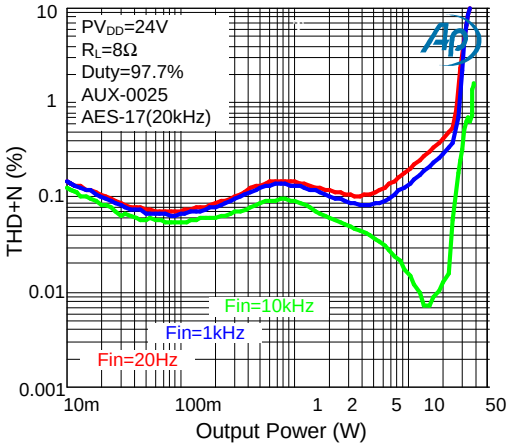


Typical Operating Characteristics, BTL Configuration(Cont.)

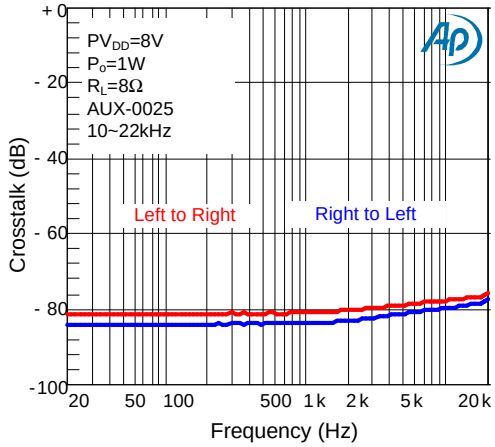
THD+N vs. Output Power



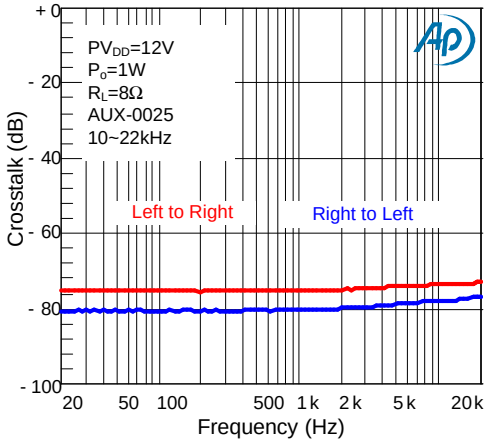
THD+N vs. Output Power



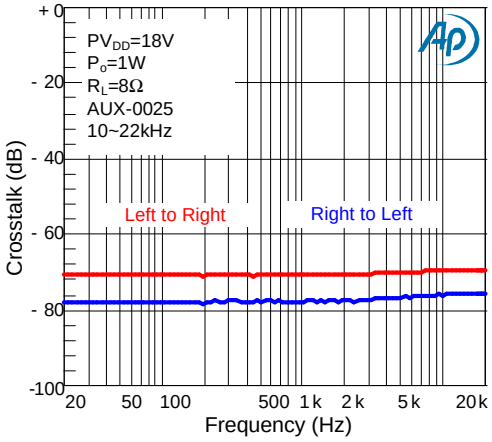
Crosstalk vs. Frequency



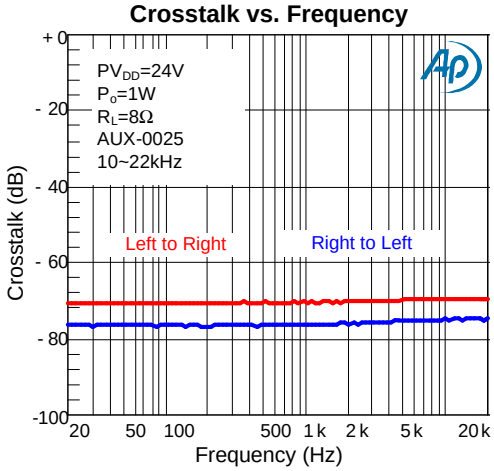
Crosstalk vs. Frequency



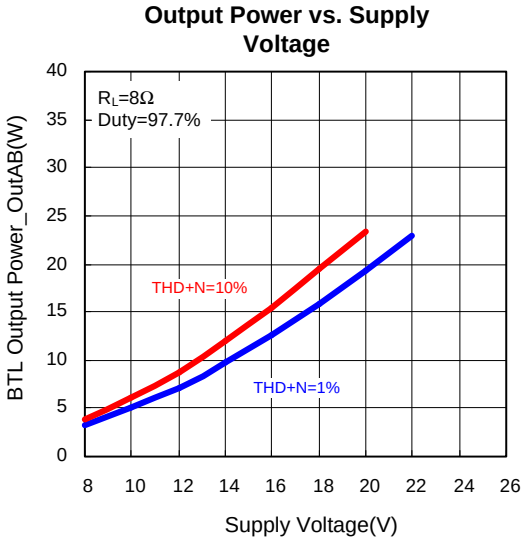
Crosstalk vs. Frequency

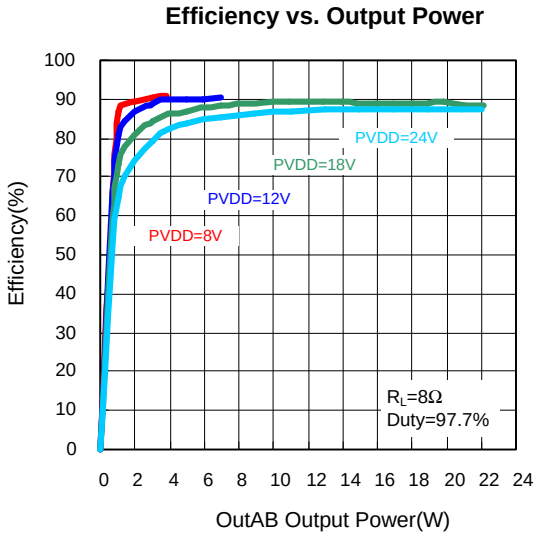


Crosstalk vs. Frequency



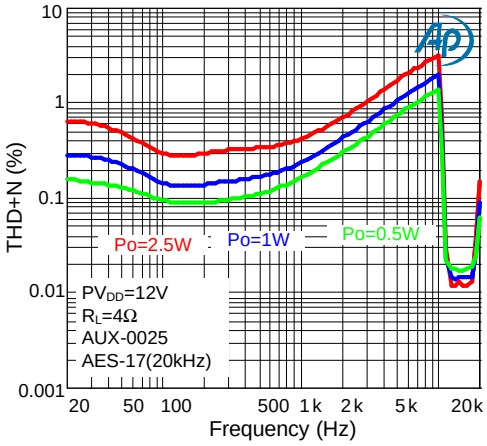
Typical Operating Characteristics, BTL Configuration(Cont.)



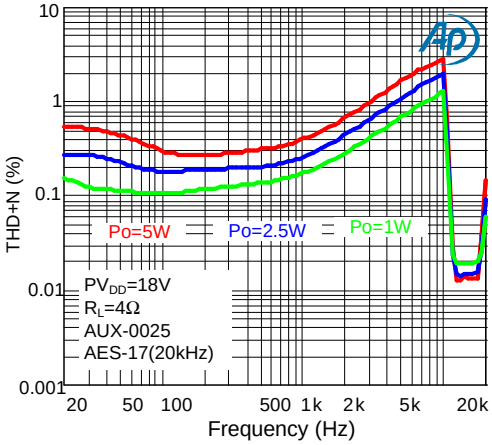


Typical Operating Characteristics, SE Configuration

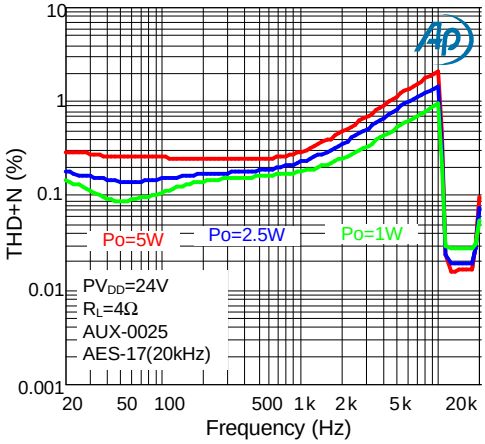
THD+N vs. Frequency



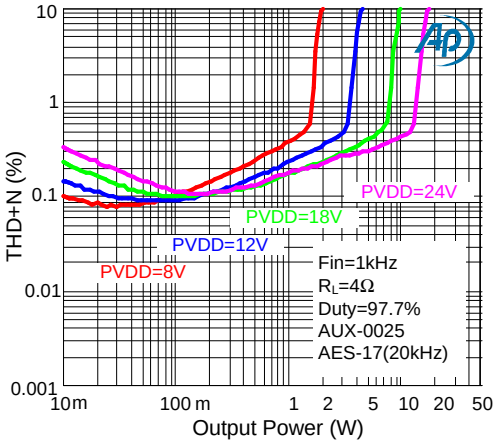
THD+N vs. Frequency



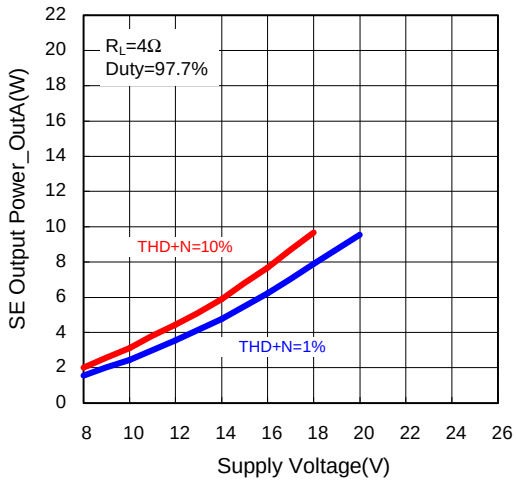
THD+N vs. Frequency



THD+N vs. Output Power

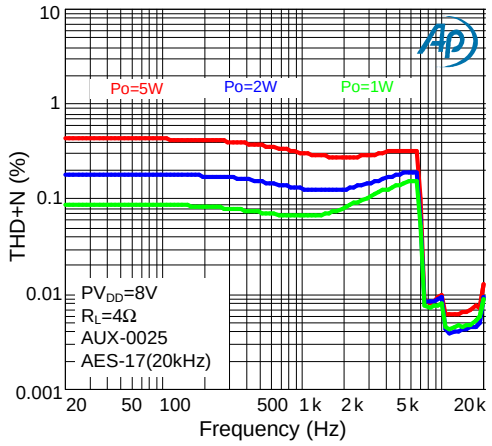


Output Power vs. Supply Voltage

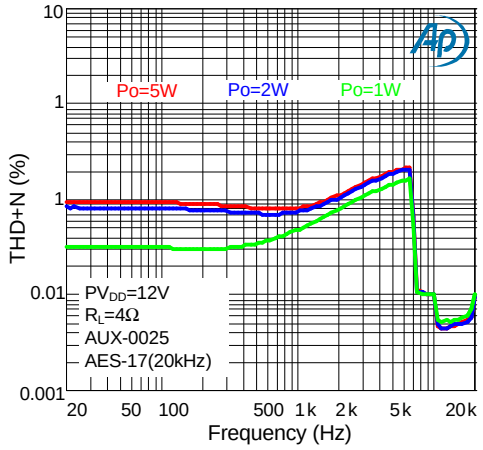


Typical Operating Characteristics, PBTL Configuration

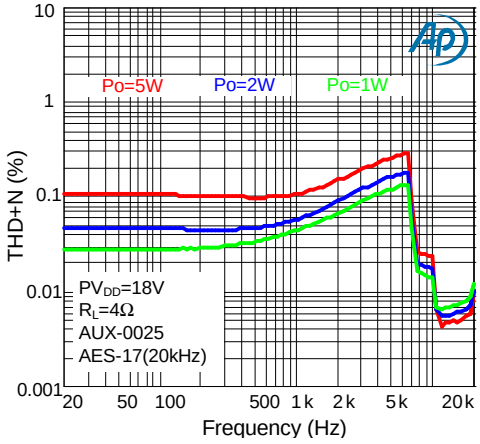
THD+N vs. Frequency



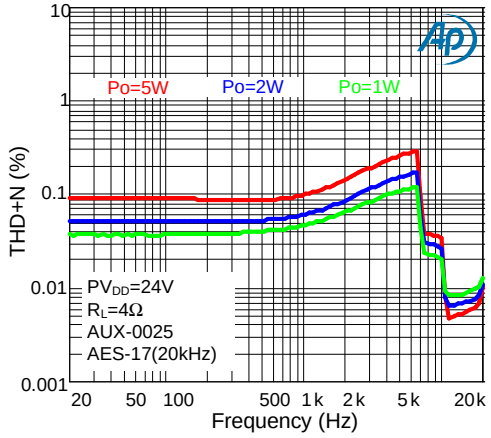
THD+N vs. Frequency



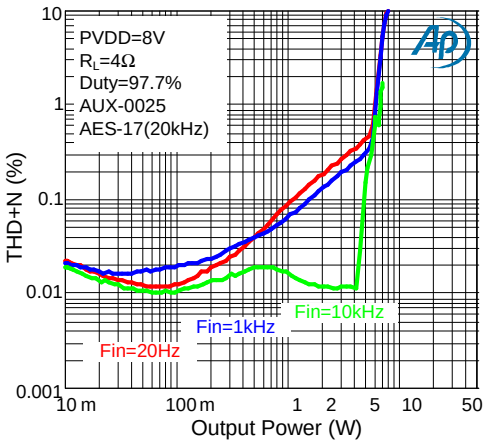
THD+N vs. Frequency



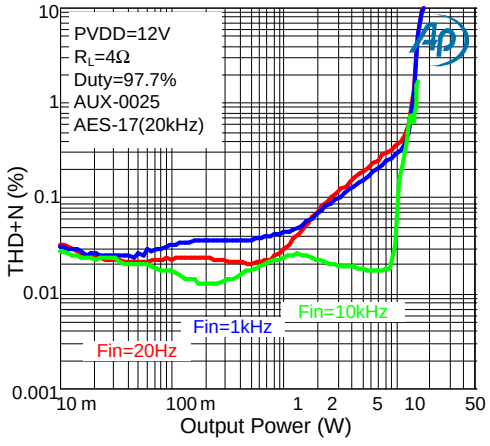
THD+N vs. Frequency



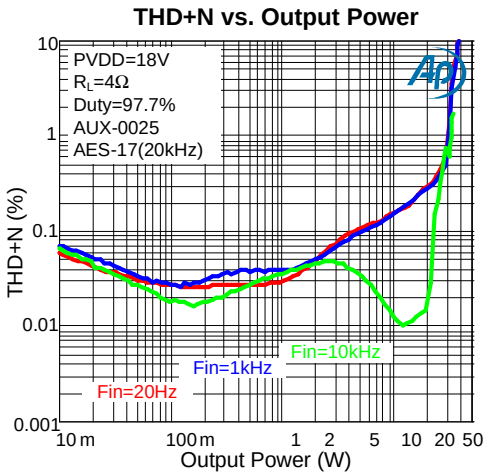
THD+N vs. Output Power

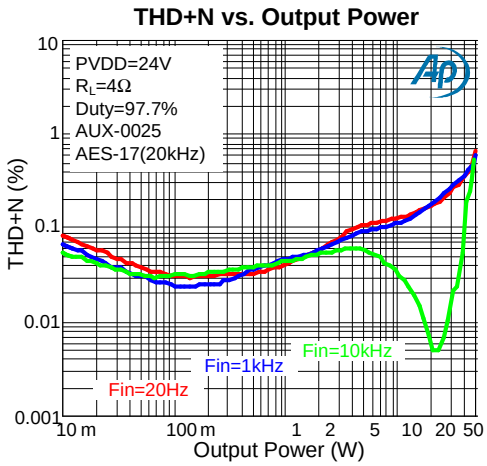


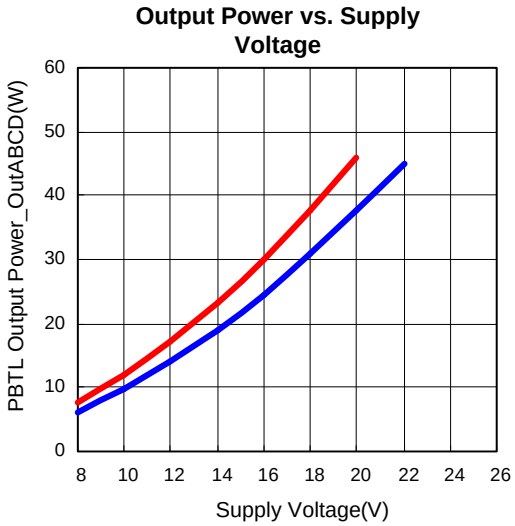
THD+N vs. Output Power



Typical Operating Characteristics, PBTL Configuration(Cont.)







Pin Description

PIN		I/O/P	FUNCTION
NO.	NAME		
1	OUT_A	O	Output,half-bridge A
2,3	PVDD_A	P	Power supply input
4	BS_A	P	High-side bootstrap supply for half-bridge A
5	VCLAB	P	internal 3.3V reference voltage
6	TM1	I	Test mode input
7	TM2	I	Test mode input
8	PBTL	I	low means BTL or SE mode;high means PBTL mode
9	AVSS	P	analog 3.3V supply ground
10	PLL_FLTM	O	PLL negative loop filter
11	PLL_FLTP	O	PLL postive loop filter
12	VR_ANA	P	analog regulator
13	AVDD	P	3.3V amalog power supply
14	A_SEL	I/O	input: device address, output : fault
15	MCLK	I	Master clock input
16	TP1	I/O	Test mode probe
17	TP2	I/O	Test mode probe
18	VR_DIG	P	digital regulator
19	PDN_N	I	Power down,active low
20	LRCLK	I	input serial audio data left/right clock
21	SCLK	I	Serial audio data clock.
22	SDIN	I	Serial audio data input
23	SDA	I/O	I2C serial control data interface input/output
24	SCL	I	I2C serial control clock input
25	RESET_N	I	Reset,active low
26	TP3	I/O	Test mode probe
27	DVDD	P	3.3V digital power supply
28	DVSS	P	Digital ground
29	DGND	P	digital ground for power stage
30	AGND	P	analog ground for power stage
31	VREG	P	Not to be used for powering external circuitry
32	VCLCD	P	internal 3.3V reference voltage
33	BS_D	P	High-side bootstrap supply for half-bridge D
34,35	PVDD_D	P	Power supply input
36	OUT_D	O	output,half bridge D
37,38	PGND_CD	P	Power ground for half-bridge C and D
39	OUT_C	O	output,half-bridge C

Pin Description

PIN		I/O/P	FUNCTION
NO.	NAME		
40,41	PVDD_C	P	Power supply input
42	BS_C	P	High-side bootstrap supply for half-bridge C
43	BS_B	P	High-side bootstrap supply for half-bridge B
44,45	PVDD_B	P	Power supply input
46	OUT_B	O	output ,half bridge B
47,48	PGND_AB	P	Power ground for half-bridge A and B

Block Diagram

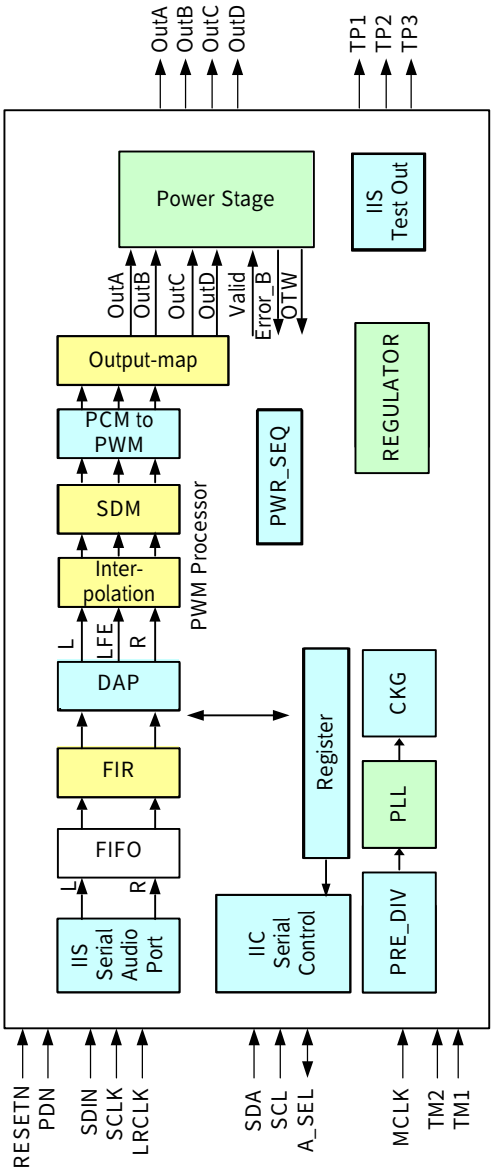


Figure 5. Block Diagram

Block Diagram

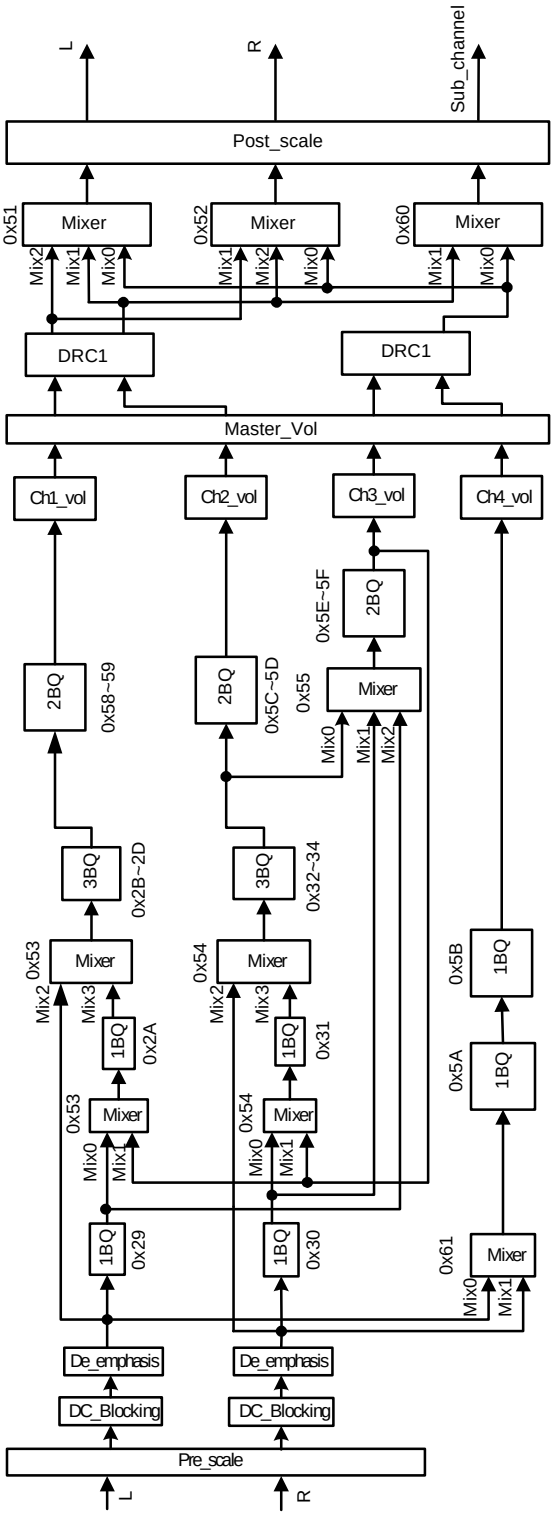
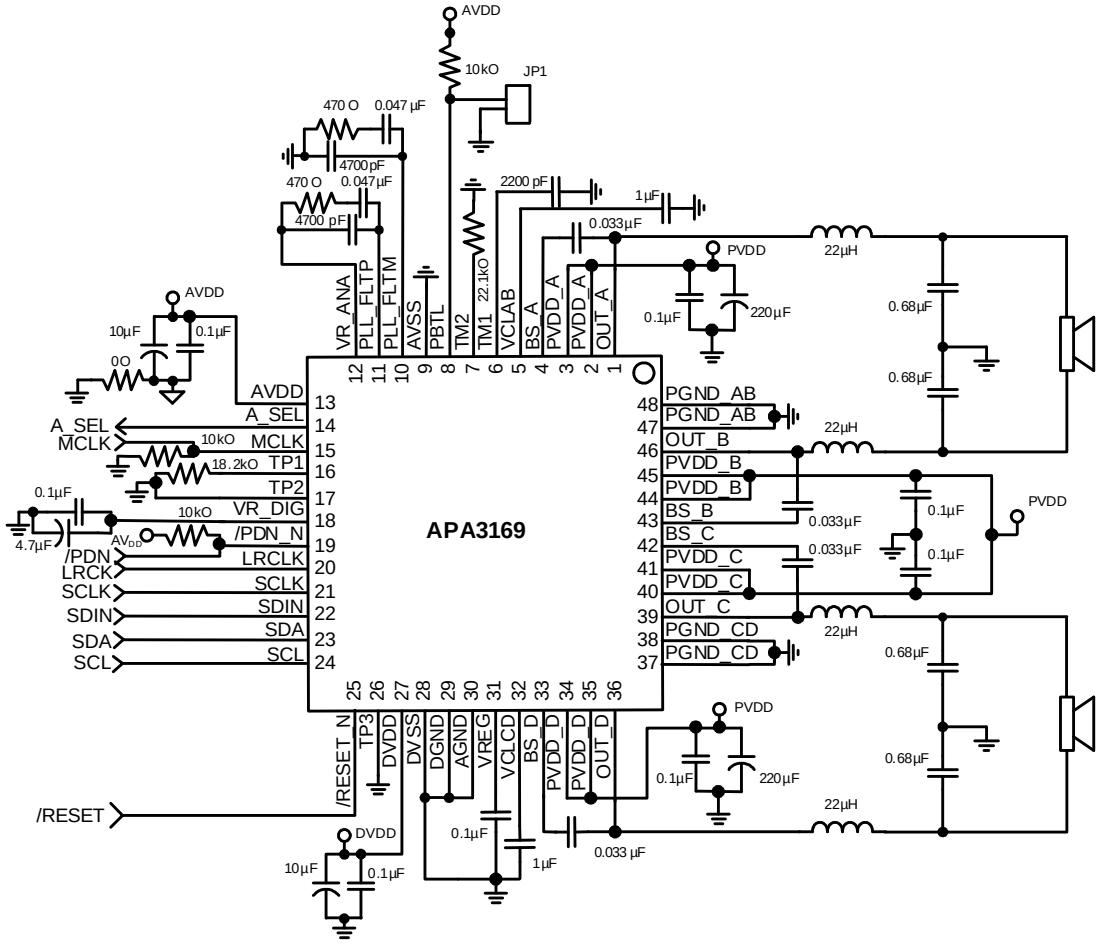


Figure 6. DAP Block Diagram

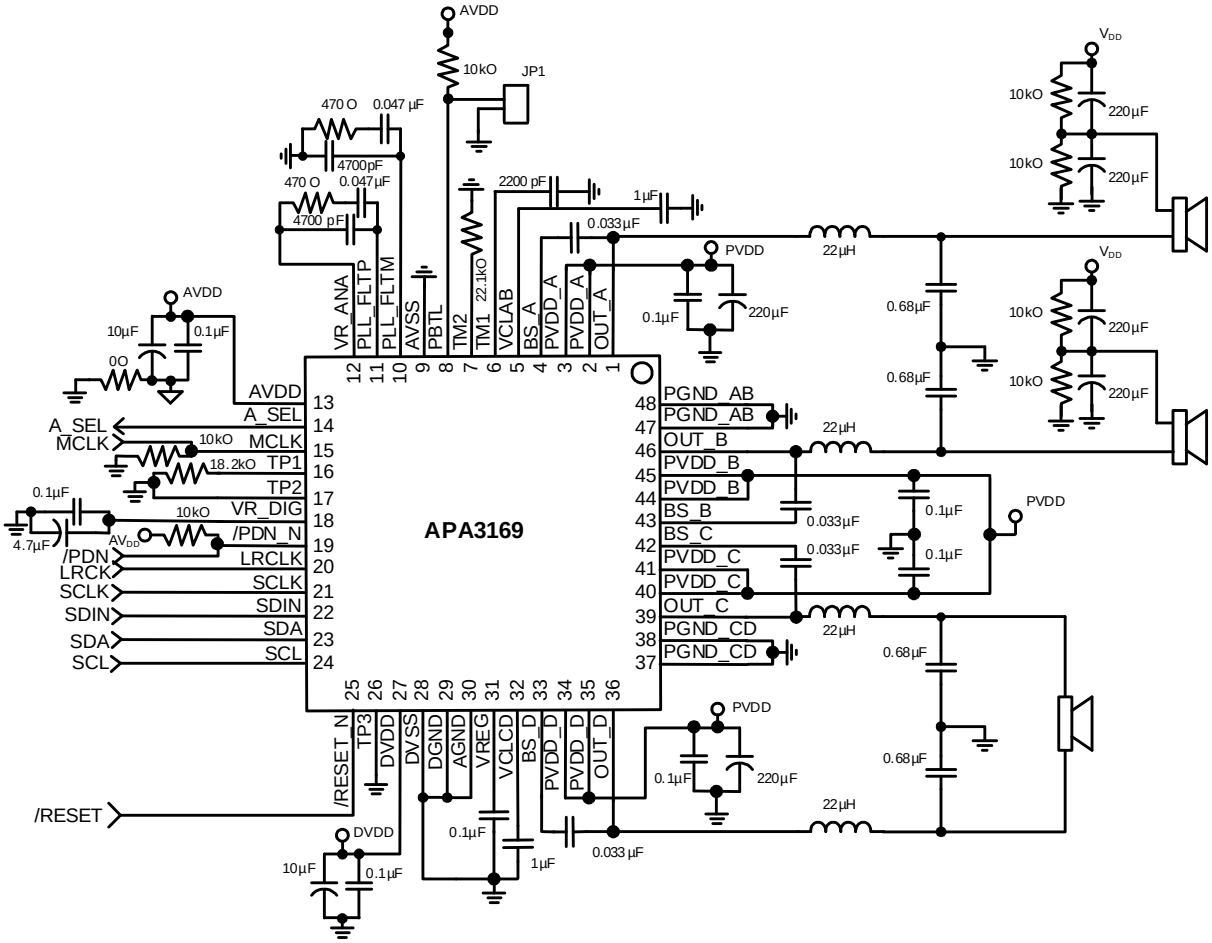
Typical Application Circuit

2.0 Channel



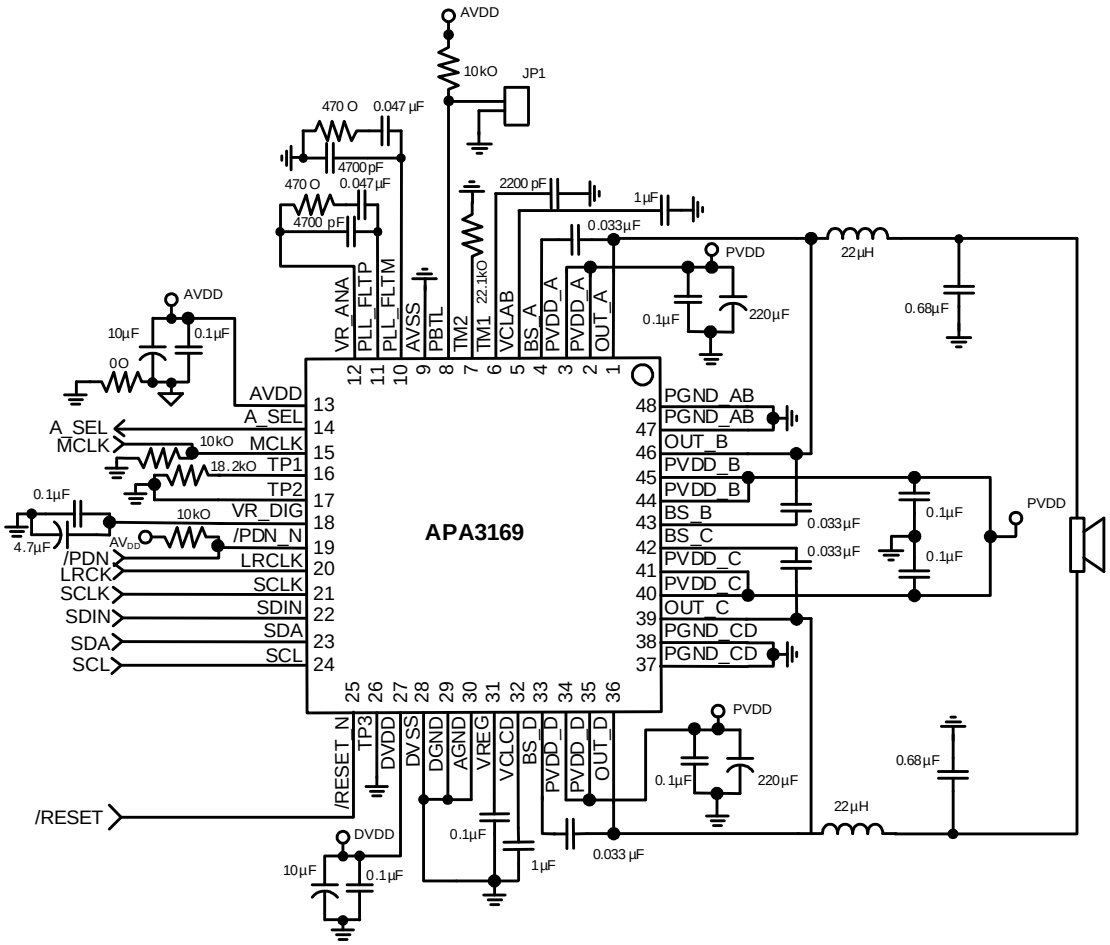
Typical Application Circuit

2.1 Channel



Typical Application Circuit

PBTL



Function Description

POWER SUPPLY

To facilitate system design, the APA3169 needs only a 3.3-V supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BS_x), and power-stage supply pins (PVDD_x). The gate drive voltages (VCLAB and VCLCD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BS_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (VCL_x) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 256 kHz to 384 kHz, it is recommended to use 33-nF 50-V X7R capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_x). For optimal electrical performance, EMC compliance, and system reliability, it is important that each PVDD_x pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin.

The APA3169 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

DEVICE PROTECTION SYSTEM

Overcurrent (OC) Protection With Current Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current further increasing, i.e., it performs a cycle-by-cycle current-limiting function, rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current condition situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. The device returns to normal operation once the fault condition (i.e., a short circuit on the output) is removed. Current limiting and overcurrent protection are not independent for half-bridges.

That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

Overtemperature Protection

The APA3169 has over temperature-protection system. If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and /FAULT being asserted low. The APA3169 recovers automatically once the temperature drops approximately 30°C

Function Description (Cont.)

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the APA3169 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit and ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach 7.6 V and 2.7 V, respectively. Although PVDD and AVDD are independently monitored, a supply voltage drop below the UVP threshold on AVDD or either PVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and /FAULT being asserted low.

SERIAL DATA INTERFACE

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The APA3169 DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, and I2S serial data formats.

PWM Section

The APA3169 DAP device uses noise-shaping to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has individual channel dc blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual channel de-emphasis filters are included and can be enabled and disabled. Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 98.4%.

SERIAL INTERFACE CONTROL AND TIMING

The I^2S mode is set by writing to register 0x04.

I^2S Timing

I^2S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64xf_s is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

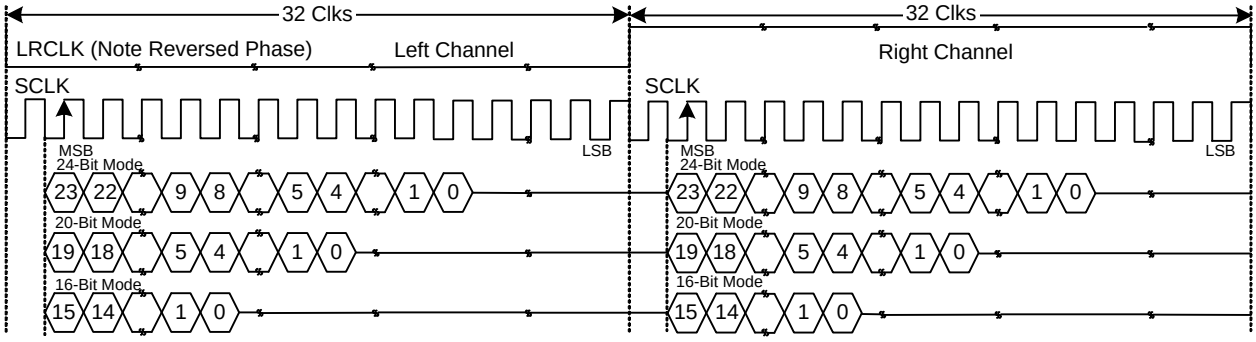


Figure 7. I^2S 64 f_s Format

Function Description (Cont.)

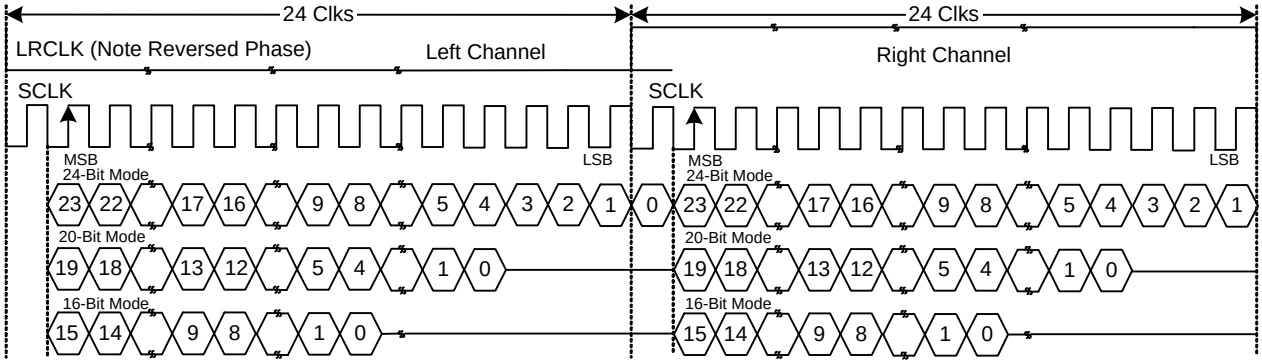


Figure 8. I²S 48 f_S Format

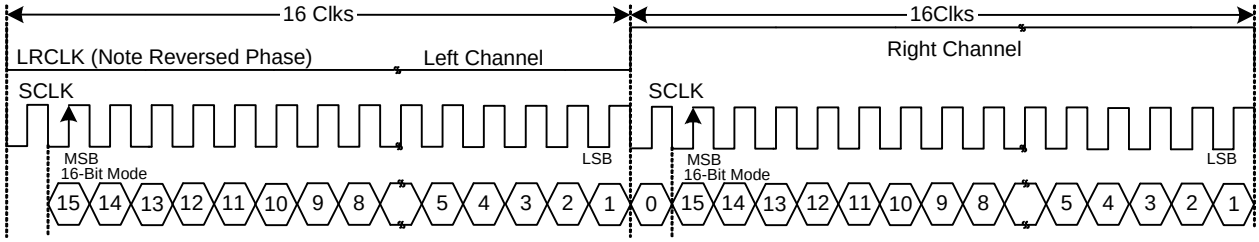


Figure 9. I²S 32 f_S Format

Left-Justified

Left-justified (LJ) timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is high; for the right channel, the LRCLK is low. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines when LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

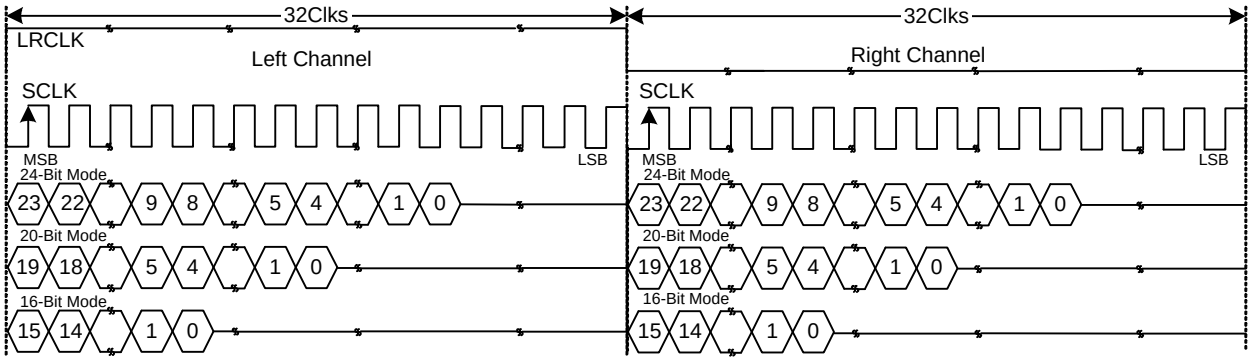


Figure 10. Left-Justified 64 f_S Format

Function Description (Cont.)

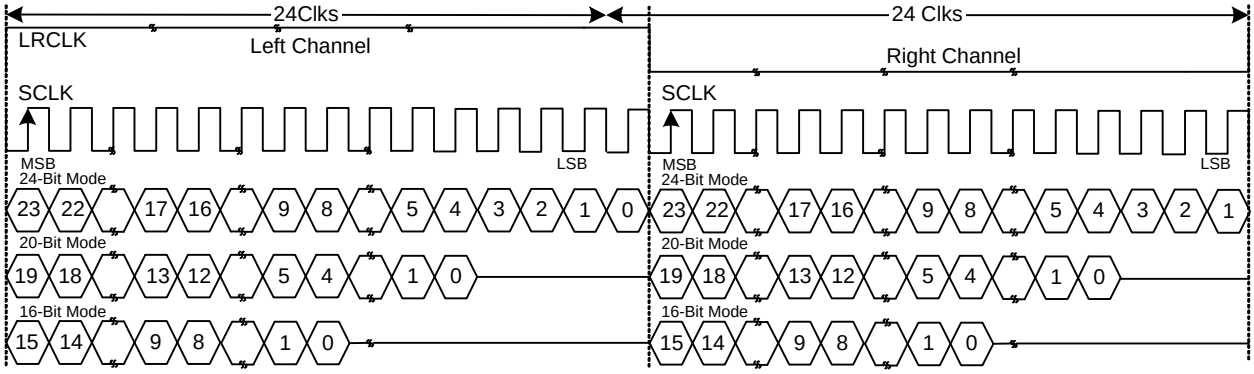


Figure 11. Left-Justified 48 f_S Format

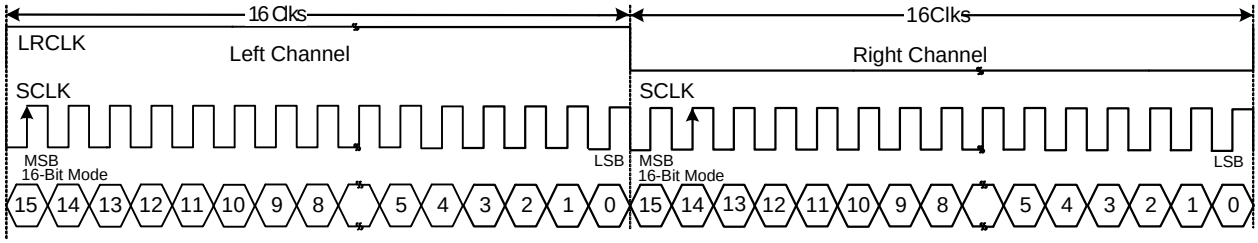


Figure 12. Left-Justified 32 f_S Format

Right-Justified

Right-justified (RJ) timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is high; for the right channel, the LRCLK low. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. After LRCLK toggles, for 24bit data, the first bit of data appears on the data 8 bit-clock. In RJ mode, the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

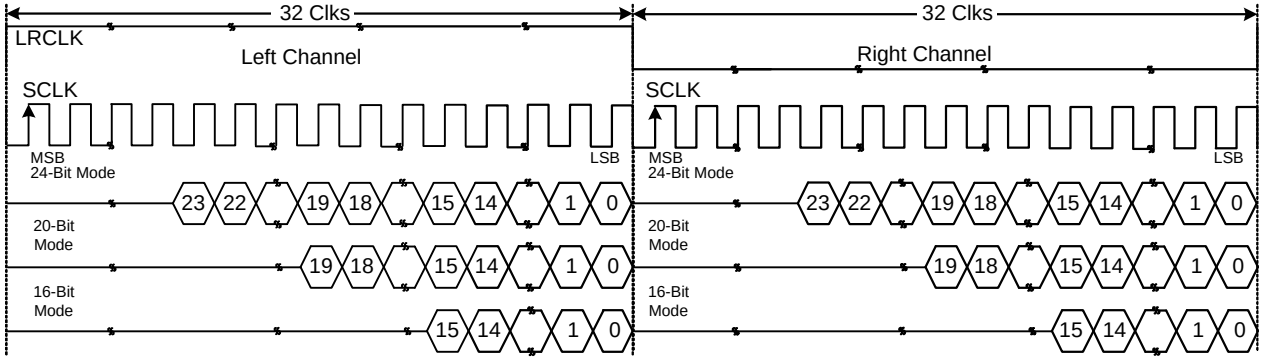


Figure 13. Right-Justified 64 f_S Format

Function Description (Cont.)

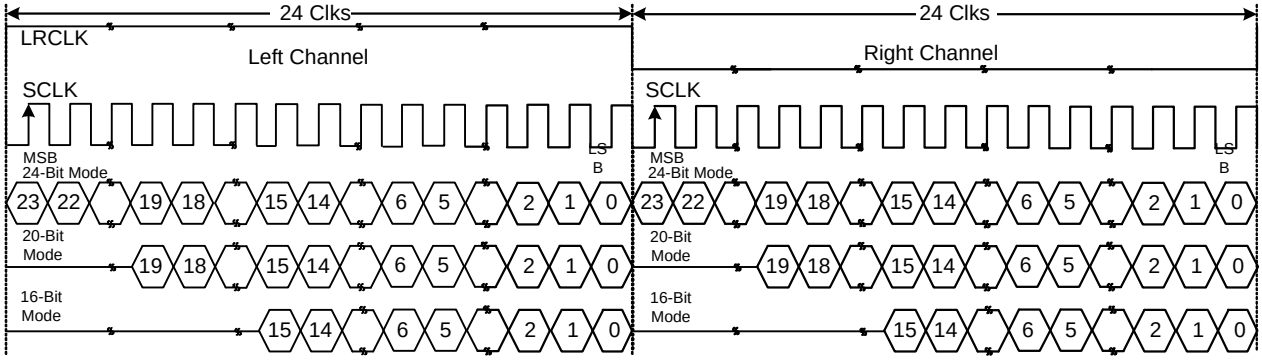


Figure 14. Right-Justified 48 f_S Format

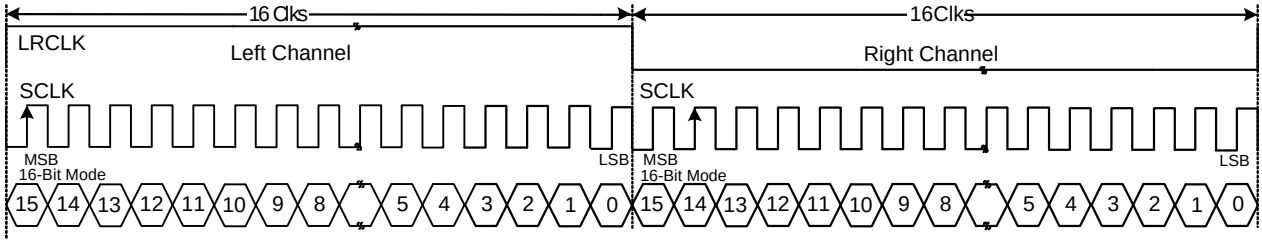


Figure 15. Right-Justified 32 f_S Format

I²C Serial Control Interface

The APA3169 DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol. Besides, it provides both 100kHz and 400kHz data transfer rates to single and multiple bytes write and read operations.

This is a slave only device, and it doesn't support a multi-master bus environment or wait state insertion. The function of the control interface is to read device status and to program the registers of the device.

The DAP supports the standard-mode I²C bus operation (100kHz maximum) and the fast I²C bus operation (400kHz maximum). Without I²C wait cycles, the DAP performs I²C operations.

General I²C Operation

The I²C bus uses SDA (data) and SCL (clock) to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. With the most significant bit (MSB) transferred first, the address and data can be transferred in byte (8bit) format. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the SDA when the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock. These conditions are shown in Figure 10. The master generates the 7bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The APA3169 holds SDA low during the acknowledge clock to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

Function Description (Cont.)

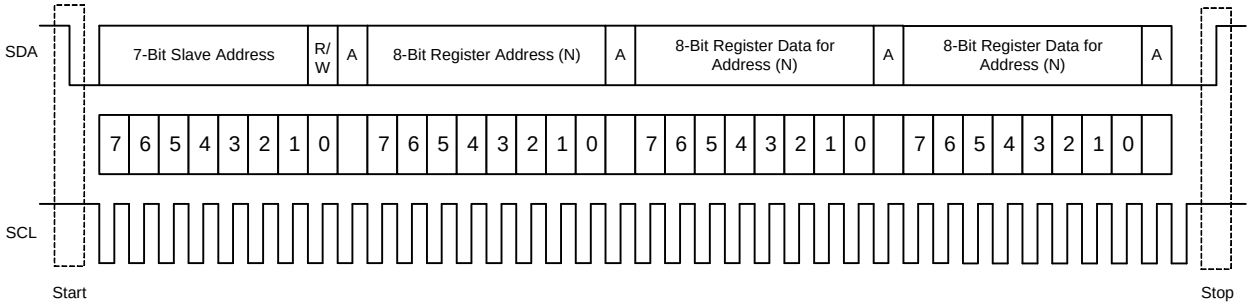


Figure 16. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 16.

Pin A_SEL defines the I2C device address. An external 15kΩ pulldown on this pin gives a device address of 0x34 and a 15kΩ pullup gives a device address of 0x36. The 7-bit address is 0011 010 (0x34) or 0011 011 (0x36).

Single- and Multiple-Byte Transfers

The serial control interface supports single-byte and multiple-byte (R/W) operations for sub-addresses 0x00 to 0x1F. However, for the sub-addresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the sub-address assigned, as long as the master device continues to respond with acknowledges. If a particular sub-address does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific sub-address.

Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APA3169 also supports sequential I²C addressing. For write transactions, if a sub-address is issued and followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APA3169. For I²C sequential write transactions, the sub-address then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last sub-address, the data for the last sub-address is discarded. However, if all other data written is accepted, only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 17, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct I2C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APA3169 internal memory address being accessed. After receiving the address byte, the APA3169 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APA3169 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

Function Description (Cont.)

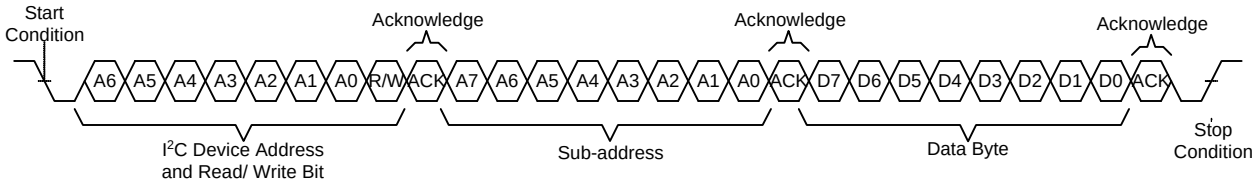


Figure 17. Single-Byte Write Transfer

Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 18. After receiving each data byte, the APA3169 responds with an acknowledge bit.

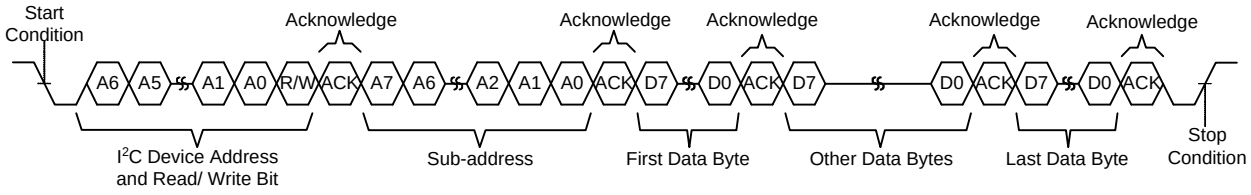


Figure 18. Multiple-Byte Write Transfer

Single-Byte Read

As shown in Figure 19, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/W bit becomes a 0. After receiving the APA3169 address and the read/write bit, APA3169 responds with an acknowledge bit. Besides, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APA3169 address and the read/write bit again. This time the read/ write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the APA3169 again responds with an acknowledge bit. And then, the APA3169 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

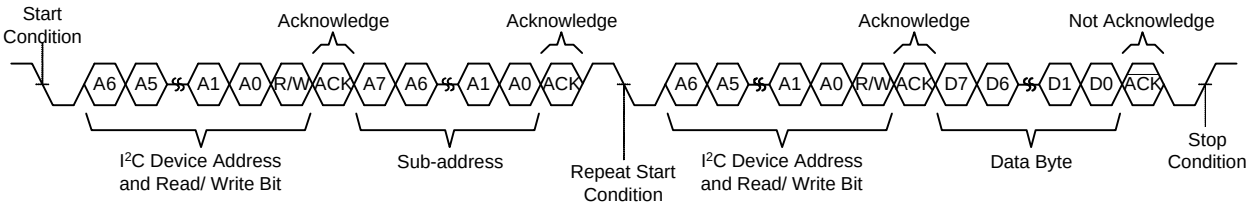


Figure 19. Single-Byte Read Transfer

Function Description (Cont.)

Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the APA3169 to the master device as shown in Figure 20. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

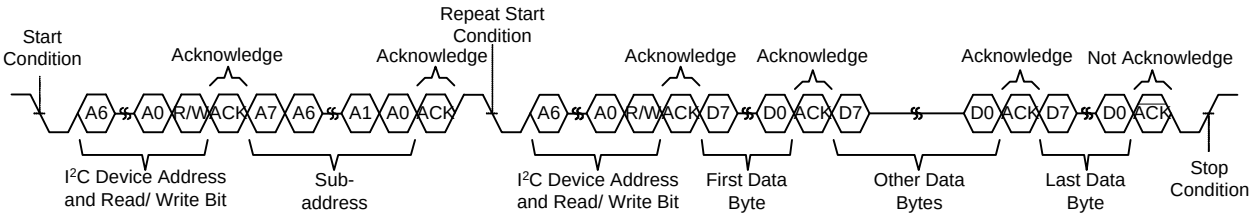


Figure 20. Multiple-Byte Read Transfer

Output Mode and MUX Selection

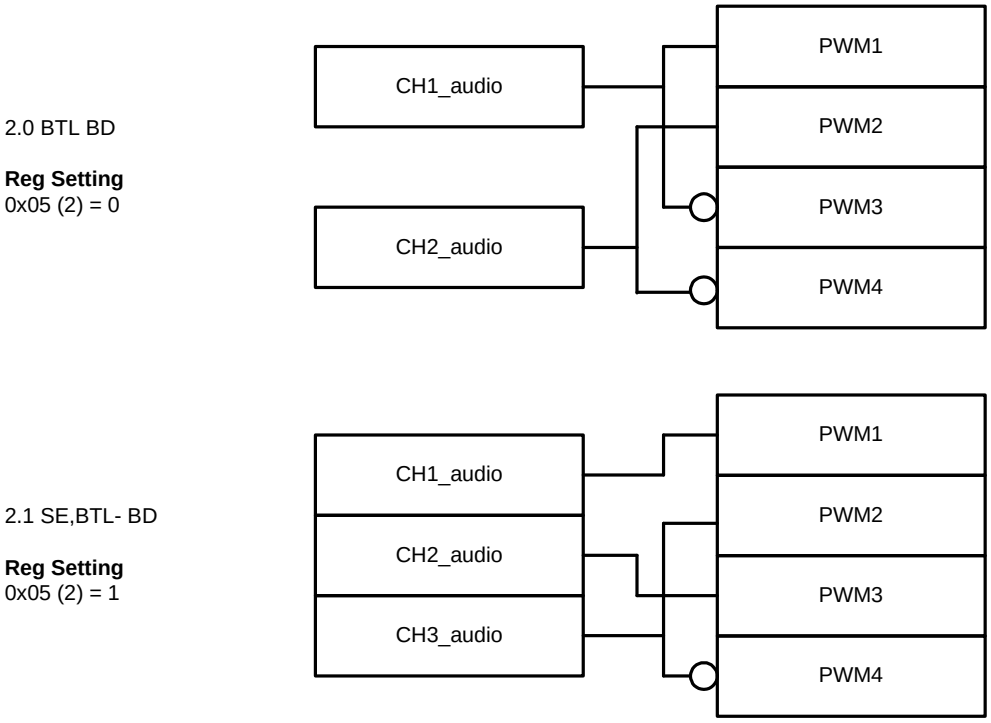


Figure 21. Output Mode and MUX Selection

Function Description (Cont.)

2.1-Mode Support

The APA3169 supports 2.0-mode and 2.1-mode operation.To enable 2.1 mode, register 0x05 bit D2 must be set to 1.

Single-Filter PBTL-Mode Support

The APA3169 supports parallel BTL (PBTL) mode with OUT_A/OUT_B (and OUT_C/OUT_D) connected before the LC filter. In order to put the part in PBTL configuration, drive PBTL (pin 8) HIGH. This synchronizes the turnoff of half-bridges A and B (and similarly C/D) if an overcurrent condition is detected in either half-bridge.

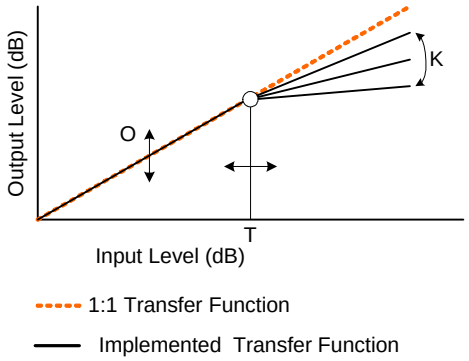
There is a pulldown resistor on the PBTL pin that configures the part in BTL mode if the pin is left floating.

PWM output multiplexers should be updated to set the device in PBTL mode. Output Mux Register (0x25) should be written with a value of 0x01 10 32 45.

Dynamic Range Control (DRC)

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/right channels.

The DRC input/output diagram is shown in Figure 22.



Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

• The DRC has adjustable threshold, offset, and compression levels.

Figure 22. Dynamic Range Control

BiQuad Structure

All biquads use a 2nd order IIR filter structure as shown below. Each biquad has 3 coefficients on the direct path (b0, b1, b2) and 2 coefficients on feedback path (a1 and a2) which is shown in the diagram.

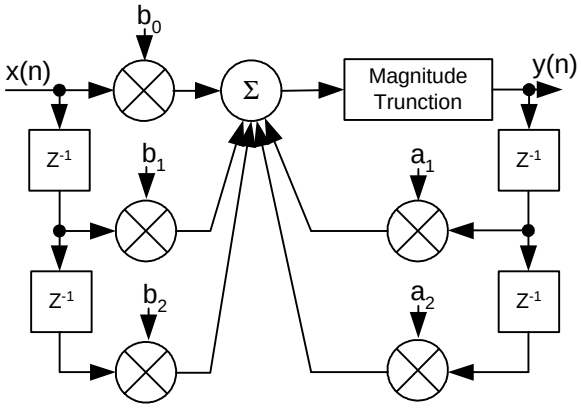


Figure 24. Biquad Filter

Function Description (Cont.)

26Bit 3.23 Number Format

All mixer gain coefficients are 26 bit coefficients and use a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in Figure 18.

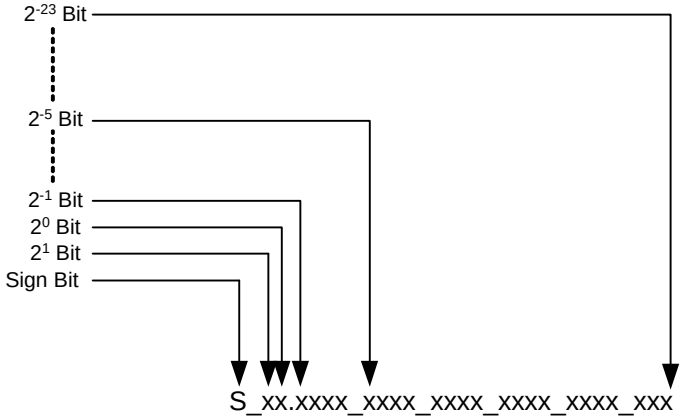


Figure 25. 3.23 Format

The decimal value of a 3.23 format number can be found by following the weighting and is shown in Figure 25. If the MSB is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the MSB is a logic 1, and then the number is a negative number. In this case, every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 26 applied to obtain the magnitude of the negative number.

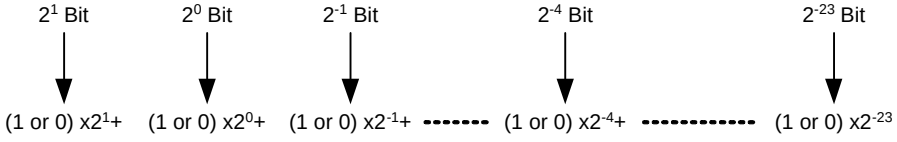


Figure 26. Conversion Weighting Facroes 3.23 Format to Floating Point

Gain coefficients, entered via the I²C bus, must be entered as 32 bit binary numbers. The format of the 32 bit number (4 byte or 8 digit hexadecimal number) is shown in Figure 27.

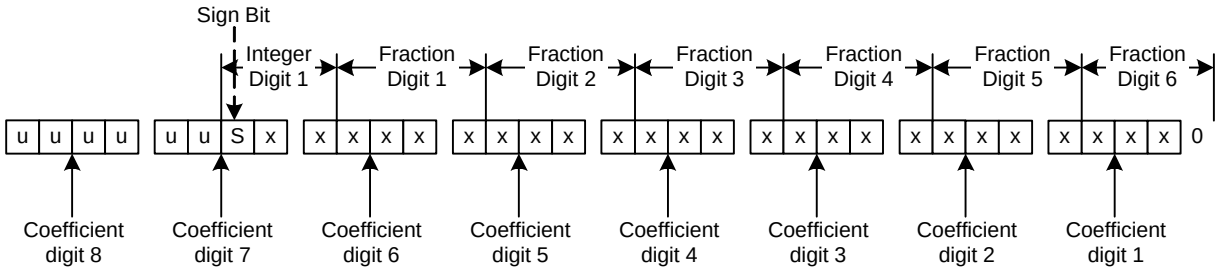


Figure 27. Alignment of 3.23 Coefficient in 32Bit I²C Word

Function Description (Cont.)

Sample Calculation for 3.23 Format

dB	Linear	Decimal	Hex (3.23 Format)
0	1	8388608	00800000
5	1.7782794	14917288	00E39EA8
-5	0.5623413	4717260	0047FACC
X	$L = 10^{(X/20)}$	D = 8388608 × L	H = dec2hex (D, 8)

Sample Calculation for 9.17 Format

dB	Linear	Decimal	Hex (9.17 Format)
0	1	131072	00020000
5	1.7782794	233082.6	00038E7A
-5	0.5623413	73707.2	00011FEB
X	$L = 10^{(X/20)}$	D = 131072 × L	H = dec2hex (D, 8)

Recommended Use Model

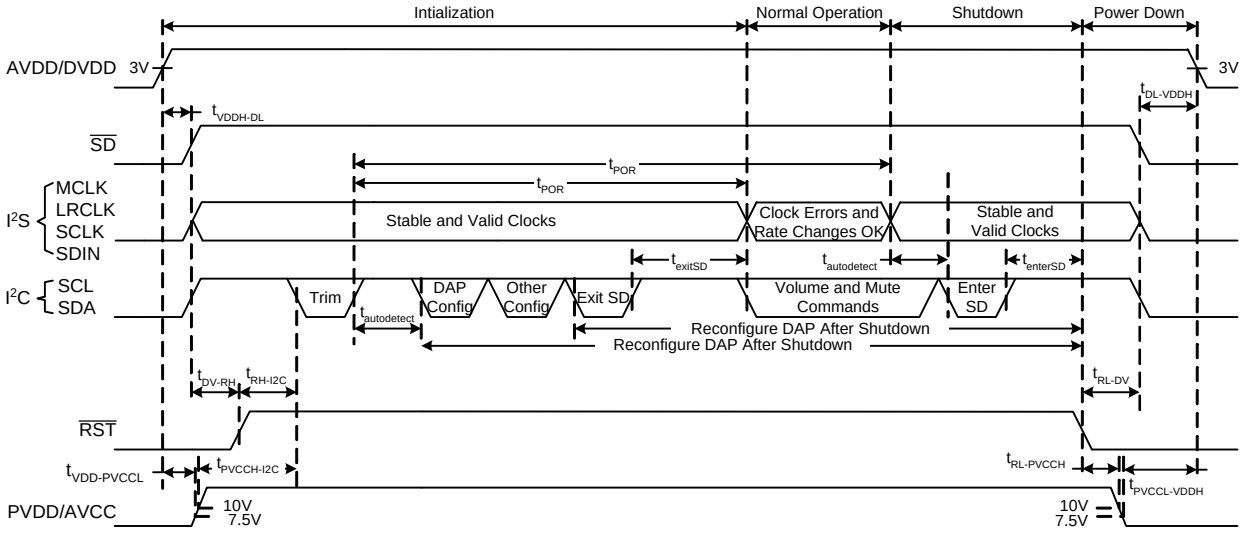


Figure 28. Recommended Command Sequence

Function Description (Cont.)

Recommended Use Model (Cont.)

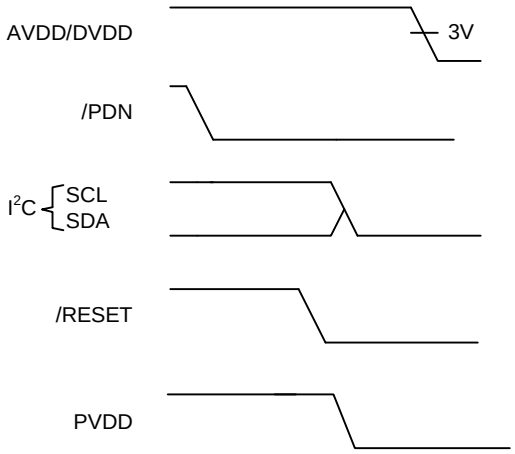


Figure 29. Power Loss Sequence

Recommended Command Sequences

The DAP has two groups of commands. One set is for configuration and is intended for use only during initialization. The other set has built-in click and pop protection and may be used during normal operation while audio is streaming. The following supported command sequences illustrate how to initialize, operate, and shutdown the device.

Initialization Sequence

Use the following sequence to power-up and initialize the device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3V.
2. Initialize digital inputs and PVDD supply as follows:
   - Drive $\overline{\text{RESET}}$=0, $\overline{\text{PDN}}$=1, and other digital inputs to their desired state while ensuring that all are never more than 2.5V above AVDD/DVDD. Drive $\overline{\text{RESET}}$ =1.
   - Ramp up PVDD to at least 8V.
3. Configure the DAP via I^2C.
4. Configure remaining registers.
5. Exit shutdown.

Normal Operation

The following are the only events supported during normal operation:

(a) Writes to master/channel volume registers

(b) Writes to soft mute register

(c) Enter and exit shutdown

Function Description (Cont.)

Shutdown Sequence

Enter:

1. Write 0x40 to register 0x05.
2. If desired, reconfigure by returning to step 4 of initialization sequence.

Exit:

1. Write 0x00 to register 0x05.
2. Proceed with normal operation.

Power-down Sequence

Use the following sequence to power-down the device and its supplies:

1. If time permits, enter shutdown ; else, in case of sudden power loss, assert $\overline{PDN}$=0.
2. Assert $\overline{RESET}$=0.
3. Drive digital inputs low and ramp down PVDD supply as follows:
   - Drive all digital inputs low after $\overline{RESET}$ has been low.
   - Ramp down PVDD while ensuring that it remains above 8V until $\overline{RESET}$ has been low.
4. Ramp down AVDD/DVDD while ensuring that it remains above 3V until PVDD is below 6V and that it is never more than 2.5V below the digital inputs.

Table 1. Serial Control Interface Register Summary

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
			A u indicates unused bits.	
0x00	Clock control register	1	Description shown in subsequent section	0x6C
0x01	Device ID register	1	Description shown in subsequent section	0x69
0x02	Error status register	1	Description shown in subsequent section	0x00
0x03	System control register 1	1	Description shown in subsequent section	0x80
0x04	Serial data interface	1	Description shown in subsequent section	0x05
0x05		1	Description shown in subsequent section	0x4C
0x06	Soft mute register	1	Description shown in subsequent section	0x00
0x07	Master volume	1	Description shown in subsequent section	0xFF (mute)
0x08	Channel 1 vol	1	Description shown in subsequent section	0x30 (0dB)
0x09	Channel 2 vol	1	Description shown in subsequent section	0x30 (0dB)
0x0A	Channel 3 vol	1	Description shown in subsequent section	0x30 (0dB)
0x0B - 0X0D			Reserved (1)	
0x0E	Volume configuration register	1	Description shown in subsequent section	0x91
0x0F		1	Reserved(1)	
0x10	Modulation limit register	1	Description shown in subsequent section	0x02
0x11-0x19		1	Reserved(1)	
0x1A	Start/stop period register	1	Description shown in subsequent section	0x0F
0x1B-0x1F		1	Reserved(1)	
0x20	Input MUX register	4	Description shown in subsequent section	0x0089 7772
0x21	CH4 Source select register	4	Description shown in subsequent section	0x0000 4303
0x22-0x24		1	Reserved(1)	

Function Description (Cont.)

Table 1. Serial Control Interface Register Summary (Cont.)

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
0x25	PWM output MUX register	4	Description shown in subsequent section	0x0102 1345
0x26-0x28		4	Reserved(1)	
0x29	ch1_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2A	ch1_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2B	ch1_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2C	ch1_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2D	ch1_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2E	ch1_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2F	ch1_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Function Description (Cont.)

Table 1. Serial Control Interface Register Summary (Cont.)

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
0x30	ch2_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x31	ch2_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x32	ch2_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x33	ch2_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x34	ch2_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x35	ch2_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x36	ch2_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Function Description (Cont.)

Table 1. Serial Control Interface Register Summary (Cont.)

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
0x37~ 0x3F			Reserved(1)	
0x40	DRC1-T	4	T[31:0] (9.23 format)	0x007F FFFF
0x41	DRC1-K	4	u[31:26], K[25:0]	0x0080 0000
0x42	DRC1-O	4	u[31:26], O[25:0]	0x0080 0000
0x43	DRC2-T	4	T[31:0] (9.23 format)	0x007F FFFF
0x44	DRC2-K	4	u[31:26], K[25:0]	0x0080 0000
0x45	DRC2-O	4	u[31:26], O[25:0]	0x0080 0000
0x46	DRC control	4	Description shown in subsequent section	0x0000 0000
0x47–0x4F			Reserved(1)	
0x50	EQ Control	4	Description shown in subsequent section	0x0000 0000
0x51	Ch1 output mixer	12	ch1_output_mixer2	0x0707 0707
			ch1_output_mixer1	0x0707 0707
			ch1_output_mixer0	0x0707 0707
0x52	Ch2 output mixer	12	ch2_output_mixer2	0x0707 0707
			ch2_output_mixer1	0x0707 0707
			ch2_output_mixer0	0x0707 0707
0x53	Ch1 input mixer	16	ch1_input_mixer3	0x0808 0808
			ch1_input_mixer2	0x0808 0808
			ch1_input_mixer1	0x0808 0808
			ch1_input_mixer0	0x0808 0808
0x54	Ch2 input mixer	16	ch2_input_mixer3	0x0808 0808
			ch2_input_mixer2	0x0808 0808
			ch2_input_mixer1	0x0808 0808
			ch2_input_mixer0	0x0808 0808
0x55	Ch3 input mixer	12	ch3_input_mixer2	0x0707 0707
			ch3_input_mixer1	0x0707 0707
			ch3_input_mixer0	0x0707 0707
0x56	Output Post scale	4	9.17 format	0x0002 0000
0x57	Input Pre scale	4	Description shown in subsequent section	0x0080 0000
0x58	ch1_bq[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Function Description (Cont.)

Table 1. Serial Control Interface Register Summary (Cont.)

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
0x59	ch1_bq[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5A	subchannel bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5B	subchannel bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5C	ch2_bq[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5D	ch2_bq[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5E	pseudo_ch2_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Function Description (Cont.)

Table 1. Serial Control Interface Register Summary (Cont.)

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
0x5F	pseudo_ch2_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x60	Ch4 output mixer	8	ch4_output_mixer1	0x0000 0000
			ch4_output_mixer0	0x0080 0000
0x61	Ch4 input mixer	8	ch4_input_mixer1	0x0040 0000
			ch4_input_mixer0	0x0040 0000
0x62-0xF0			Reserved(1)	

Note (1): Reserved register should not be accessed

All DAP coefficients are 3.23 format unless specified otherwise.

Clock Control Register (0x00)

The clocks and data rates are automatically determined by the APA3169. The clock control register contains the auto-detected clock status. Bits D7-D5 reflect the sample rate. Bits D4-D2 reflect the MCLK frequency.

Table 2. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	-	-	-	-	-	f_S=32kHz sample rate
0	0	1	-	-	-	-	-	f_S=88.2/96kHz sample rate
0	1	0	-	-	-	-	-	f_S=176.4/192kHz sample rate
0	1	1	-	-	-	-	-	f_S=44.1/48kHz sample rate (2)
1	0	0	-	-	-	-	-	Reserved(1)
1	0	1	-	-	-	-	-	Reserved(1)
1	1	0	-	-	-	-	-	Reserved(1)
1	1	1	-	-	-	-	-	Reserved(1)
-	-	-	0	0	0	-	-	MCLK frequency=64xf_S (3)
-	-	-	0	0	1	-	-	MCLK frequency=128xf_S (3)
-	-	-	0	1	0	-	-	MCLK frequency=192xf_S (4)
-	-	-	0	1	1	-	-	MCLK frequency=256xf_S (2)
-	-	-	1	0	0	-	-	MCLK frequency=384xf_S
-	-	-	1	0	1	-	-	MCLK frequency=512xf_S
-	-	-	1	1	0	-	-	Reserved (1)
-	-	-	1	1	1	-	-	Reserved (1)
-	-	-	-	-	-	0	-	Reserved (1)
-	-	-	-	-	-	-	0	Reserved (1)

Note (1): Reserved registers should not be accessed.

Note (2): Default values are in bold

Note (3): Only available for 44.1kHz and 48kHz rates.

Note (4): Rate only available for 32/44.1/48kHz sample rates.

Function Description (Cont.)

Device Id Register (0x01)

The Anpec ID register contains the ID code for the firmware revision.

Table 3. General Status Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	1	1	0	1	0	0	1	Identification code

Error Status Register (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error Definitions:

MCLK Error : MCLK frequency is changing. The number of MCLKs per LRCLK is changing.

SCLK Error: The number of SCLKs per LRCLK is changing.

LRCLK Error: LRCLK frequency is changing.

Table 4. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	-	-	-	-	-	-	-	MCLK error
-	1	-	-	-	-	-	-	PLL auto clock error
-	-	1	-	-	-	-	-	SCLK error
-	-	-	1	-	-	-	-	LRCLK error
-	-	-	-	0	-	-	-	Reserved
-	-	-	-	-	0	-	-	Reserved
-	-	-	-	-	-	1	-	Over Current, Over Temperature, Over Voltage or Under Voltage errors
-	-	-	-	-	-	-	1	Over temperature warning (sets around 150^{O}C)
0	0	0	0	0	0	0	0	No errors

Note: Default values are in bold.

System Control Register 1 (0x03)

The system control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled. If 1, the dc-blocking filter (-3dB cutoff < 1Hz) for each channel is enabled (default).

Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes same time as volume ramp defined in reg 0x0E.

If 1, use hard unmute on recovery from clock error (default). This is a fast recovery, a single step volume ramp

Bits D1-D0: Select de-emphasis.

Table 5. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	-	-	-	-	-	-	-	PWM high-pass (dc blocking) disenabled
1	-	-	-	-	-	-	-	PWM high-pass (dc blocking) enabled
-	0	0	0	0	0	-	-	Reserved
-	-	-	-	-	-	0	0	No de-emphasis
-	-	-	-	-	-	0	1	De-emphasis for f_S=32kHz

Function Description (Cont.)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	-	-	-	1	0	De-emphasis for f_S=44.1kHz
-	-	-	-	-	-	1	1	De-emphasis for f_S=48kHz

Note: Default values are in bold.

Serial Data Interface Register (0x04)

As shown in Table 6, the APA3169 supports 9 serial data modes. The default is 24bit, I^2S mode.

Table 6. Serial Data Interface Control Register (0x04) Format

D7	D6	D5	D4	D3	D2	D1	D0	Word Length	Receive Serial Data Interface Format
0	0	0	0	-	-	-	-		Reserved
-	-	-	-	0	0	0	0	16	Right-justified
-	-	-	-	0	0	0	1	20	Right-justified
-	-	-	-	0	0	1	0	24	Right-justified
-	-	-	-	0	0	1	1	16	I^2S
-	-	-	-	0	1	0	0	20	I^2S
-	-	-	-	0	1	0	0	24	I^2S
-	-	-	-	0	1	1	0	16	Left-justified
-	-	-	-	0		1	1	20	Left-justified
				1	0	0	0	24	Left-justified
-	-	-	-	1	0	0	1		Reserved
-	-	-	-	1	0	1	0		Reserved
-	-	-	-	1	0	1	1		Reserved
-	-	-	-	1	1	0	0		Reserved
-	-	-	-	1	1	0	1		Reserved
-	-	-	-	1	1	1	0		Reserved
-	-	-	-	1	1	1	1		Reserved

Note: Default values are in bold.

System Control Register 2 (0x05)

When bit D6 is set low, the system exits all channel shutdown and starts playing audio; otherwise, the outputs are shut down (hard mute).

Table 7. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	-	-	-	-	-	-	-	Reserved
-	1	-	-	-	-	-	-	Enter all channel shut down (hard mute)
-	0	-	-	-	-	-	-	Exit all channel shut down (Normal operation)
-	-	0	0	1	-	-	-	Reserved
-	-	-	-	-	0	-	-	2.0 mode (2 BTL)
-	-	-	-	-	1	-	-	2.1 mode (2 SE + 1 BTL)

Function Description (Cont.)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	-	-	-	0	-	A_SEL configured as input
-	-	-	-	-	-	1	-	A_SEL configured as $\overline{\text{FAULT}}$ output
-	-	-	-	-	-	-	0	Reserved

Note: Default values are in bold.

Soft Mute Register (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

Table 8. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	-	-	-	Reserved
-	-	-	-	-	1	-	-	Soft mute channel 3
-	-	-	-	-	0	-	-	Soft un-mute channel 3
-	-	-	-	-	-	1	-	Soft mute channel 2
-	-	-	-	-	-	0	-	Soft un-mute channel 2
-	-	-	-	-	-	-	1	Soft mute channel 1
-	-	-	-	-	-	-	0	Soft un-mute channel 1

Note: Default values are in bold.

Volume Registers (0x07, 0x08, 0x09)

Step size is 0.5 dB.
Master volume - 0x07 (default is mute)
Channel-1 volume - 0x08 (default is 0 dB)
Channel-2 volume - 0x09 (default is 0 dB)
Channel-3 volume - 0x0A (default is 0 dB)

Table 9. Volume Registers (0x07, 0x08, 0x09)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	24dB
0	0	1	1	0	0	0	0	0dB
1	1	1	1	1	1	1	0	-103dB
1	1	1	1	1	1	1	1	MUTE (default for master volume)

Note: Default values are in bold.

Volume Configuration Register (0x0E)

Bits Volume slew rate (Used to control volume change and MUTE ramp rates). These bits control the D2-D0: number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I²S data as follows.

Sample Rate (kHz)	Approximate Ramp Rate
8/16/32	125µs/step
11.025/22.05/44.1	90.7µs/step
12/24/48	83.3µs/step

Function Description (Cont.)

Table 10. Volume Control Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	-	-	1	0	-	-	-	Reserved
	0							Subchannel (ch4) volume = ch1 volume (default)
	1							Subchannel volume = register 0x.A
		0						Ch3 volume = ch2_volume (default)
		1						Ch3 volume = register 0x.A
-	-	-	-	-	0	0	0	Volume slew 512 steps (43ms volume ramp time at 48kHz)
-	-	-	-	-	0	0	1	Volume slew 1024 steps (43ms volume ramp time at 48kHz)
-	-	-	-	-	0	1	0	Volume slew 2048 steps (43ms volume ramp time at 48kHz)
-	-	-	-	-	0	1	1	Volume slew 256 steps (43ms volume ramp time at 48kHz)
-	-	-	-	-	1	0	0	Reserved
					1	0	1	Reserved
					1	1	0	Reserved
					1	1	1	Volume slew 0 step (Disable)

Note: Default values are in bold.

Modulation Limit Register (0x10)

The modulation limit is the maximum duty cycle of the PWM output waveform.

Table 11. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	MODULATION LIMIT
0	0	0	0	0	–	–	–	Reserved
-	-	-	-	-	0	0	0	Reserved
-	-	-	-	-	0	0	1	98.4%
-	-	-	-	-	0	1	0	97.7%
-	-	-	-	-	1	0	0	96.9%
-	-	-	-	-	0	1	1	96.1%
-	-	-	-	-	1	0	1	95.3%
-	-	-	-	-	1	1	0	94.5%
-	-	-	-	-	1	1	1	93.8%

Note: Default values are in bold.

Start/Stop Period Register (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all channel shut down command or change in the $\overline{PDN}$ state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I^2S clock stability.

Table 12. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	-	-	-	-	-	Reserved
-	-	-	0	0	-	-	-	No 50% duty cycle start/stop period
-	-	-	0	1	0	0	0	16.5ms 50% duty cycle start/stop period

Function Description (Cont.)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	0	1	0	0	1	23.9ms 50% duty cycle start/stop period
-	-	-	0	1	0	1	0	31.4ms 50% duty cycle start/stop period
-	-	-	0	1	0	1	1	40.4ms 50% duty cycle start/stop period
-	-	-	0	1	1	0	0	53.9ms 50% duty cycle start/stop period
-	-	-	0	1	1	0	1	70.3ms 50% duty cycle start/stop period
-	-	-	0	1	1	1	0	94.2ms 50% duty cycle start/stop period
-	-	-	0	1	1	1	1	125.7ms 50% duty cycle start/stop period
-	-	-	1	0	0	0	0	164.6ms 50% duty cycle start/stop period
-	-	-	1	0	0	0	1	239.4ms 50% duty cycle start/stop period
-	-	-	1	0	0	1	0	314.2ms 50% duty cycle start/stop period
-	-	-	1	0	0	1	1	403.9ms 50% duty cycle start/stop period
-	-	-	1	0	1	0	0	538.6ms 50% duty cycle start/stop period
-	-	-	1	0	1	0	1	703.4ms 50% duty cycle start/stop period
-	-	-	1	0	1	1	0	942.5ms 50% duty cycle start/stop period
-	-	-	1	0	1	1	1	1256.6ms 50% duty cycle start/stop period
-	-	-	1	1	0	0	0	1728.1ms 50% duty cycle start/stop period
-	-	-	1	1	0	0	1	2513.6ms 50% duty cycle start/stop period
-	-	-	1	1	0	1	0	3299.1ms 50% duty cycle start/stop period
-	-	-	1	1	0	1	1	4241.7ms 50% duty cycle start/stop period
-	-	-	1	1	1	0	0	5655.6ms 50% duty cycle start/stop period
-	-	-	1	1	1	0	1	7383.7ms 50% duty cycle start/stop period
-	-	-	1	1	1	1	0	9897.3ms 50% duty cycle start/stop period
-	-	-	1	1	1	1	0	13196.4ms 50% duty cycle start/stop period

Note: Default values are in bold.

Input Multiplexer Register (0x20)

This register controls the routing of I²S audio to the internal channels.

Table 13. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
1	-	-	-	-	-	-	-	Reserved
-	0	0	0	-	-	-	-	SDIN-L to Channel 1
-	0	0	1	-	-	-	-	SDIN-R to Channel 1
-	0	1	0	-	-	-	-	Reserved
-	0	1	1	-	-	-	-	Reserved
-	1	0	0	-	-	-	-	Reserved
-	1	0	1	-	-	-	-	Reserved
-	1	1	0	-	-	-	-	Ground (0) to channel 1

Function Description (Cont.)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
-	1	1	1	-	-	-	-	Reserved
-	-	-	-	1	-	-	-	Reserved
-	-	-	-	-	0	0	0	SDIN-L to Channel 2
-	-	-	-	-	0	0	1	SDIN-R to Channel 2
-	-	-	-	-	0	1	0	Reserved
-	-	-	-	-	0	1	1	Reserved
-	-	-	-	-	1	0	0	Reserved
-	-	-	-	-	1	0	1	Reserved
-	-	-	-	-	1	1	0	Ground (0) to channel 2
-	-	-	-	-	1	1	1	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	1	1	1	0	1	1	1	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	1	1	1	0	0	1	0	Reserved

Note: Default values are in bold.

CHANNEL 4 SOURCE SELECT REGISTER (0x21)

This register selects the channel 4 source.

Table 14. Subchannel Control Register (0x21)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	0	0	0	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	1	0	0	0	0	1	1	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	1	1	Reserved

Note: Default values are in bold.

Pwm Output Mux Register (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21-D20: Selects which PWM channel is output to OUT_A

Bits D17-D16: Selects which PWM channel is output to OUT_B

Bits D13-D12: Selects which PWM channel is output to OUT_C

Bits D09-D08: Selects which PWM channel is output to OUT_D

Note that channels are enclosed so that channel 1=0x00, channel 2=0x01, channel 1=0x02, and channel 2=0x03.

Function Description (Cont.)

Table 15. PWM Output Mux Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	-	-	-	-	-	-	Reserved
-	-	0	0	-	-	-	-	Multiplex channel 1 to OUT_A
-	-	0	1	-	-	-	-	Multiplex channel 2 to OUT_A
-	-	1	0	-	-	-	-	Multiplex $\overline{\text{channel 1}}$ to OUT_A
-	-	1	1	-	-	-	-	Multiplex $\overline{\text{channel 2}}$ to OUT_A
-	-	-	-	0	0	-	-	Reserved
-	-	-	-	-	-	0	0	Multiplex channel 1 to OUT_B
-	-	-	-	-	-	0	1	Multiplex channel 2 to OUT_B
-	-	-	-	-	-	1	0	Multiplex $\overline{\text{channel 1}}$ to OUT_B
-	-	-	-	-	-	1	1	Multiplex $\overline{\text{channel 2}}$ to OUT_B
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	0	-	-	-	-	-	-	Reserved
-	-	0	0	-	-	-	-	Multiplex channel 1 to OUT_C
-	-	0	1	-	-	-	-	Multiplex channel 2 to OUT_C
-	-	1	0	-	-	-	-	Multiplex $\overline{\text{channel 1}}$ to OUT_C
-	-	1	1	-	-	-	-	Multiplex $\overline{\text{channel 2}}$ to OUT_C
-	-	-	-	0	0	-	-	Reserved
-	-	-	-	-	-	0	0	Multiplex channel 1 to OUT_D
-	-	-	-	-	-	0	1	Multiplex channel 2 to OUT_D
-	-	-	-	-	-	1	0	Multiplex $\overline{\text{channel 1}}$ to OUT_D
-	-	-	-	-	-	1	1	Multiplex $\overline{\text{channel 2}}$ to OUT_D
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	1	0	0	0	1	0	1	Reserved

Note: Default values are in bold.

DRC Control (0x46)

Each DRC can be enabled independently using the DRC control register. The DRCs are disabled by default.

Table 16. DRC Control Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	0	0	0	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	0	0	0	0	0	0	0	Reserved

Function Description (Cont.)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	-	-	Reserved
-	-	-	-	-	-	0	-	DRC2 turned OFF
-	-	-	-	-	-	1	-	DRC2 turned ON
-	-	-	-	-	-	-	0	DRC1 turned OFF
-	-	-	-	-	-	-	1	DRC1 turned ON

Note: Default values are in bold.

EQ Control (0x50)

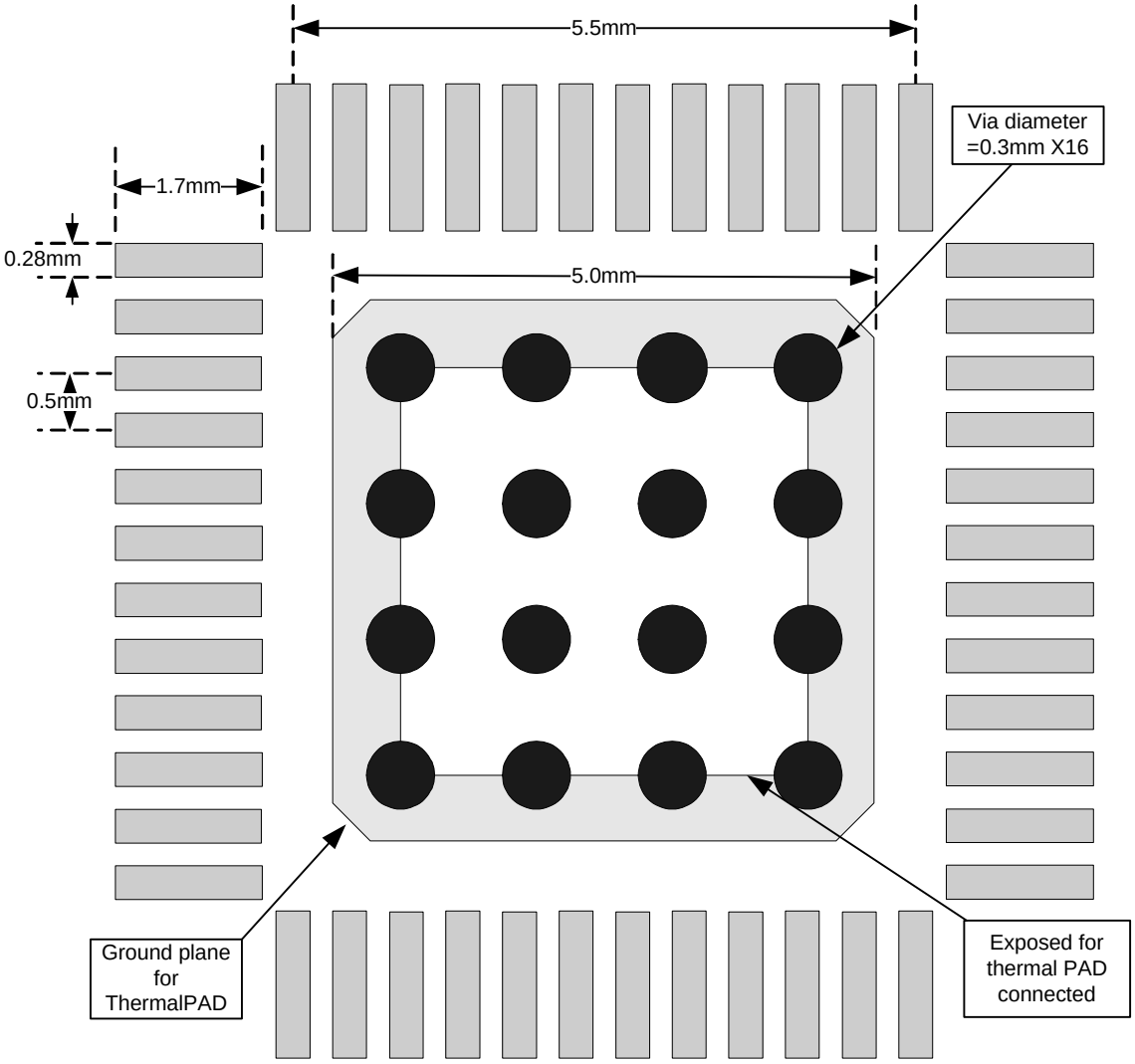
Table 1. EQ Control Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	0	0	0	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	0	0	0	0	0	0	0	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	-	-	-	-	-	-	-	EQ ON
1	-	-	-	-	-	-	-	EQ OFF
-	0	0	0	0	0	0	0	Reserved

Note: Default values are in bold.

Application Information

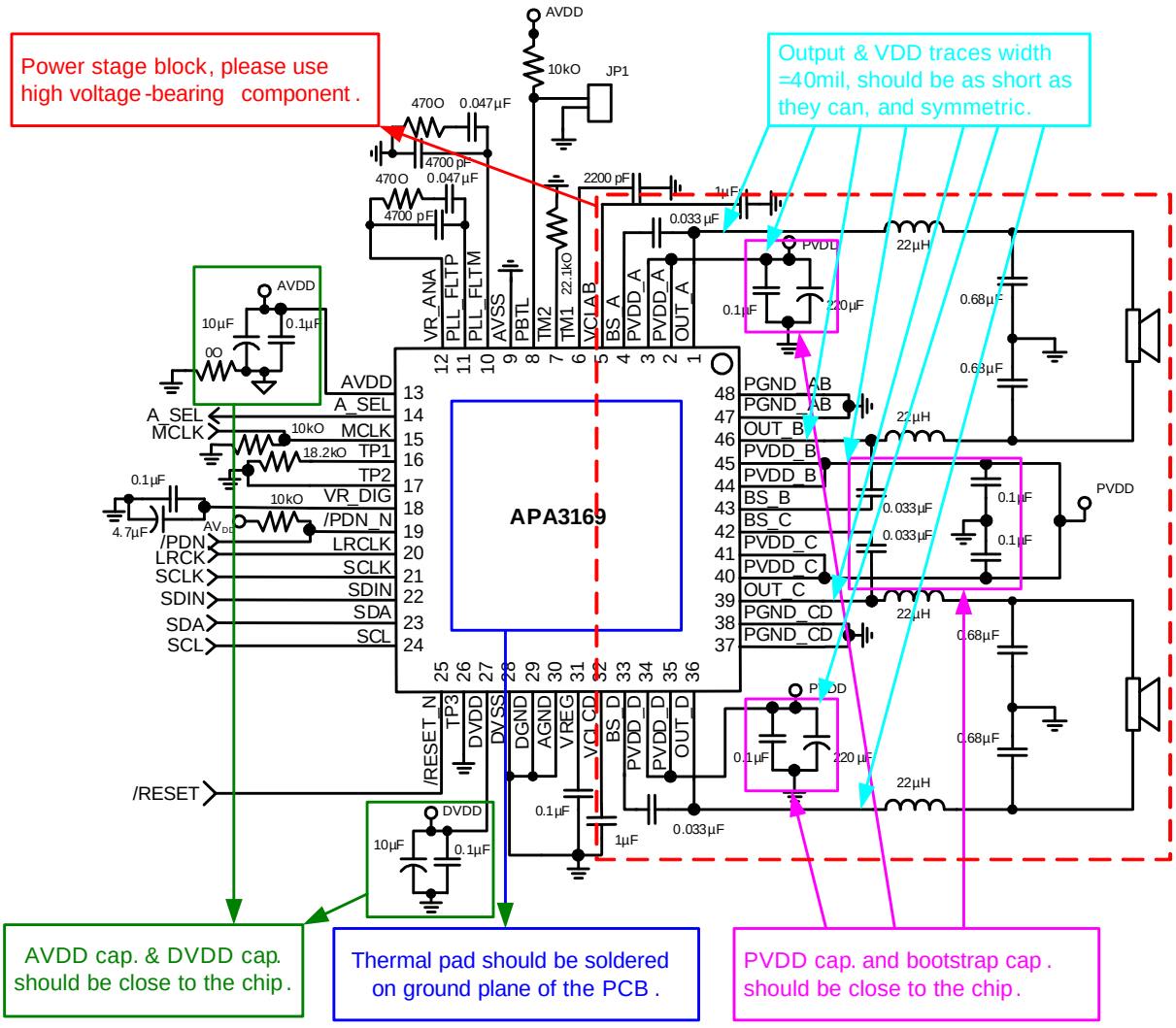
Land Pattern Recommendation



TQFP7X7-48 Land Pattern Recommendation

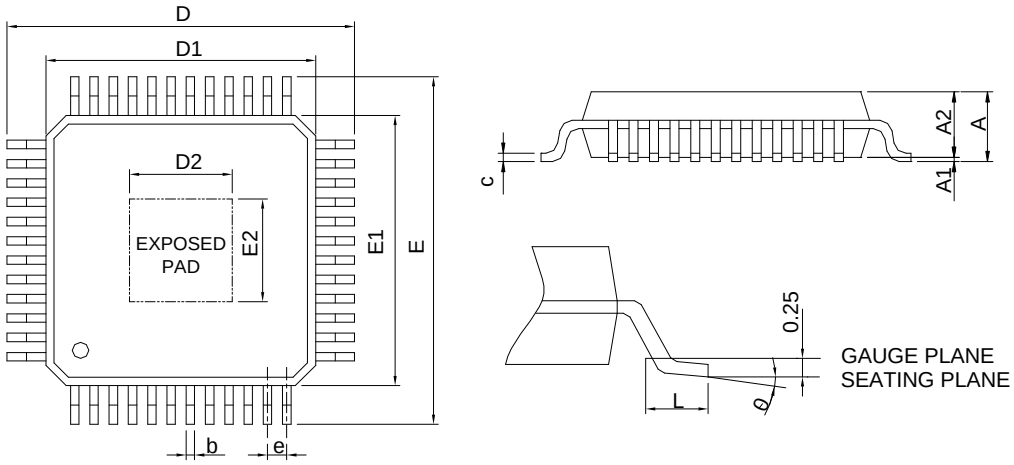
Application Information (Cont.)

Layout Recommendation



Package Information

TQFP7x7-48P

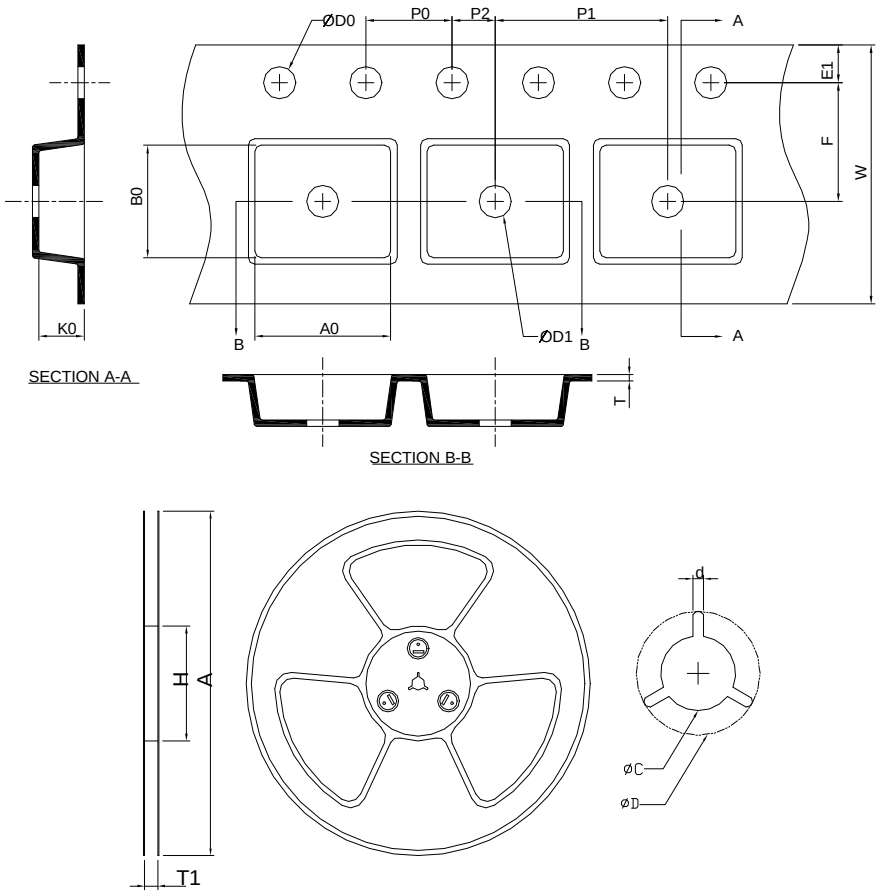


SYMBOL	TQFP7x7-48P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.95	1.05	0.037	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
D	8.80	9.20	0.346	0.362
D1	6.90	7.10	0.272	0.280
D2	3.00	5.50	0.118	0.177
E	8.80	9.20	0.346	0.362
E1	6.90	7.10	0.272	0.280
E2	3.00	5.50	0.118	0.177
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030
	0^o	7^o	0^o	7^o

Note : 1. Followed from JEDEC MS-026 ABC.

2. Dimension "D1" and "E1" do not include mold protrusions. Allowable protrusions is 0.25 mm per side. "D1" and "E1" are maximun plasticbody size dimensions including mold mismatch.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFP7x7-48P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	9.4±0.20	9.4±0.20	1.8±0.20

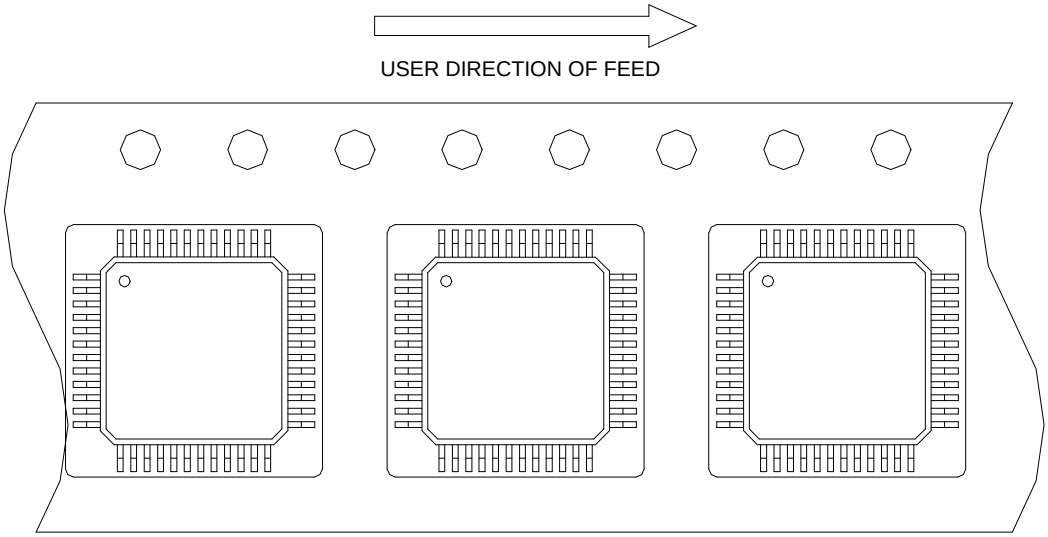
(mm)

Devices Per Unit

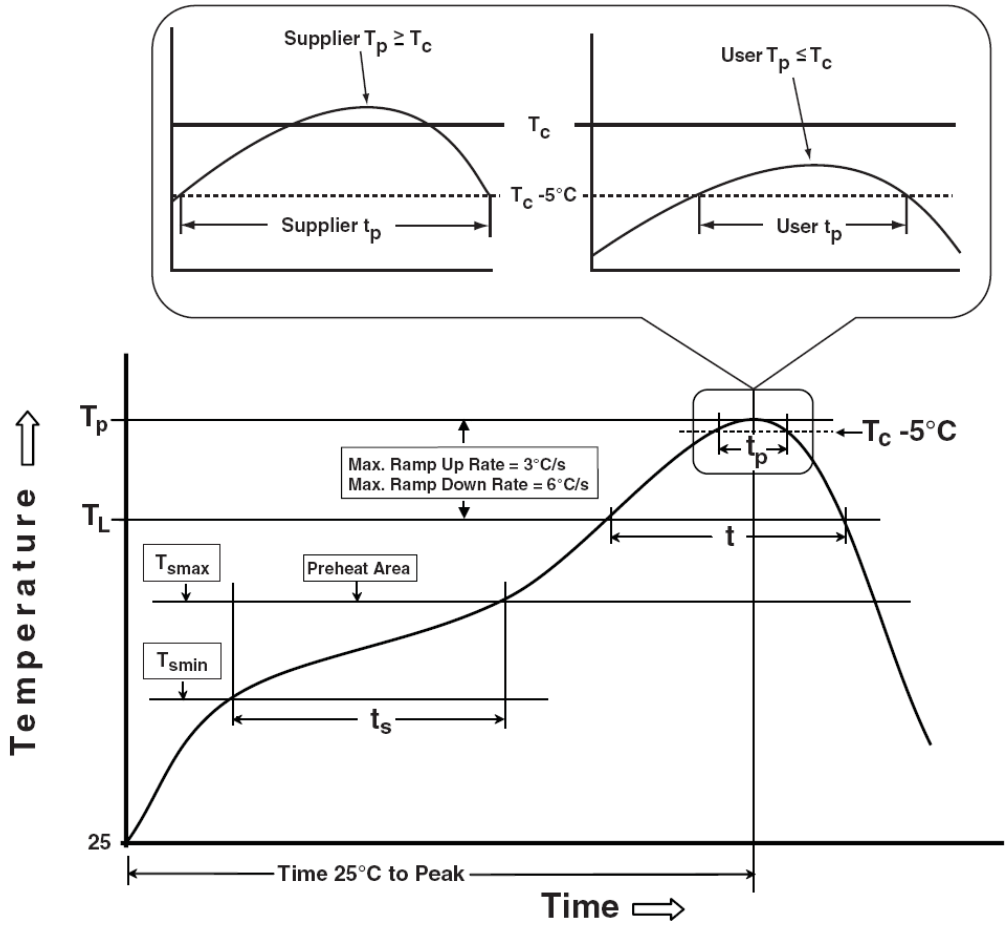
Package Type	Unit	Quantity
TQFP7x7-48P	Tape & Reel	2500

Taping Direction Information

TQFP7x7-48P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

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