SONY

High Power SP5T Antenna Switch MMIC for GSM/UMTS Dual Mode

CXG1195XR

Description

The CXG1195XR is a SP5T antenna switch for GSM/UMTS applications. The low insertion loss on transmit means increased talk time as the Tx power amplifier can be operated at a lower output level. On chip logic reduces component count and simplifies PCB layout by allowing direct connection of the switch to digital base band control lines with the CMOS logic levels. It requires 3 CMOS control lines. The Sony GaAs JPHEMT MMIC process is used for low insertion loss.
(Applications: GSM/UMTS dual mode handsets)

Features

◆ Insertion loss (Tx) : 0.40dB (Typ.) at 34dBm (GSM900)
0.50dB (Typ.) at 32dBm (GSM1800)
0.50dB (Typ.) at 29dBm (UMTS2100)

Package

Small and low height package size: 20-pin XQFN (2.7mm × 2.7mm × 0.35mm (Typ.))

Structure

GaAs JPHEMT MMIC

This IC is ESD sensitive device. Special handling precautions are required.

Absolute Maximum Ratings

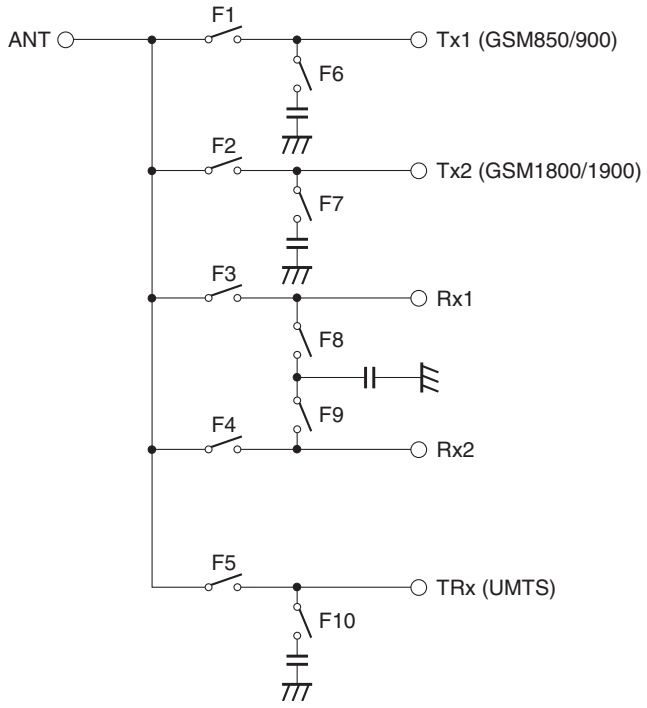
(Ta = 25℃)

◆ Bias voltage	V_{DD}	7	V	
◆ Control voltage	Vctl	5	V	
◆ Input power max. [Tx1]		35	dBm	(Duty cycle = 12.5 to 50%)
◆ Input power max. [Tx2]		33	dBm	(Duty cycle = 12.5 to 50%)
◆ Input power max. [TRx]		32	dBm	
◆ Input power max. [all_Rx]		13	dBm	
◆ Operating temparature	Topr	–35 to +85	℃	
◆ Storage temperature	Tstg	–65 to +150	℃	
◆ Maximum power dissipation	PD	750	mW	

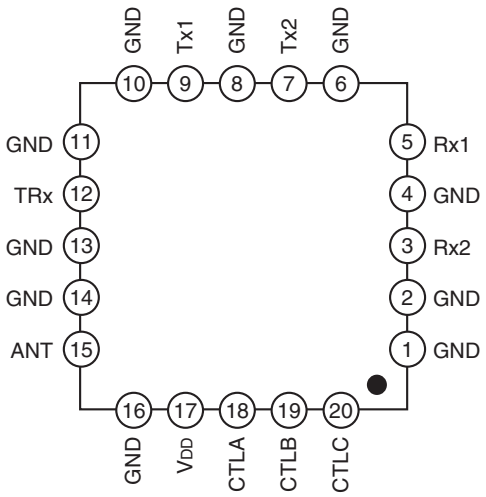
・Copper-clad lamination of glass board (4 layers) : 30mm square, t = 0.8mm, FR-4.

Note) Use this product without exceeding the PD value specified in this specification.
If it is used with exceeding the PD value even for a moment, the heat generated by the operation may cause the degradation or breakdown of the product.

Block Diagram



Pin Configuration



Truth Table

State	ON Path	CTLA	CTLB	CTLC	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
1	ANT – Tx1	H	H	L	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON
2	ANT – Tx2	H	L	L	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON
3	ANT – Rx1	L	L/H	L	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON
4	ANT – Rx2	L	L/H	H	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON
5	ANT – TRx	H	L	H	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Tx1 – ANT	*1	—	0.35	0.50	dB
		Tx2 – ANT	*2	—	0.45	0.60	dB
		TRx (Tx) – ANT	*3	—	0.45	0.60	dB
		ANT – Rx1	*4	—	0.5	0.65	dB
		ANT – Rx2	*5	—	0.65	0.80	dB
		ANT – TRx (Rx)	*6	—	0.5	0.65	dB
Isolation	ISO.	Active path: Tx1					
		ANT – Rx1	*1	25		—	dB
		ANT – Rx2		25		—	dB
		ANT – Tx2		25		—	dB
			1760 to 1830MHz	25		—	dB
		ANT – TRx	*1	25		—	dB
		Active path: Tx2					
		ANT – Rx1	*2	25		—	dB
		ANT – Rx2		25		—	dB
		ANT – TRx		25		—	dB
		Active path: TRx					
		ANT – Rx1	*3	25		—	dB
		ANT – Rx2		25		—	dB
		Tx1 – ANT	*1	25		—	dB
		Tx2 – ANT	*2	25		—	dB
		Active path: Rx1					
		Tx1 – ANT	*1	20		—	dB
		Tx2 – ANT	*2	20		—	dB
		Active path: Rx2					
		Tx1 – ANT	*1	20		—	dB
		Tx2 – ANT	*2	20		—	dB
VSWR	VSWR				1.2		—
Harmonics	2fo	Tx1 – ANT	*1	—	–45	–35	dBm
	3fo			—	–35	–30	dBm
	2fo	Tx2 – ANT	*2	—	–38	–33	dBm
	3fo			—	–33	–30	dBm
	2fo	TRx – ANT	*3	—	–40	–35	dBm
	3fo			—	–35	–30	dBm
Control current	Ictl		Vctl = 2.8V	—	20	50	μA
Supply current	I_{DD}		V_{DD} = 2.8V	—	0.2	0.5	mA
Switching speed	Swt			—	5	10	μs

Note) Electrical Characteristics are measured with all RF ports terminated in 50Ω.

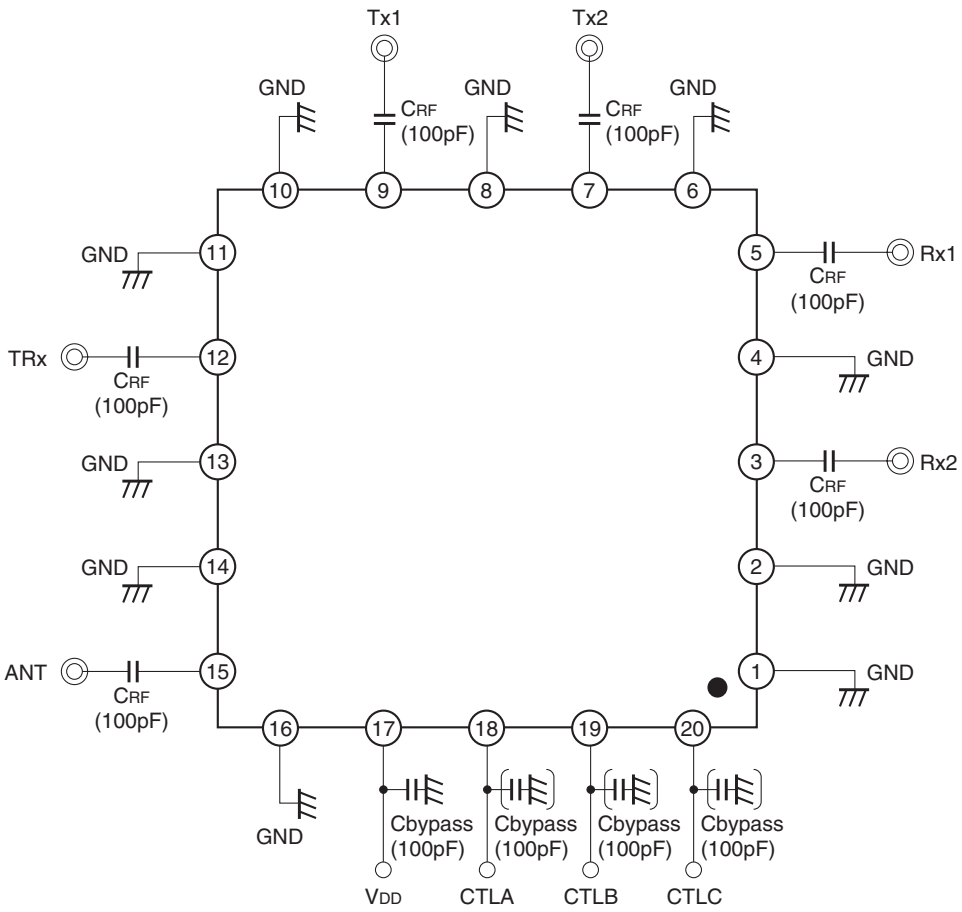
*1 Power incident on Tx1, Pin = +34dBm (CW), 824 to 915MHz, V_{DD} = 2.8V, Tx1 enabled
*2 Power incident on Tx2, Pin = +32dBm (CW), 1710 to 1910MHz, V_{DD} = 2.8V, Tx2 enabled
*3 Power incident on TRx, Pin= +29dBm (CW), 1920 to 1980MHz, V_{DD} = 2.8V, TRx enabled
*4 Power incident on ANT, Pin = –5dBm, 869 to 894MHz, 925 to 960MHz, V_{DD} = 2.8V, Rx1 enabled
*5 Power incident on ANT, Pin = –5dBm, 1805 to 1880MHz, 1930 to 1990MHz, V_{DD} = 2.8V, Rx2 enabled
*6 Power incident on ANT, Pin = –5dBm, 2110 to 2170MHz, V_{DD} = 2.8V, TRx enabled

DC Bias Condition

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.8	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.6	2.8	3.6	V

Recommended Circuit



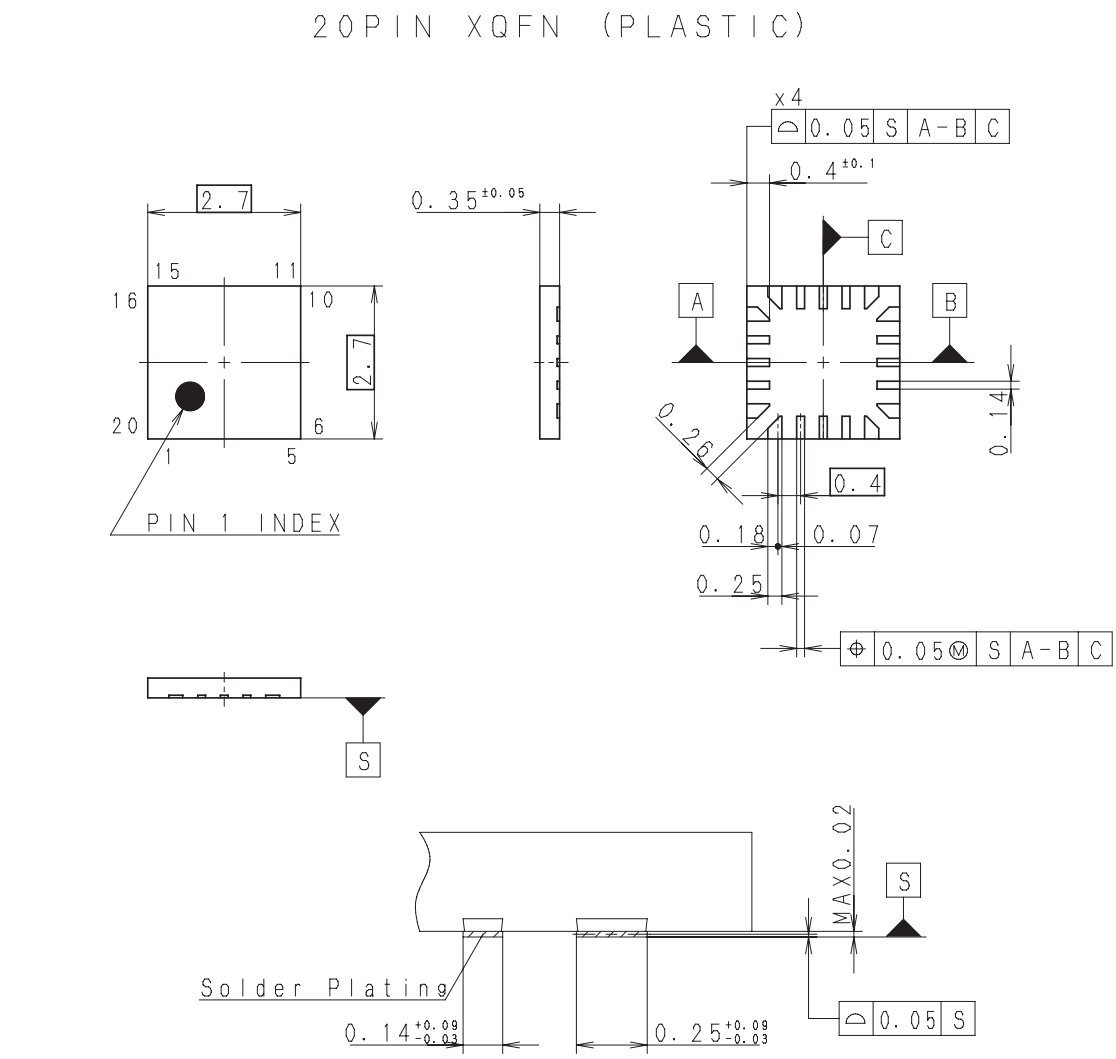
When using this IC, the following external components should be used:

CRF: This capacitor is used for RF decoupling and must be used for all applications. 100pF is recommended.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Package Outline

(Unit: mm)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	XQFN-20P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm