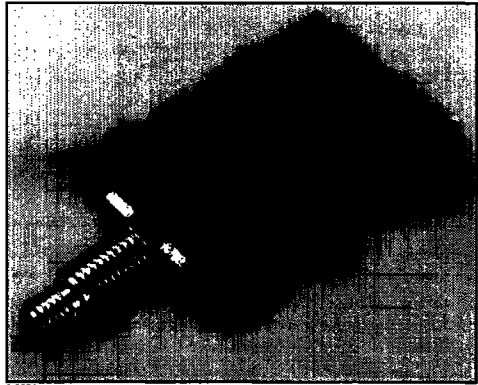


HFM1011

Low Profile Receiver Module

FEATURES

- 1.5 μ W optical sensitivity using 100/140 micron fiber
- Designed to operate with HFM2010 fiber optic transmitters
- SMA interface
- Standard TTL interface
- Low profile package only 0.32 in. high
- Signal quality latch designates module operation
- Case operating temperature range from -55 to +100°C



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DESCRIPTION

The HFM1011 fiber optic receiver module is designed for point-to-point digital data transmission. This low profile module converts bilevel or trilevel optical signals into a TTL level output.

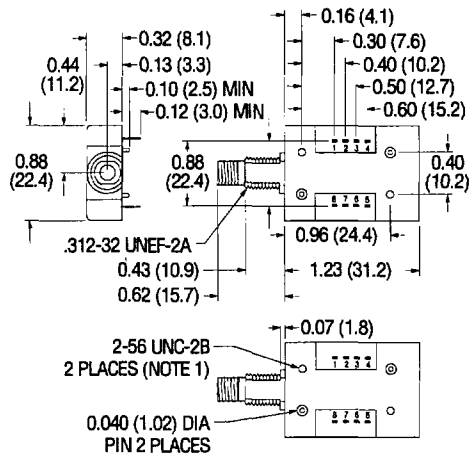
The module contains an AC coupled bipolar MASTERSLICE IC and PIN photodiode. It requires periodic signal transitions such as those supplied by the trilevel transmitter module HFM2010. Internal voltage regulation allows adjustment-free operation over the full operating temperature range without external power supply filtering.

APPLICATION

The HFM1011 receiver may be used with the trilevel HFM2010 transmitter for up to 10 Mbps data transmission. Light falls directly on the PIN photodiode. It drives a transimpedance pre-amp which uses a direct coupled (DC) feedback loop to soak up the DC component of the photodiode current.

The AGC (automatic gain control) post-amp output constant amplitude peaks are averaged by a DC loop capacitor. The capacitor also AC couples the combination amplifier. A pair of comparators sets a positive and negative threshold with respect to the average value of the input signal. Their latched outputs reconstruct pulse widths from the trilevel transparent code. For bilevel code, the latch output follows the signal transitions.

OUTLINE DIMENSIONS in Inches (mm)



FIBER02S DIM

Pinout

1. SQ signal quality
2. G ground
3. G ground
4. DO output
5. V V_{CC}
6. G ground
7. G ground
8. PD photodiode bias



HFM1011

Low Profile Receiver Module

APPLICATION (continued)

The Signal Quality output derives its input from the comparators, which allow the peak detectors to keep the AGC capacitor charged to maintain correct post-amp gain. Signal peaks of either polarity cause the SQ capacitor to discharge, keeping SQ latch reset (SQ output low). Failure of both peaks to keep the SQ capacitor discharged results in a time out, and sets the SQ latch (SQ output high) to indicate a bad input signal. The AGC capacitor is also discharged, increasing the post-amp gain.

Power up requires 25 ms. An additional 10 ms is necessary following initial light input to the receiver. If a bilevel optical signal is used, it must have a 50% duty cycle with pulse widths as given in RECOMMENDED OPERATING CONDITIONS.

Notes

1. Penetration greater than 0.09 in. (2.3 mm) into tapped holes may damage the module.
2. Leads (pins 1 to 8) are 0.01 in. (0.25 mm) x 0.02 in. (0.50 mm).
3. Data Output and SQ Output are bipolar TTL type outputs.
4. To keep SQ Output low, input transitions must occur at least every $1/f_R$ period (refresh pulses).
5. PD (pin 8) may be used to monitor photodiode current during testing. It must be connected to V_{CC} (pin 5) or separate 5 V supply for proper module operation.



HFM1011

Low Profile Receiver Module

ELECTRO-OPTICAL CHARACTERISTICS (Values shown apply over ranges given in RECOMMENDED OPERATING CONDITIONS unless otherwise stated.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
High Level Logic Output Voltage	V_{DOH}	2.4	3.7		V	$I_{DOH} = I_{SOH} = -400 \mu A$, $P_H = 0 \mu W$
Low Level Logic Output Voltage	V_{DOL}	2.4	3.7		V	$I_{DOL} = I_{SOL} = 4 mA$, $P_H > 3 \mu W$
Supply Current	I_{CC}		35	60	mA	$P_H = 0 \mu W$
Output Short Circuit Current	I_{OSC}	-30	-80	-140	mA	$P_H = 0 \mu W$ (1)
Transition Time	t_r/t_f		7	11	ns	$P_H > 3 \mu W$, optical t_r/t_f < 25 ns, 10 Mbps
Propagation Delay	t_{PH}	38	62	100	ns	$P_H > 3 \mu W$, optical t_r/t_f < 25 ns, 10 Mbps
Pulse Width Distortion	PWD		1	15	%	$P_H > 3 \mu W$, $(t_{IN} - t_{OUT})/t_{IN}$, optical $t_r/t_f < 25 ns$, 10 Mbps
Edge Jitter (RMS)			1.3	2.5	ns	$P_H > 3 \mu W$, optical $t_r/t_f < 25 ns$, 10 Mbps
Input Sensitivity (2)	P_{INBER}		0.5	1.5	μW	$BER \leq 10^{-9}$ (4) (5)
	$P_{IN SQ}$	0.2	0.4	0.8	μW	SQ Low Threshold

Notes

- I_{OSC} flows during momentary connection of DO (pin 4) to GND while DO is at V_{OH} .
- For typical values, $V_{CC} = 5$ volts and $T_{AMB} = 25^\circ C$.
- $K = (P_H - P_O)/P_O$ is a measure of the difference in amplitude for trilevel pulses.
- Max edge jitter specified corresponds to a normalized Bit Error Rate (BER) of 10^{-9} if the output is strobed with an ideally phased jitter-free clock. BER is guaranteed, but not normally tested.
- Minimum P_O for operation should be 2 dB higher than the rated P_O of the part when refresh pulses only are present.

ABSOLUTE MAXIMUM RATINGS

(25°C Free-Air Temperature unless otherwise noted)

Storage temperature	-65 to +150°C
Case operating temperature	-55 to +100°C
Lead solder temperature	260°C, 10 s
Supply voltage	-0.5 to +7 V

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Case operating temperature	-55 to +100°C
Supply voltage	+5 ± 10% V
Average optical input power	1.5 to 200 μW
Optical input pulse width, t_L or t_H	40 to 600 ns
Refresh repetition rate, f_R	1.0 Mbps
Amplitude symmetry ratio, k	0.8 to 1.2 (3)



HFM1011

Low Profile Receiver Module

ORDER GUIDE

Description	Catalog Listing
Standard low profile module, SMA optical connector	HFM1011-222

FIBER INTERFACE

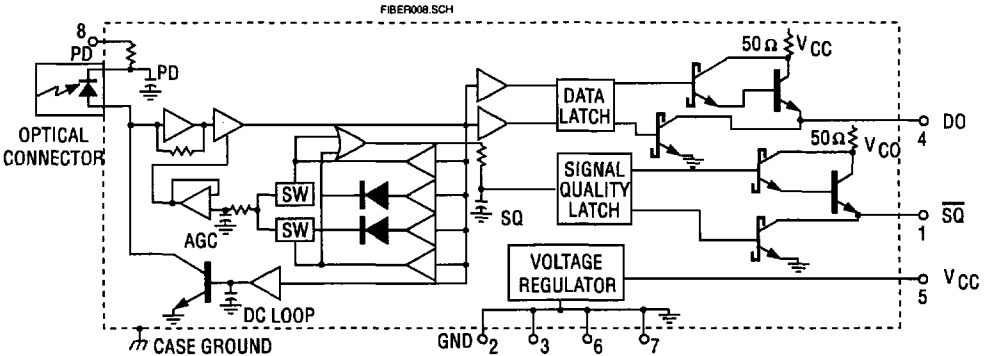
Honeywell detectors are designed to interface with multimode fibers with sizes (core/cladding diameters) ranging from 50/125 to 200/230 microns. Honeywell performs final tests using 100/140 micron core fiber.

CAUTION

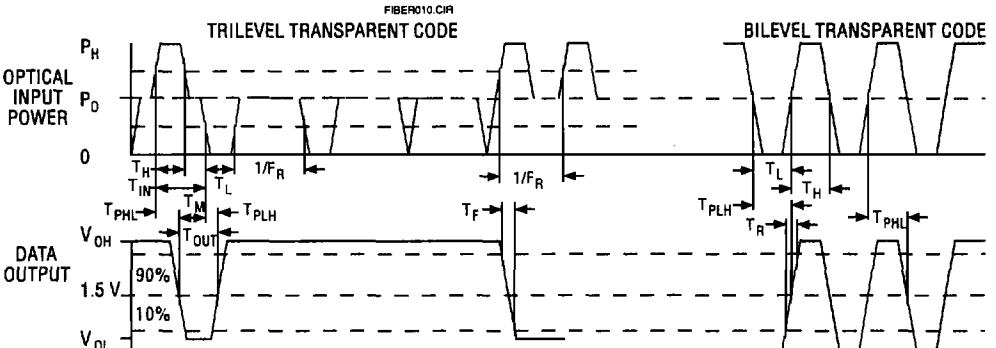
The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation to equipment, take normal ESD precautions when handling this product.



BLOCK DIAGRAM



DECODING AND TIMING DIAGRAM



HFM1011

Low Profile Receiver Module

TEST LOAD

DIODES ARE 1N914
OR EQUIVALENT

