OC-3/STM-1 Receiver with Clock Recovery

SRC03 Series

Product Description

The SRC03 is a Receiver Module with internal clock,recovery designed to meet or exceed the SONET/SDH optical interface requirements at OC-3/STM-1 (155 Mb/s) data rate. Highly reliable InGaAs/InP PIN photodiodes are used to cover the entire long wavelength range from 1100 nm to 1550 nm.

The receiver features a low noise GaAs transimpedance IC with AGC capability to provide an extremely wide dynamic range and high sensitivity. A Phase Lock Loop (PLL) circuit is included to perform the clock recovery function and resampling of the data.

The SRC03 receiver can be operated with dual +5 V and - 5 V supply, or single +5 V supply. The DATA & CLOCK interface signals are differential PECL while the SIGNAL DETECT outputs have TTL interface.

The SRC03 module operate over an operating temperature range of 0°C to +70°C ("H" option) or -40°C to +85°C (" " option). They are housed in a 20-pin dual-in-line metal package with integral ST, FC or SC connector receptacle or 50 µm multimode fiber pigtail. The fiber pigtail is terminated with ST, FC or SC connector.

Related OC-3/STM-1 transmitters & receivers

STX-03-LED: 20-pin LED transmitter

STX-03: 20-pin laser transmitter

SRX-03: 20-pin receiver without clock recovery

SRC-03-S: 24-pin receiver with clock recovery

Features

- ☑ Full compliance with SONET/SDH OC-3/STM-1 specifications
- ☑ Long Reach and Intermediate Reach
- ☑ Phase-Lock-Loop (PLL) Clock Recovery
- ☑ - 40°C to +85°C Operating Temperature (option "I")
- ☑ Multi-sourced 20-pin DIP metal package
- ☑ FC, ST, SC-connectorized fiber pigtails or Integral FC, SC or ST connector receptacle
- ☑ PECL DATA & CLOCK interface
- ☑ TTL SIGNAL DETECT interface

Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
Storage Temperature		T_{ST}	- 40	+ 85	°C
Operating Temperature	"I" option	T_{OP}	- 40	+ 85	°C
	"H" option		0	+ 70	
Operating & Storage Humidity		-	-	85	%
Supply Voltage		V_{CC}	0	+ 6.0	V
Lead Soldering Temperature & Time		-	-	260°C, 10 sec	

Receiver Electrical Interface (Over Operating Case Temperature)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage [1]	V_{CC}	4.75	5.0	5.5	V
	V_{PD}	- 10.0	- 5.0	- 2.0	V
Supply Current	I_{CC}	-	85	120	mA
Output HIGH Voltage (DATA & CLOCK)	V_{OH}	V_{CC} - 1.20	-	V_{CC} - 0.70	V
Output LOW Voltage (DATA & CLOCK)	V_{OL}	V_{CC} - 2.0	-	V_{CC} - 1.70	V
Output HIGH Voltage (SIGNAL DETECT)	V_{OH}	2.7	-	V_{CC}	V
Output LOW Voltage (SIGNAL DETECT)	V_{OL}	0	-	0.5	V

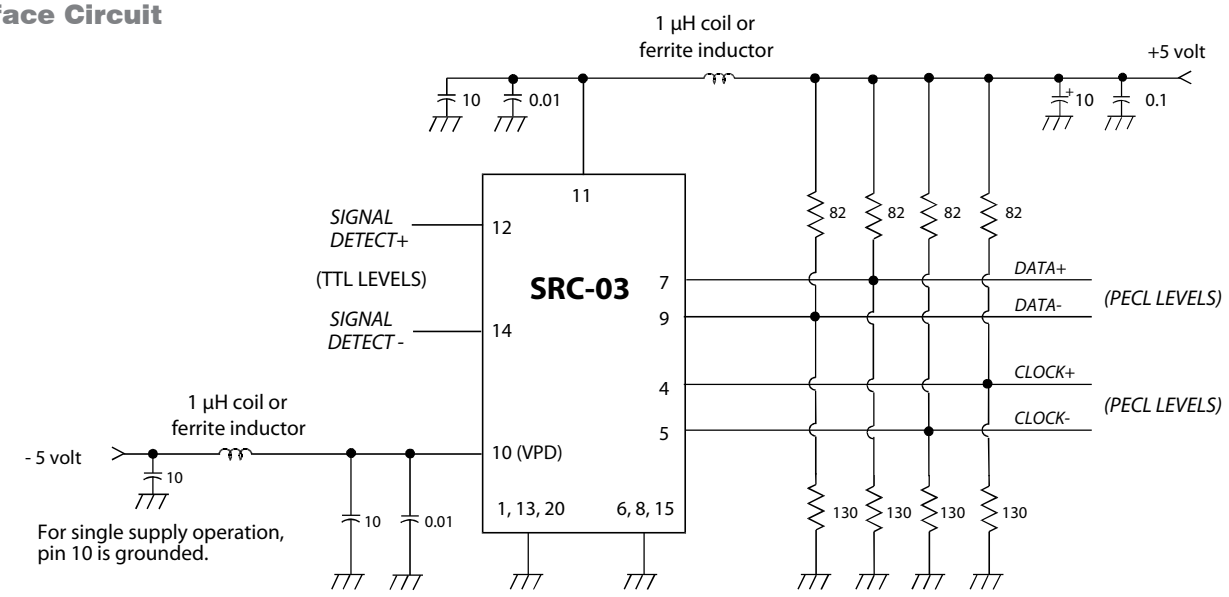
[1] For +5V & - 5V dual supply: V_{CC} = +5V, CASE = GND = 0V and V_{PD} = - 5V.
V_{PD} is the photodiode supply voltage only. I_{VPD} can be used for monitoring the signal photocurrent.
For +5V single supply: V_{CC} = +5V, V_{PD} = CASE = GND = 0V.

Receiver Performance Characteristics (Over Operating Case Temperature)

Parameter		Symbol	Minimum	Typical	Maximum	Units
Data Rate		B	155	155.52	156	Mb/s
Receiver Sensitivity (10^{-10} BER) [1]		P_{min}	- 34.0	- 36.0	-	dBm
Maximum Input Optical Power (10^{-10} BER) [1]	Single Supply	P_{max}	- 6.0	0	-	dBm
	Dual Supply		- 3.0	0	-	
Signal Detect Thresholds	Increasing Light Input	P_{sd+}	-	-	- 34.0	dBm
	Decreasing Light Input	P_{sd-}	- 45.0	-	-	dBm
Signal Detect Hysteresis			-	0.5	-	dB
Wavelength of Operation		λ	1100	-	1600	nm
Output Clock Jitter		CLK_J	-	-	0.01	UIrms
Jitter Tolerance & Transfer Function		compliant with ITU Recommendation G.958				

[1] Specified in Average Optical Input Power and measured at 1300 nm wavelength with 2^{23}-1 PRBS.

Interface Circuit



RESISTOR VALUES ARE IN OHM, CAPACITOR VALUES ARE IN µF UNLESS OTHERWISE INDICATED

Application Notes

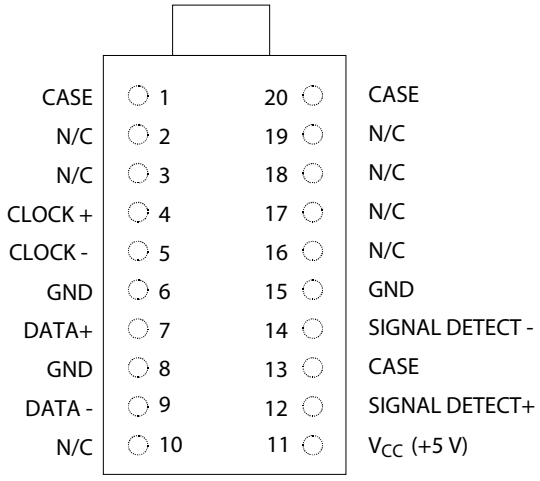
Receiver Circuit: The receiver converts the incident optical power to a photocurrent via a high performance PIN photodiode. The photocurrent is converted to a voltage signal by a transimpedance amplifier. This signal is then amplified by additional gain stages and processed through a shaping filter and a comparator to generate the data to the clock recovery circuit. The clock recovery circuit uses a Phase Lock Loop (PLL) to recover the clock from the data and resamples the data to generate clean and reshaped differential DATAoutputs. Also provided are differential recovered CLOCK outputs.

Both differential DATA+ and DATA- as well as CLOCK+ and CLOCK- outputs are open emitter PECL levels requiring termination (50 ohms to V_{CC} - 2 volts or 510 ohms to *GND* is recommended). For optimum performance, both outputs should be terminated in the same manner, even if only one is used.

The Signal Detect circuit monitors the level of the incoming optical signal and generates a logic LOW (TTL) signal when insufficient photocurrent is produced.

Interface Circuit: The power supply line should be wellfiltered. The power supply should be bypassed by 0.01 or 0.1 µF ceramic chip capacitors placed as close to the receiver module as possible. If the receiver outputs drive long traces or multiple loads, the use of an ECL buffer gate to isolate the receiver from transmission line reflections is recommended.

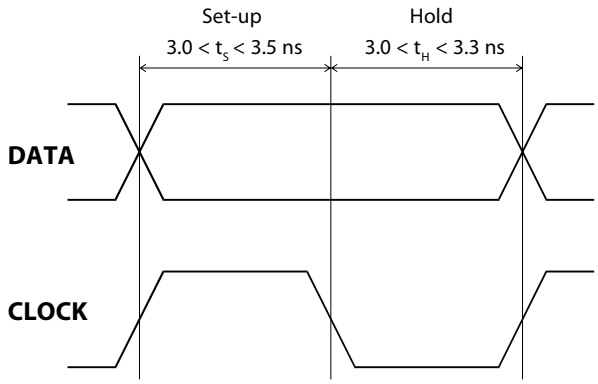
Pin Assignments (Top View)



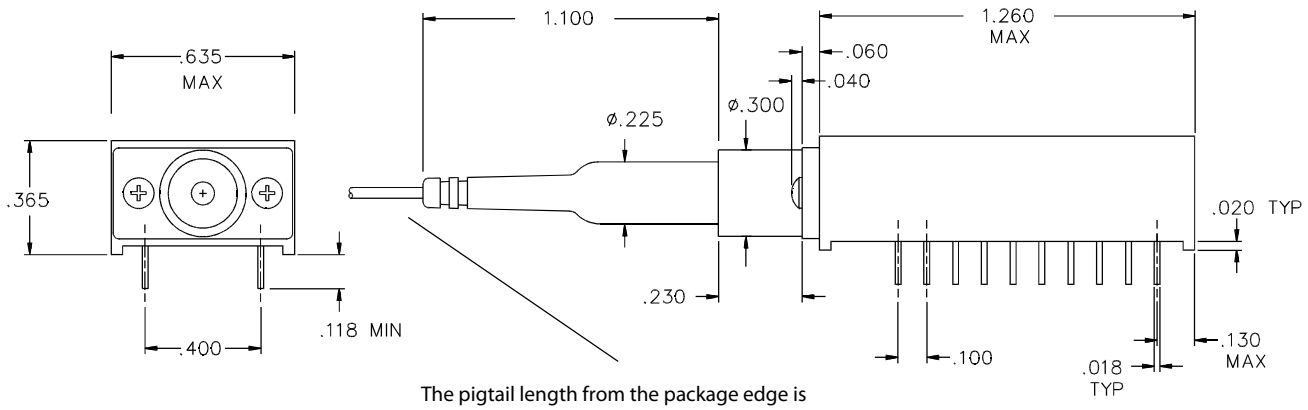
N/C: No internal connection

All CASE pins should be grounded

DATA & CLOCK Timing Diagram



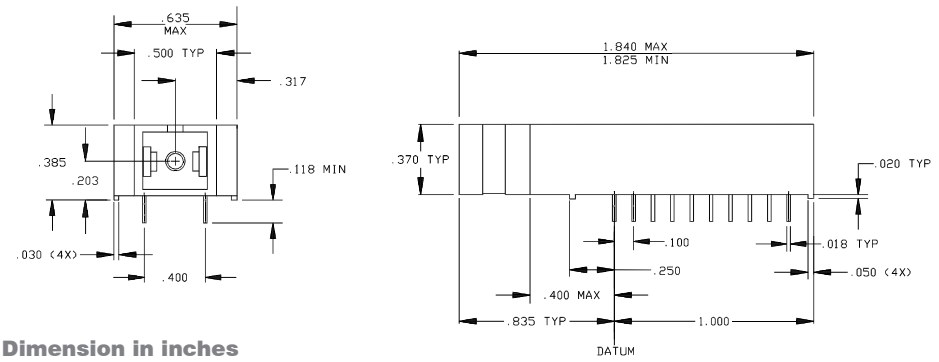
Pigtail Package



The pigtail length from the package edge is 1.0 meter minimum, 1.1 meter typical.

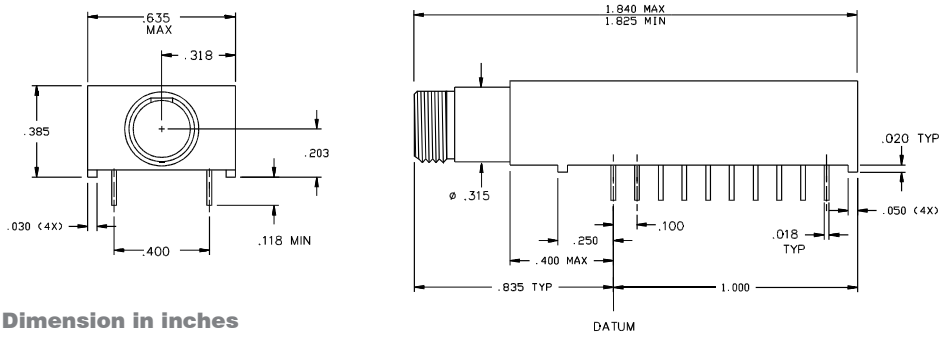
Dimension in inches

SC-receptacled Package



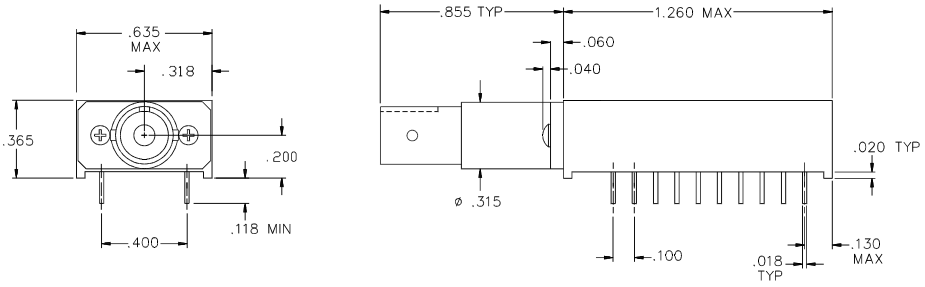
Dimension in inches

FC-receptacled Package



Dimension in inches

ST Receptacle Package



Dimension in inches

Laser Safety: All transceivers are Class I Laser products per FDA/CDRH and IEC-60825 standards. They must be operated under specified operating conditions.

Oplink Communications, Inc.
DATE OF MANUFACTURE:

This product complies with 21 CFR 1040.10 and 1040.11
Meets Class I Laser Safety Requirements

Ordering Information

SRC	8	0	3	X	R	1	☐	0	0	0	☐	☐

Supply Voltage
RX only 5V= 8

Receivers

Wavelength Range
1100~1600nm PIN

Temperature Range
-40 ~85˚C= I
0~70˚C= H

Connector Type & Option
Pigtail FC, SD-TTL = PA
Pigtail ST, SD-TTL = PB
Pigtail SC, SD-TTL = P5
Pigtail FC, SD-PECL = PC
Pigtail ST, SD-PECL = PD
Pigtail SC, SD-PECL = P4

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