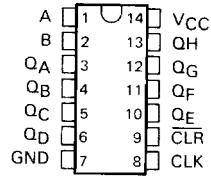
# SN54ALS164, SN74ALS164
# 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

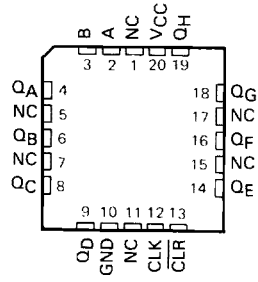
D2661, APRIL 1982 – REVISED MAY 1986

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS164 . . . J PACKAGE
SN74ALS164 . . . D OR N PACKAGE
(TOP VIEW)




SN54ALS164 . . . FK PACKAGE
(TOP VIEW)



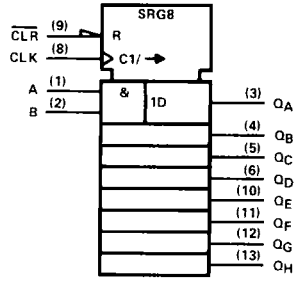

NC – No internal connection

## description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54ALS164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS164 is characterized for operation from 0°C to 70°C.

## logic symbol†



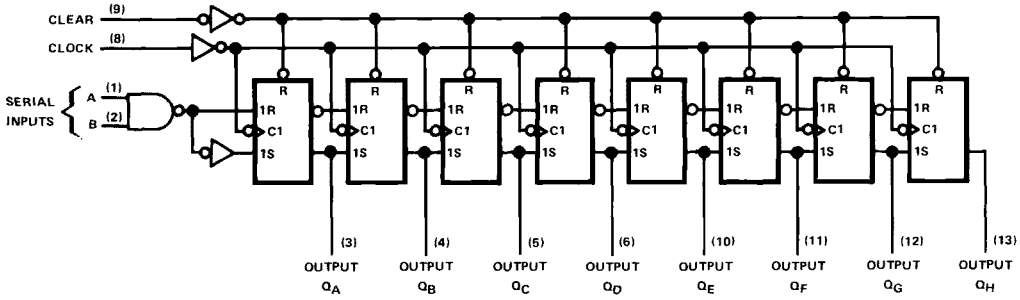

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J and N packages.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| CLEAR | CLOCK | A | B | $Q_A$ | $Q_B$ . . . $Q_H$ | |
| L | X | X | X | L | L | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | $Q_{Gn}$ |

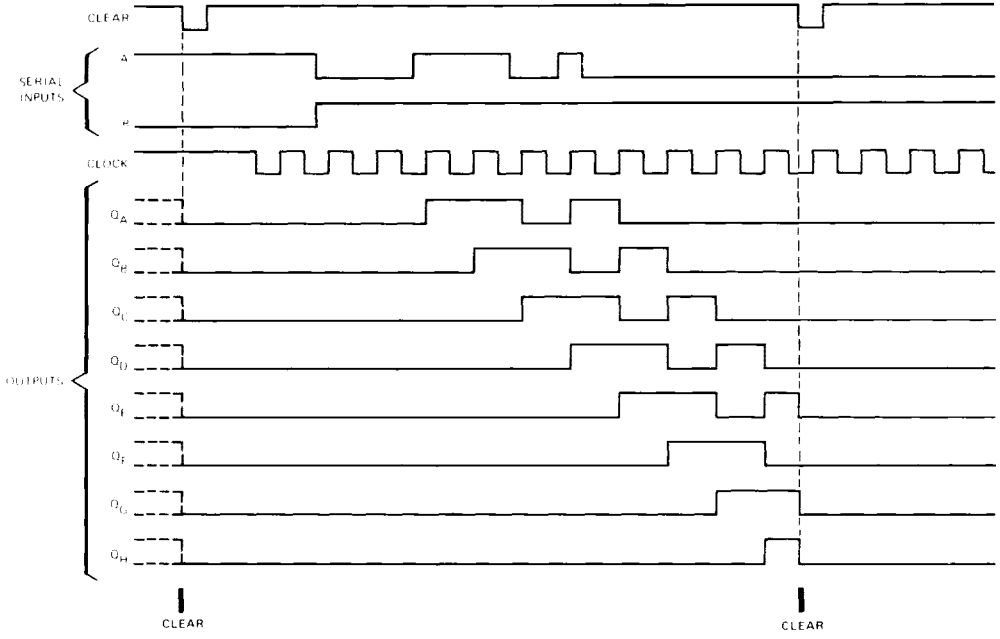
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Gn}$ = the level of $Q_A$ or $Q_G$ before the most-recent ↑ transition of the clock; indicates a one-bit shift.

### logic diagram (positive logic)




Pin numbers shown are for D, J, and N packages.

### typical clear, shift, and clear sequences




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS164 . . . . . −55 °C to 125 °C
SN74ALS164 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C



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### recommended operating conditions

| | | | SN54ALS164 | | | SN74ALS164 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | | | | | | | MHz |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | | | | | | | ns |
| | | CLK high | | | | | | | |
| | | CLK low | | | | | | | |
| $t_{su}$ | Setup time before CLK↑ | SH/$\overline{LD}$ | | | | | | | ns |
| | | Data | | | | | | | |
| | | $\overline{CLR}$ inactive | | | | | | | |
| $t_h$ | Hold time, data after CLK↑ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALS164 | | | SN74ALS164 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | $V_{CC}$−2 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.1 | | | −0.1 | mA |
| $I_O$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | See Note 1 | | 10 | | | 10 | | mA |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.
NOTE 1: With 4.5 Volts applied to the serial input and all other inputs except the clock grounded, $I_{CC}$ is measured after a clock transition from 0 to 4.5 volts.

### switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | SN54ALS164 | | | SN74ALS164 | | | |
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $f_{max}$ | | | | 60 | | | 60 | | MHz |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | | 12 | | | 12 | | ns |
| $t_{PLH}$ | CLK | Any Q | | 10 | | | 10 | | ns |
| $t_{PHL}$ | | | | 11 | | | 11 | | |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

**Additional information on these products can be obtained from the factory as it becomes available.**