



PRELIMINARY

CY82C69x

# Pentium™ hyperCache™ Chipset Family

## System Features

- Full system, data, cache, and peripheral control
  - CY82C691 System Controller
  - CY82C692 Data Path Unit with integrated 128-KB BSRAM
  - CY82C693 Peripheral Controller
  - CY82C693U Peripheral Controller with USB support
  - CY82C694 128-KB Expansion Cache Unit
- Supports all 3.3V Pentium™, AMD K5, K6, and Cyrix 6x86 (M1) CPUs
- Full support for ISA, PCI, and USB interfaces
- Integrated 8Kx21 tag (direct mapped and two-way set associative) supporting cache sizes up to 512 MB
- Integrated 16K by 64 (128-KB) Pipelined BSRAM
- Supports 6 banks of DRAM with up to 768 MB main memory
- Fully integrated Peripheral Controls
  - Keyboard Controller with full 8042 functionality
  - PS/2-compliant mouse controller
  - Real-time clock with 242 bytes user-defined SRAM
  - Dual-channel enhanced EIDE controller with CD-ROM and PCI bus mastering support
  - Two 8237-compliant DMA controllers

— General purpose I/O pins and registers

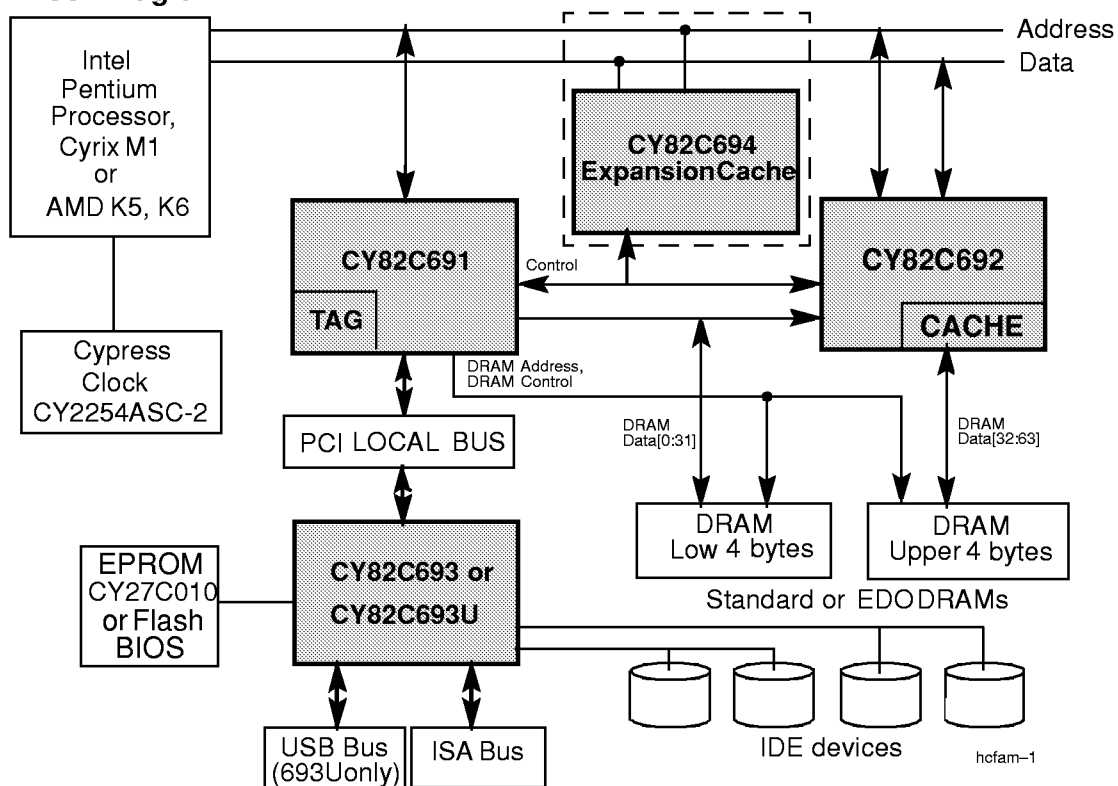
- Flexible power management with five timers and ten programmable event detectors

## System Overview

The hyperCache™ family is a family of chips created to provide flexible solutions for today's PC designs. The chipset provides all the functions necessary to implement a 3.3V Pentium-class processor based system with the USB (Universal Serial Bus), PCI (Peripheral Component Interconnect), and the ISA (Industry Standard Architecture) buses. System designers can exploit the advantages of the USB and PCI buses while maintaining access to the large base of ISA cards in the marketplace.

The Cypress hyperCache family offers system designers several key advantages. With only three chips, a complete system can be implemented. Cache can be added up to 512 MB with additional CY82C694 devices in 128-KB increments or with commercial synchronous SRAMs. Upgrading between solutions (e.g. addition of USB support) is straight-forward since all solutions are pin-compatible. Six banks of page-mode or EDO DRAM further increase the system designer's options. The chipset also contains concurrent bus support, PCI enhanced IDE with CD-ROM support, integrated RTC, integrated peripheral control (Interrupts/ DMA), and integrated keyboard controller. This chipset is flexible enough to provide the system designer with many cost/performance/function options to build an optimum solution Pentium-based system.

## System Block Diagram



# CY82C691 System Controller

## CY82C691 System Controller Features

- Provides control for the cache, system memory, and the PCI bus
- PCI Bus Rev. 2.1 compliant
- Supports all 3.3V Pentium™, AMD K5, K6, and Cyrix 6x86 (M1) CPUs
- Support for WB or WT L1 cache
- Supports 3-1-1-1 burst read/write operation at 66, 60, and 50 MHz bus speeds
- Supports CPU address pipelining
- Support for synchronous or pipelined BSRAMs
- Provides power management support through SMM (APM compliant)
- Integrated 8Kx21 tag (direct mapped and two-way set associative) supporting cache sizes up to 512 MB
- Supports mixed standard page-mode and EDO DRAMs
- Supports VESA Unified Memory Architecture (VUMA)
- Support for standard 72-bit-wide DRAM banks
- Supports non-symmetrical DRAM banks
- Supports six banks of DRAM (six RAS lines) with DRAM densities up to 16 Mb
- Up to 768 MB main memory
- Variable drive on DRAM address lines (max. 20 mA)
- Provides glueless (0 TTL) system solution
- Support for concurrent operation among CPU, cache, DRAM, and PCI
- Byte-Merge operation

- 8 deep PCI post-write/pre-read buffers
- Packaged in a 208-pin PQFP

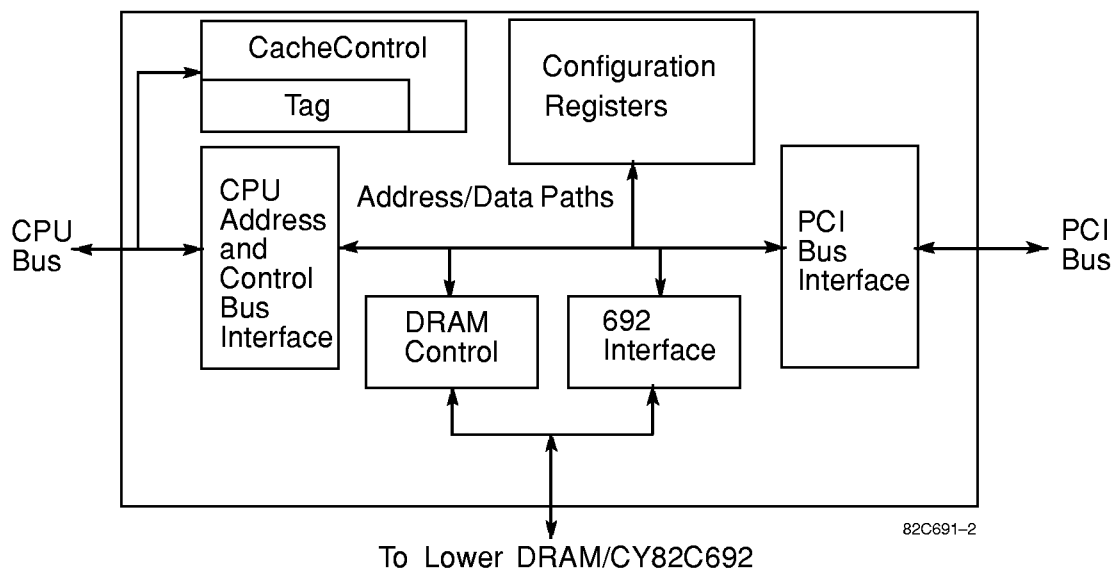
## CY82C691 Functional Overview

The CY82C691 System Controller is a highly integrated device. It provides control for the CPU, cache, memory, and PCI. The memory controller supports up to 768 MB of main memory with standard page-mode DRAMs or EDO DRAMs. The cacheable range can be configured to cover the entire DRAM main system memory space. Support is provided for up to 6 banks of 72-bit wide DRAM SIMMs. Asymmetrical DRAM banks are also supported. 20 mA outputs with programmable drive are provided on the DRAM lines, thus eliminating the need for external buffers.

The cache controller supports a look-aside (parallel) cache with synchronous or pipelined burst SRAMs. Asynchronous SRAMs are not supported. Burst reads and writes to and from the cache with 3-1-1-1 timing are maintained even at 66 MHz. The CY82C691 integrates an 8Kx21 tag-RAM to further reduce system cost. The tag can be configured to be either direct mapped or two-way set associative. Cache sizes can range from 128 KB to 512 MB in 128-KB increments. Cache coherency with main memory is maintained at all times.

Bus concurrency is supported between the CPU, cache, DRAM, and PCI bus with the use of post-write and pre-read FIFOs. Pentium pipelined addressing and power management features (SMM) are supported. The CY82C691 also supports the Cyrix M1 processor and the AMD K5 processor. The CY82C691 also generates all the control for the CY82C692 Data Path/Cache chip.

## CY82C691 Block Diagram



# CY82C692 Data-Path Controller

## CY82C692 Data Path Features

- Supports all 3.3V Pentium™, AMD K5, K6, and Cyrix M1 CPUs
- Directly interfaces with CY82C691 and CY82C693 to provide high-performance three-chip Pentium Chipset system
- Provides 64-bit data path between CPU, PCI, and DRAM memory
- 3.3V I/O CPU bus operation
- On-Chip 8-Deep FIFOs support Post-Writing/Pre-Reading PCI data
- Provides Data steering and Bus size conversion

## CY82C692 Integrated Cache Features

- 16K by 64 (128-KB) Integrated Pipelined BSRAM
- Direct-mapped or two-way set associative L2 cache mapping configurations
- Supports 3-1-1-1 Level 2 cache operation up to 66 MHz bus speed
- Fast Clock-to-Data ( $T_{CO}$ )=8.5 ns
- Synchronous self-timed write to L2 cache BSRAM
- Packaged in a 208-pin PQFP

## CY82C692 Functional Overview

The CY82C692 is a 64-bit data path unit between the DRAM and CPU for the hC-VX and hC-DX chipsets. The CY82C692 serves two main functions: (1) Provides data steering to/from three different interfaces (CPU bus, the DRAM high or MD bus, and the DRAM low or CY bus), and (2) Provides 128 KB of integrated synchronous pipelined burst SRAM. With a

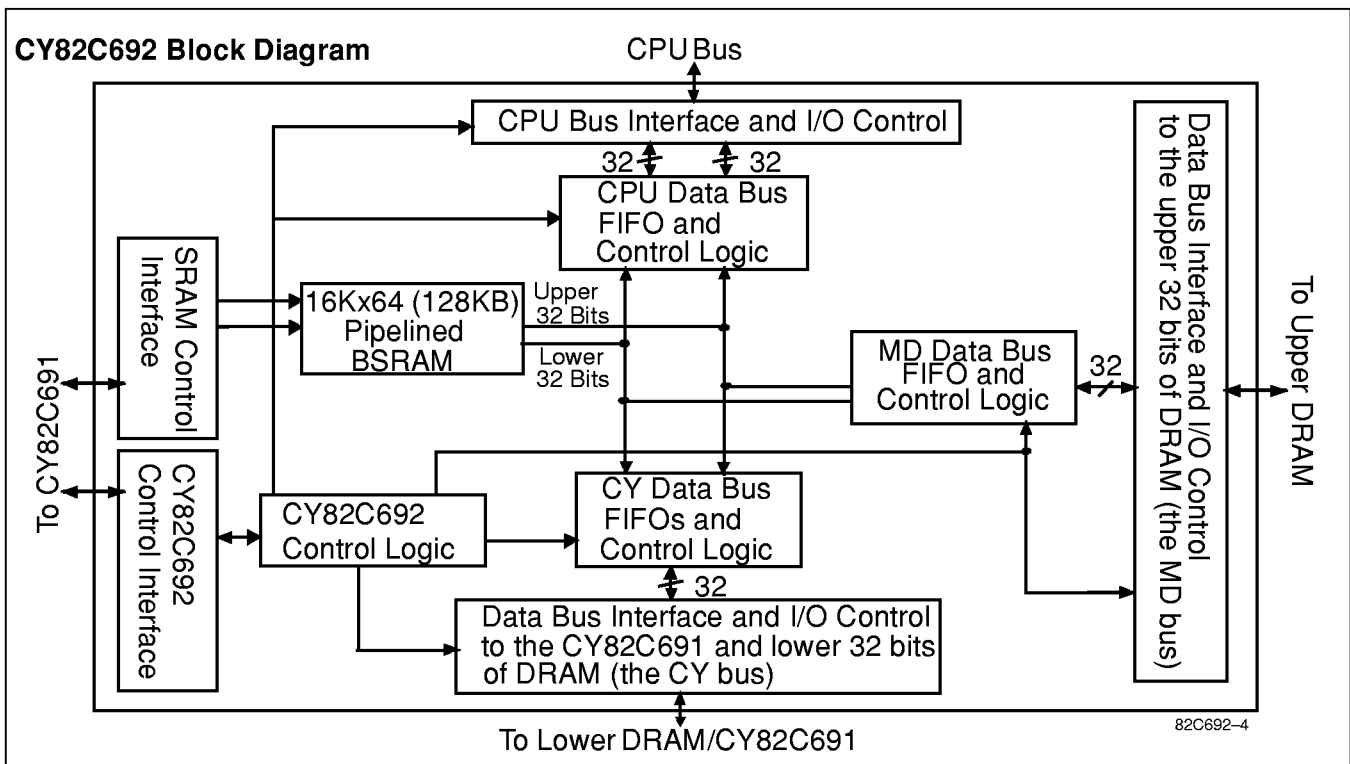
clock-to-data valid time ( $T_{CO}$ )=8.5 ns, 3-1-1-1 burst cycles are supported at bus frequencies up to 66 MHz.

The CY82C692 contains several sets of FIFOs that serve as Pre-Reading/Post-Writing buffers. These buffers are controlled by signals (Control[10:0]) coming from the CY82C691 System Controller. The Pre-Reading/Post-Writing feature enhances system performance by allowing concurrent transactions on the CPU, PCI, and DRAM buses.

The 3.3V CPU bus interface contains an 8-deep, 64-bit wide FIFO. This FIFO is logically broken into two 32-bit FIFOs in order to properly route data and accommodate for bus size-conversions. All data going to the CPU data bus must pass through the CPU FIFO.

The DRAM interface is divided between the upper 32 bits and lower 32 bits of data. The upper 32 bits are transferred on the MD bus. The MD bus is a dedicated connection between the CY82C692 and the upper 32 bits of DRAM memory. The lower 32 bits of data are transferred on the CY bus. The CY bus also serves as the data path connecting the PCI bus (via the CY82C691) to the CPU.

The CY82C692 contains an integrated Level 2 cache configured as a 16Kx64 (128-KB) synchronous pipelined BSRAM. The BSRAM can be used as either a direct mapped or two-way set associative L2 cache. The BSRAM is controlled by dedicated control signals coming from the CY82C691 System Controller. The L2 cache can be expanded with additional CY82C694s (Cypress's 16Kx64 pipelined BSRAM in a 128-pin TQFP) or additional discrete BSRAMs (synchronous or pipelined). Each bank must be comprised of the same type of BSRAM. L2 cache sizes of up to 512 MB are supported, using one or two banks.



# CY82C693 / CY82C693U Peripheral Controller

## CY82C693 / CY82C693U Features

- PCI to ISA bridge
- PCI Bus Rev. 2.1 compliant
- Supports up to 5 additional PCI masters including the CY82C691
- Integrated Open HCI USB host controller supporting 2 USB ports (CY82C693U only)
- Integrated DMA controllers with Type A, B, and F support
- Integrated Interrupt controllers
- Integrated timer/counters
- Integrated Real-Time-Clock with 256 bytes of battery-backed SRAM (14 bytes of clock RAM and 242 bytes of CMOS scratch RAM)
- Write-only Register Shadowing
- Integrated Dual-Channel enhanced IDE controller with
  - PCI bus mastering
  - CD ROM support
  - PIO modes 0 through 4 operation
  - Single-word and Multi-word DMA modes 0 through 2
- Integrated Keyboard Controller
- Integrated PS/2 Mouse Controller
- APM compliant power management support through SMM or under hardware control
- Flash PROM support with Write-protection
- Power-on reset circuitry

- QuietBus™ support for the PCI and ISA bus interfaces for better noise immunity
- General-purpose I/O pins and registers
- Zero TTL system operation
- Provides PCI-ISA/ISA-PCI/IDE-PCI/PCI-IDE post writing
- Provides ISA-PCI pre-reading
- Packaged in a 208-pin PQFP

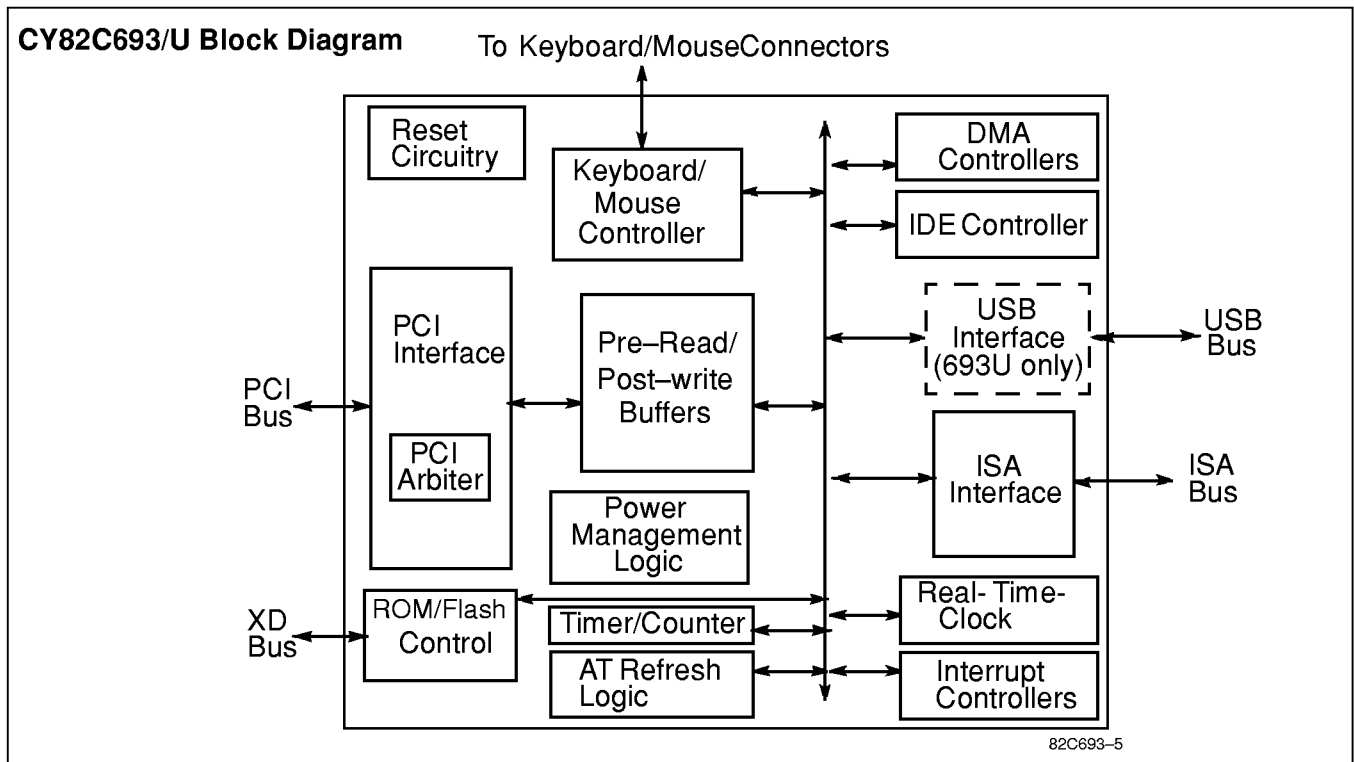
## CY82C693 Functional Overview

The CY82C693 is a highly integrated peripheral solution for PCI-based motherboards. The CY82C693 provides a bridge between the PCI bus, the ISA bus, and the IDE peripherals. The CY82C693 provides support for 6 PCI masters. In addition, the CY82C693 integrates several key peripherals, including an 8042-compatible keyboard controller, support for a PS/2 mouse, a real time clock with 256 bytes of battery-backed RAM, two 8237-compatible DMA controllers, and a dual-channel enhanced IDE controller. For added flexibility, the keyboard controller can be fabbed with custom code.

The CY82C693 also contains the logic to support AT refresh cycles on the ISA bus and provides flexible power management with 5 timers and 10 programmable event detectors. Additional features include two general-purpose I/Os and support for 4 MB of Flash ROM.

## CY82C693U - USB Support

The CY82C693U is pin-compatible with the CY82C693. In addition to the features listed above, it incorporates the logic for an Open HCI-compliant USB host controller and 2 USB ports.



# CY82C694 128-KB hyperCache™ Chipset Expansion RAM

## CY82C694 Features

- Interfaces directly to hyperCache™ Chipset (CY82C691/692/693) at 66 MHz with 0 wait states
- Synchronous pipelined operations with registered inputs and outputs
- 16K x 64 common I/O architecture
- I/Os capable of 3.3V operation
- Fast Clock-to-output timing —  $T_{CO}=8.5$  ns
- User selectable two-bit wraparound burst counter supporting Intel® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous address increment control logic
- Synchronous self-timed writes
- Individual byte write control
- Five chip selects allow easy memory depth expansion
- Asynchronous output enable
- 14 mm x 20 mm 128-pin TQFP package

## CY82C694 Functional Overview

The CY82C690 is a 16K by 64 synchronous/pipelined cache Burst SRAM (BSRAM) designed to support a zero wait state secondary cache with minimal glue logic.

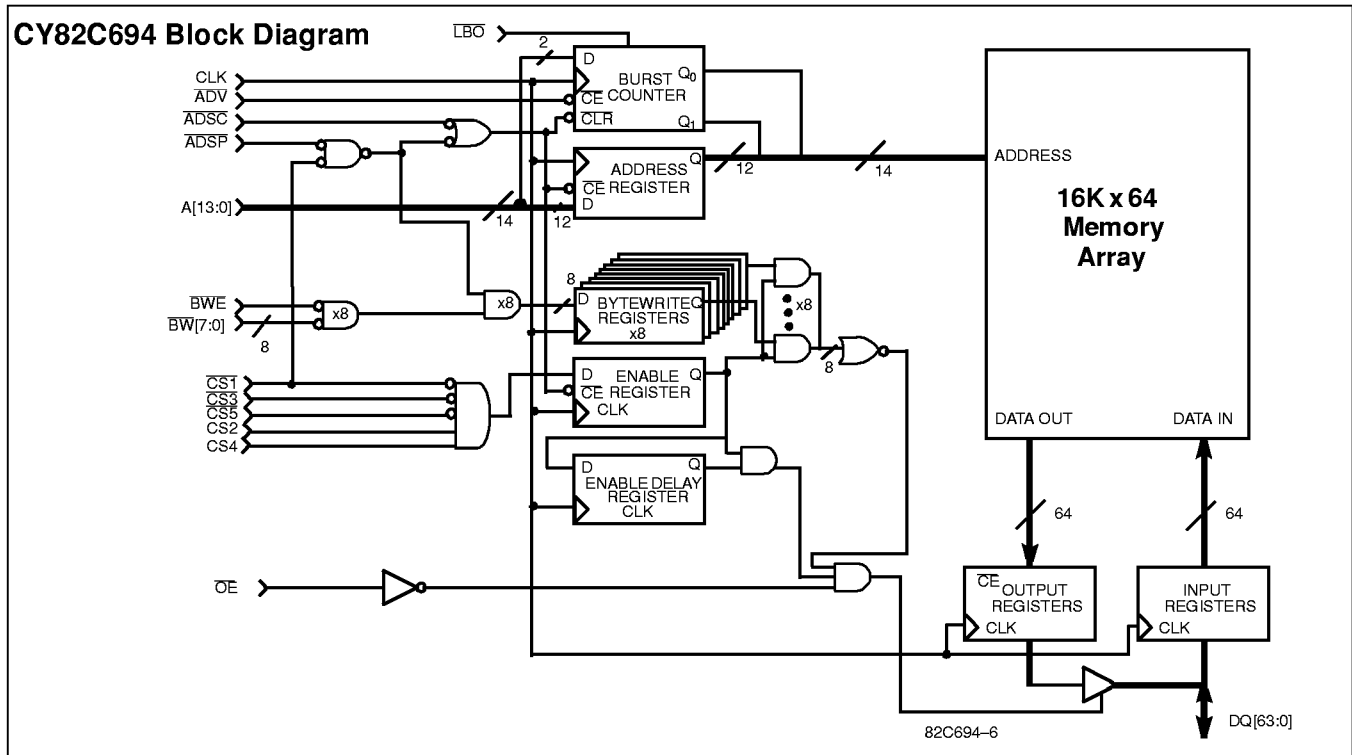
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through

output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise in pipelined mode ( $T_{CO}$ ) is 8.5 ns. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access according to the  $\overline{ADV}$  input.

The CY82C694 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence, such as the Cyrix 6X86. The burst order is user selectable, and is determined by state of the  $\overline{LBO}$  (Linear Burst Order) input. A LOW level selects the linear burst order while a HIGH level activates the interleaved burst order. Accesses can be initiated with either the processor address strobe ( $\overline{ADSP}$ ) or the controller address strobe ( $\overline{ADSC}$ ). Address advancement through the burst sequence is controlled by the  $\overline{ADV}$  input.

Byte write operations are qualified with the Byte Write Enable ( $\overline{BWE}$ ) and Byte Write Select ( $\overline{BW0-7}$ ) inputs. Writes operations are simplified with an on-chip synchronous self-timed write circuitry.

Five synchronous chip selects ( $\overline{CS1}$ ,  $\overline{CS5}$ ,  $\overline{CS3}$ ,  $\overline{CS4}$ ,  $\overline{CS2}$ ) and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output three-state control.  $\overline{ADSP}$  is ignored if  $\overline{CS1}$  is HIGH.



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