EPSON

Micro MINI S1C60N08/60R08

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- S1C6200C Core CPU
- Built-in LCD Driver
- Serial Interface

■ DESCRIPTION

The S1C60N08 Series is a single-chip microcomputer made up of the 4-bit core CPU S1C6200C, ROM (4,096 words × 12 bits), RAM (832 words × 4 bits), LCD driver, serial interface, event counter with dial input function, watchdog timer, and two types of time base counter. Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.
The S1C60R08 is a microcomputer with a CMOS 4-bit core CPU S1C6200C as main component, and a built-in programmable RAM (ROM emulator). The S1C60R08 has almost the same functions as the S1C60N08/60A08. The mask ROM in the S1C60N08/60A08 has been changed to a ROM emulator that allows the user to rewrite programs using a Serial EEPROM.

■ CONFIGULATION

The S1C60N08 Series is configured as follows, depending on supply voltage and oscillation circuits.

Model	**S1C60N08**	**S1C60A08**	**S1C60L08**
Supply voltage	3.0 V	3.0 V	1.5 V
Oscillation circuit	OSC1 only (Single clock)	OSC1 and OSC3 (Twin clock)	OSC1 only (Single clock)
Evaluation tool	**S1C60R08**		–

■ FEATURES

- OSC1 oscillation circuit ..... Crystal oscillation circuit 32.768 kHz (Typ.)/38.400 kHz (Typ.)
- OSC3 oscillation circuit ..... CR or ceramic oscillation circuit (∗1) 500 kHz (Typ.)
  ...**S1C60A08/60R08** only
- Instruction set ..... 108 types
- Instruction execution time ..... CLK = 32.768 kHz: 153 µsec, 214 µsec, 366 µsec
  (differs depending on instruction) CLK = 38.400 kHz: 130 µsec, 182 µsec, 313 µsec
  (CLK: CPU operation frequency) CLK = 500 kHz: 10 µsec, 14 µsec, 24 µsec...**S1C60A08/60R08** only
- ROM capacity ..... 4,096 words × 12 bits
- Serial EEPROM interface ..... Built-in (Microchip 24AA65 two wire bus protocol interfaces
  ...**S1C60R08** only
- RAM capacity ..... 832 words × 4 bits
- Input ports ..... 9 bits (pull-down resistor can be added ∗1)
- Output ports ..... 8 bits (BZ, $\overline{BZ}$, FOUT and SIOF outputs are available ∗1)
- I/O ports ..... 8 bits (pull-down resistor is added during input data read-out)
- Serial interface ..... 1 port (8-bit clock synchronous system)
- LCD driver ..... 48 segments × 4, 3, or 2 commons (∗1)
  V-3 V 1/4, 1/3 or 1/2 duty (voltage regulator and booster circuits built-in)
- Time base counter ..... Two types (timer and stopwatch)
- Watchdog timer ..... Built-in (∗1)

- Event counter ..... Two 8-bit inputs (dial input evaluation or independent)
- Sound generator ..... Programmable in 8 sounds (8 frequencies)
  Digital envelope built-in (∗1)
- Analog comparator ..... Inverted input × 1, non-inverted input × 1
- Battery low detection circuit (BLD) .. Dual system (programmable in 8 values and a fixed value)
  2.4 V, 2.2–2.55 V ...**S1C60N08/60A08/60R08**
  1.2 V, 1.05–1.4 V ...**S1C60L08**
- External interrupt ..... Input interrupt: 3 systems
- Internal interrupt ..... Time base counter interrupt: 2 systems
  Serial interface interrupt: 1 system
- Supply voltage ..... 3.0 V (1.8–3.5 V) ...**S1C60N08/60A08/60R08**
  1.5 V (0.9–1.7 V) ...**S1C60L08**
- Current consumption **S1C60N08**
  Halt state: 1.0 µA when CLK = 32.768 kHz (Typ.)
  Run state: 2.2 µA when CLK = 32.768 kHz (Typ.)

  S1C60L08
  Halt state: 1.0 µA when CLK = 32.768 kHz (Typ.)
  Run state: 2.2 µA when CLK = 32.768 kHz (Typ.)

  S1C60A08
  Halt state: 1.1 µA when CLK = 32.768 kHz (Typ.)
  Run state: 3.0 µA when CLK = 32.768 kHz (Typ.)
  Run state: 50 µA when CLK = 500 kHz (Typ.)

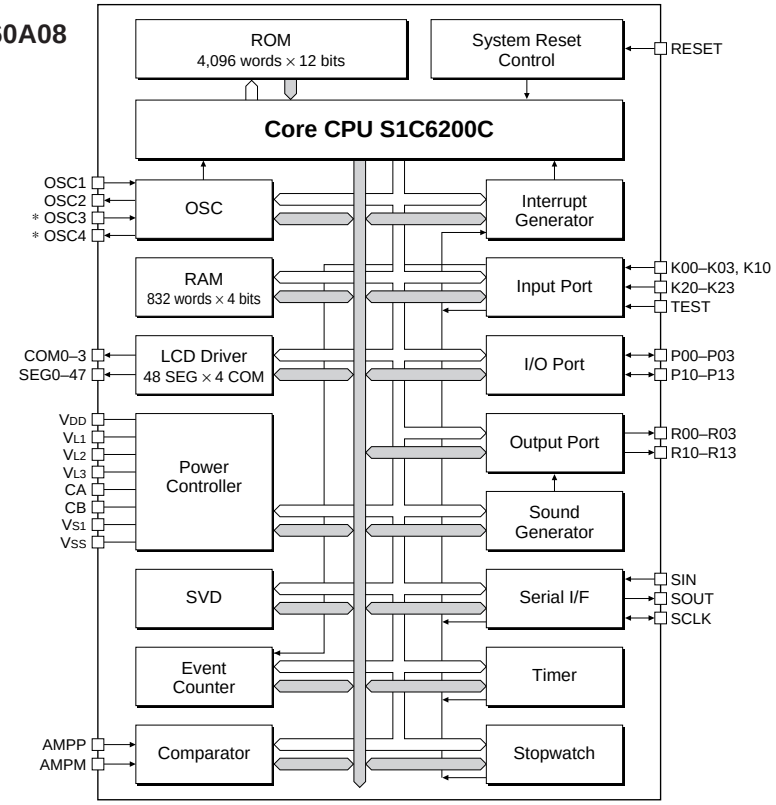
  S1C60R08
  Halt state: 1.0 µA when CLK = 32.768 kHz (Typ.)...Target for **S1C60N08**
  1.1 µA when CLK = 32.768 kHz (Typ.)...Target for **S1C60A08**
  Run state: 6.5 µA when CLK = 32.768 kHz (Typ.)...Target for **S1C60N08**
  7.5 µA when CLK = 32.768 kHz (Typ.)...Target for **S1C60A08**
  Run state: 115 µA when CLK = 500 kHz (Typ.)...Target for **S1C60A08** only
- Package ..... QFP5-100pin, QFP15-100pin (plastic) or chip

∗1: Can be selected with mask option

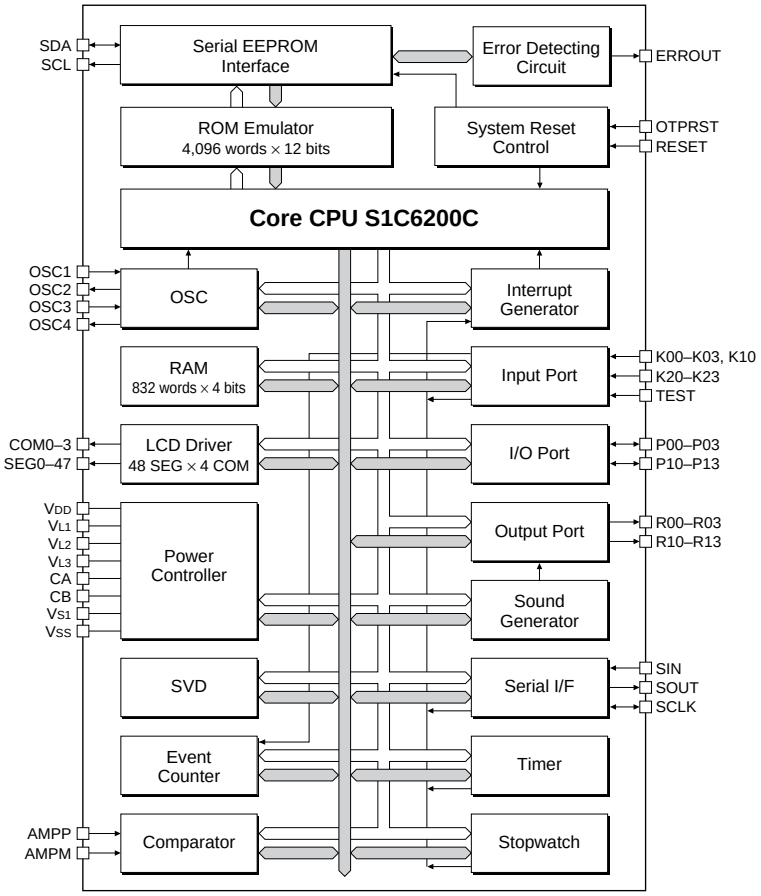
■ BLOCK DIAGRAM

S1C60N08/60L08/60A08

∗: S1C60A08 only



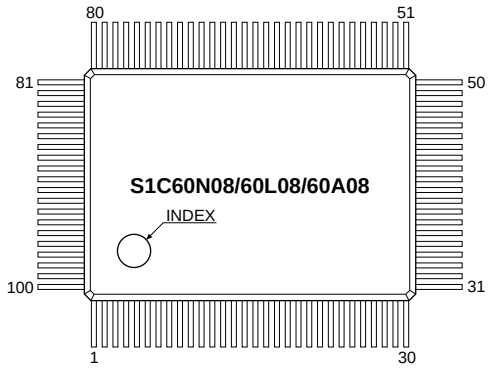
S1C60R08



■ PIN CONFIGURATION

● S1C60N08/60L08/60A08 Pin Configuration

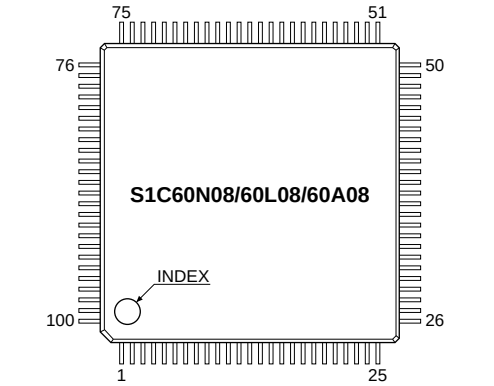
QFP5-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	21	SEG29	41	SEG10	61	K01	81	R12
2	COM0	22	SEG28	42	SEG9	62	K00	82	R11
3	SEG47	23	SEG27	43	SEG8	63	SIN	83	R10
4	SEG46	24	SEG26	44	SEG7	64	SOUT	84	R13
5	SEG45	25	SEG25	45	SEG6	65	N.C.	85	V_{SS}
6	SEG44	26	SEG24	46	SEG5	66	SCLK	86	RESET
7	SEG43	27	TEST	47	SEG4	67	P03	87	OSC4
8	SEG42	28	SEG23	48	SEG3	68	P02	88	OSC3
9	SEG41	29	SEG22	49	SEG2	69	P01	89	V_{S1}
10	SEG40	30	SEG21	50	SEG1	70	P00	90	OSC2
11	SEG39	31	SEG20	51	SEG0	71	N.C.	91	OSC1
12	SEG38	32	SEG19	52	AMPP	72	N.C.	92	V_{DD}
13	SEG37	33	SEG18	53	AMPM	73	P13	93	V_{L3}
14	SEG36	34	SEG17	54	K23	74	P12	94	V_{L2}
15	SEG35	35	SEG16	55	K22	75	P11	95	V_{L1}
16	SEG34	36	SEG15	56	K21	76	P10	96	CA
17	SEG33	37	SEG14	57	K20	77	R03	97	CB
18	SEG32	38	SEG13	58	K10	78	R02	98	N.C.
19	SEG31	39	SEG12	59	K03	79	R01	99	COM3
20	SEG30	40	SEG11	60	K02	80	R00	100	COM2

N.C. = No Connection

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG47	21	SEG27	41	SEG9	61	K00	81	R10
2	SEG46	22	SEG26	42	SEG8	62	SIN	82	R13
3	SEG45	23	SEG25	43	SEG7	63	SOUT	83	V_{SS}
4	SEG44	24	SEG24	44	SEG6	64	N.C.	84	RESET
5	SEG43	25	TEST	45	SEG5	65	SCLK	85	OSC4
6	SEG42	26	SEG23	46	SEG4	66	N.C.	86	OSC3
7	SEG41	27	SEG22	47	SEG3	67	P03	87	V_{S1}
8	SEG40	28	SEG21	48	SEG2	68	P02	88	OSC2
9	SEG39	29	SEG20	49	SEG1	69	P01	89	OSC1
10	SEG38	30	SEG19	50	SEG0	70	P00	90	V_{DD}
11	SEG37	31	SEG18	51	AMPP	71	P13	91	V_{L3}
12	SEG36	32	SEG17	52	AMPM	72	P12	92	V_{L2}
13	SEG35	33	SEG16	53	K23	73	P11	93	V_{L1}
14	SEG34	34	SEG15	54	K22	74	P10	94	CA
15	SEG33	35	SEG14	55	K21	75	R03	95	CB
16	SEG32	36	SEG13	56	K20	76	R02	96	N.C.
17	SEG31	37	SEG12	57	K10	77	R01	97	COM3
18	SEG30	38	N.C.	58	K03	78	R00	98	COM2
19	SEG29	39	SEG11	59	K02	79	R12	99	COM1
20	SEG28	40	SEG10	60	K01	80	R11	100	COM0

N.C. = No Connection

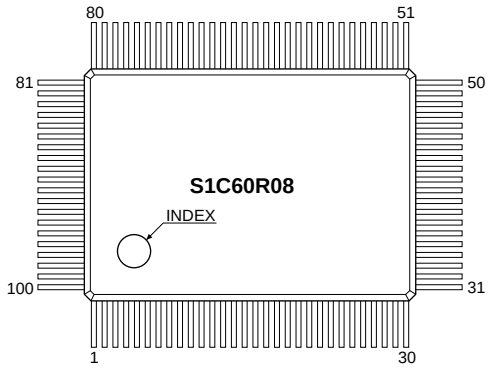
● S1C60N08/60L08/60A08 Pin Description

Pin name	Pin No.		I/O	Function
	QFP5-100	QFP15-100		
V_{DD}	92	90	(I)	Power supply pin (+)
V_{SS}	85	83	(I)	Power supply pin (-)
V_{S1}	89	87	–	Oscillation and internal logic system voltage output pin
V_{L1}	95	93	–	LCD drive voltage output pin (approx. -1.05 V or 1/2·V_{L2})
V_{L2}	94	92	–	LCD drive voltage output pin (2·V_{L1} or approx. -2.10 V)
V_{L3}	93	91	–	LCD drive voltage output pin (3·V_{L1} or 3/2·V_{L2})
CA, CB	96, 97	94, 95	–	Boost capacitor connecting pin
OSC1	91	89	I	Cryctal oscillation input pin
OSC2	90	88	O	Crystal oscillation output pin
OSC3	88	86	I	CR or ceramic oscillation input pin * (N.C. for S1C60N08 and S1C60L08)
OSC4	87	85	O	CR or ceramic oscillation output pin * (N.C. for S1C60N08 and S1C60L08)
K00–K03	62–59	61–58	I	Input port pin
K10	58	57	I	Input port pin
K20–K23	57–54	56–53	I	Input port pin
P00–P03	70–67	70–67	I/O	I/O port pin
P10–P13	76–73	74–71	I/O	I/O port pin
R00–R03	80–77	78–75	O	Output port pin
R10	83	81	O	Output port pin or BZ output pin *
R13	84	82	O	Output port pin or $\overline{BZ}$ output pin *
R11	82	80	O	Output port pin or SIOF output pin *
R12	81	79	O	Output port pin or FOUT output pin *
SIN	63	62	I	Serial interface data input pin
SOUT	64	63	O	Serial interface data output pin
SCLK	66	65	I/O	Serial interface clock input/output pin
AMPP	52	51	I	Analog comparator non-inverted input pin
AMPM	53	52	I	Analog comparator inverted input pin
SEG0–47	51–28, 26–3	50–39, 37–26, 24–1	O	LCD segment output pin or DC output pin *
COM0–3	2, 1, 100, 99	100–97	O	LCD common output pin (1/2, 1/3 or 1/4 duty are selectable *)
RESET	86	84	I	Initial reset input pin
TEST	27	25	I	Input pin for test

* Can be selected by mask option

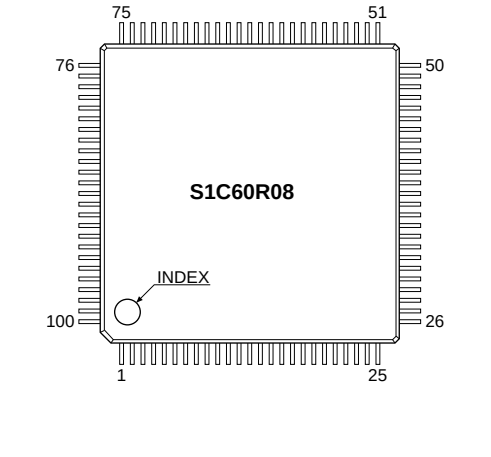
● S1C60R08 Pin Configuration

QFP5-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	21	SEG29	41	SEG10	61	K01	81	R12
2	COM0	22	SEG28	42	SEG9	62	K00	82	R11
3	SEG47	23	SEG27	43	SEG8	63	SIN	83	R10
4	SEG46	24	SEG26	44	SEG7	64	SOUT	84	R13
5	SEG45	25	SEG25	45	SEG6	65	OTPRST	85	V_{SS}
6	SEG44	26	SEG24	46	SEG5	66	SCLK	86	RESET
7	SEG43	27	TEST	47	SEG4	67	P03	87	OSC4
8	SEG42	28	SEG23	48	SEG3	68	P02	88	OSC3
9	SEG41	29	SEG22	49	SEG2	69	P01	89	V_{S1}
10	SEG40	30	SEG21	50	SEG1	70	P00	90	OSC2
11	SEG39	31	SEG20	51	SEG0	71	SCL	91	OSC1
12	SEG38	32	SEG19	52	AMPP	72	SDA	92	V_{DD}
13	SEG37	33	SEG18	53	AMPM	73	P13	93	V_{L3}
14	SEG36	34	SEG17	54	K23	74	P12	94	V_{L2}
15	SEG35	35	SEG16	55	K22	75	P11	95	V_{L1}
16	SEG34	36	SEG15	56	K21	76	P10	96	CA
17	SEG33	37	SEG14	57	K20	77	R03	97	CB
18	SEG32	38	SEG13	58	K10	78	R02	98	ERROUT
19	SEG31	39	SEG12	59	K03	79	R01	99	COM3
20	SEG30	40	SEG11	60	K02	80	R00	100	COM2

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG47	21	SEG27	41	SEG8	61	SIN	81	R10
2	SEG46	22	SEG26	42	SEG7	62	SOUT	82	R13
3	SEG45	23	SEG25	43	SEG6	63	OTPRST	83	V_{SS}
4	SEG44	24	SEG24	44	SEG5	64	SCLK	84	RESET
5	SEG43	25	TEST	45	SEG4	65	P03	85	OSC4
6	SEG42	26	SEG23	46	SEG3	66	P02	86	OSC3
7	SEG41	27	SEG22	47	SEG2	67	P01	87	V_{S1}
8	SEG40	28	SEG21	48	SEG1	68	P00	88	OSC2
9	SEG39	29	SEG20	49	SEG0	69	SCL	89	OSC1
10	SEG38	30	SEG19	50	AMPP	70	SDA	90	V_{DD}
11	SEG37	31	SEG18	51	AMPM	71	P13	91	V_{L3}
12	SEG36	32	SEG17	52	K23	72	P12	92	V_{L2}
13	SEG35	33	SEG16	53	K22	73	P11	93	V_{L1}
14	SEG34	34	SEG15	54	K21	74	P10	94	CA
15	SEG33	35	SEG14	55	K20	75	R03	95	CB
16	SEG32	36	SEG13	56	K10	76	R02	96	ERROUT
17	SEG31	37	SEG12	57	K03	77	R01	97	COM3
18	SEG30	38	SEG11	58	K02	78	R00	98	COM2
19	SEG29	39	SEG10	59	K01	79	R12	99	COM1
20	SEG28	40	SEG9	60	K00	80	R11	100	COM0

● S1C60R08 Pin Description

Pin name	Pin No.		I/O	Function
	QFP5-100	QFP15-100		
V_{DD}	92	90	(I)	Power supply pin (+)
V_{SS}	85	83	(I)	Power supply pin (-)
V_{S1}	89	87	–	Oscillation and internal logic system voltage output pin
V_{L1}	95	93	–	LCD drive voltage output pin (approx. -1.05 V or 1/2·V_{L2})
V_{L2}	94	92	–	LCD drive voltage output pin (2·V_{L1} or approx. -2.10 V)
V_{L3}	93	91	–	LCD drive voltage output pin (3·V_{L1} or 3/2·V_{L2})
CA, CB	96, 97	94, 95	–	Boost capacitor connecting pin
OSC1	91	89	I	Crystal oscillation input pin
OSC2	90	88	O	Crystal oscillation output pin
OSC3	88	86	I	CR or ceramic oscillation input pin *
OSC4	87	85	O	CR or ceramic oscillation output pin *
K00–K03	62–59	60–57	I	Input port pin
K10	58	56	I	Input port pin
K20–K23	57–54	55–52	I	Input port pin
P00–P03	70–67	68–65	I/O	I/O port pin
P10–P13	76–73	74–71	I/O	I/O port pin
R00–R03	80–77	78–75	O	Output port pin
R10	83	81	O	Output port pin or BZ output pin *
R11	82	80	O	Output port pin or SIOF output pin *
R12	81	79	O	Output port pin or FOUT output pin *
R13	84	82	O	Output port pin or $\overline{BZ}$ output pin *
SIN	63	61	I	Serial interface data input pin
SOUT	64	62	O	Serial interface data output pin
SCLK	66	64	I/O	Serial interface clock input/output pin
AMPP	52	50	I	Analog comparator non-inverted input pin
AMPM	53	51	I	Analog comparator inverted input pin
SEG0–47	51–28, 26–3	49–26, 24–1	O	LCD segment output pin or DC output pin *
COM0–3	2, 1, 100, 99	100–97	O	LCD common output pin (1/2, 1/3 or 1/4 duty are selectable *)
RESET	86	84	I	Initial reset input pin
TEST	27	25	I	Input pin for test
SCL	71	69	O	Serial EEPROM clock output pin
SDA	72	70	I/O	Serial EEPROM data input/output pin
ERROUT	98	96	O	Errout detecting singnal output for download program
OTPRST	65	63	I	Cold reset pin for re-start download program from EEPROM

* Can be selected by mask option

■ OPTION LIST

1. DEVICE TYPE
   - DEVICE TYPE ..... ☐ 1. S1C60N08 (Normal Type)
     ☐ 2. S1C60L08 (Low Power Type) (Note)
     ☐ 3. S1C60A08 (Twin Clock Type)
   - CLOCK TYPE (for Evaluation board) ☐ 1. 32 kHz ☐ 2. 38 kHz

2. OSC3 SYSTEM CLOCK (only for S1C60A08)
   ☐ 1. CR ☐ 2. Ceramic

3. MULTIPLE KEY ENTRY RESET
   - COMBINATION ..... ☐ 1. Not Use
     ☐ 2. Use K00, K01
     ☐ 3. Use K00, K01, K02
     ☐ 4. Use K00, K01, K02, K03
   - TIME AUTHORIZE ..... ☐ 1. Use ☐ 2. Not Use

4. WATCHDOG TIMER
   ☐ 1. Use ☐ 2. Not Use

5. INPUT INTERRUPT NOISE REJECTOR
   - K00–K03 ..... ☐ 1. Use ☐ 2. Not Use
   - K10 ..... ☐ 1. Use ☐ 2. Not Use
   - K20–K23 ..... ☐ 1. Use ☐ 2. Not Use

6. INPUT PORT PULL DOWN RESISTOR
   - K00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K10 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K20 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K21 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K22 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - K23 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

7. OUTPUT PORT SPECIFICATION (R00–R03)
   - R00 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - R01 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - R02 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - R03 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

8. R10 SPECIFICATION
   - OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. Buzzer Output

9. R11 SPECIFICATION
   - OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. SIO Flag

10. R12 SPECIFICATION
    - OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
    - OUTPUT TYPE ..... ☐ 1. DC Output
      ☐ 2. FOUT 32768 or 38400 [Hz]
      ☐ 3. FOUT 16384 or 19200 [Hz]
      ☐ 4. FOUT 8192 or 9600 [Hz]
      ☐ 5. FOUT 4096 or 4800 [Hz]
      ☐ 6. FOUT 2048 or 2400 [Hz]
      ☐ 7. FOUT 1024 or 1200 [Hz]
      ☐ 8. FOUT 512 or 600 [Hz]
      ☐ 9. FOUT 256 or 300 [Hz]

11. R13 SPECIFICATION
- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. Buzzer Inverted Output (R13 Control)
  ☐ 3. Buzzer Inverted Output (R10 Control)

12. I/O PORT SPECIFICATION
- P00 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P01 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P02 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P03 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P10 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P11 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P12 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P13 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

13. SIN PULL DOWN RESISTOR
☐ 1. With Resistor ☐ 2. Gate Direct

14. SOUT SPECIFICATION
☐ 1. Complementary ☐ 2. Pch-OpenDrain

15. SCLK SPECIFICATION
- PULL DOWN RESISTOR ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- LOGIC ..... ☐ 1. Positive ☐ 2. Negative

16. SIO DATA PERMUTATION
☐ 1. MSB First ☐ 2. LSB First

17. EVENT COUNTER NOISE REJECTOR
☐ 1. 2048 or 2400 [Hz] ☐ 2. 256 or 300 [Hz]

18. LCD SPECIFICATION
- BIAS SELECTION

  S1C60N08 .....
  ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V
  ☐ 2. 1/3 Bias, Regulator Not Used, LCD 3 V
  ☐ 3. 1/2 Bias, Regulator Not Used, LCD 3 V
  ☐ 4. 1/3 Bias, Regulator Not Used, LCD 4.5 V

  S1C60L08 (Note) .....
  ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V
  ☐ 2. 1/2 Bias, Regulator Not Used, LCD 3 V
  ☐ 3. 1/3 Bias, Regulator Not Used, LCD 4.5 V

  S1C60A08 .....
  ☐ 1. 1/3 Bias, Regulator Used, LCD 3 V
  ☐ 2. 1/3 Bias, Regulator Not Used, LCD 3 V
  ☐ 3. 1/2 Bias, Regulator Not Used, LCD 3 V
  ☐ 4. 1/3 Bias, Regulator Not Used, LCD 4.5 V

- DUTY SELECTION ..... ☐ 1. 1/4 Duty
  ☐ 2. 1/3 Duty
  ☐ 3. 1/2 Duty

19. SEGMENT MEMORY ADDRESS
☐ 1. 0 Page (040–06F) ☐ 2. 2 Page (240–26F)

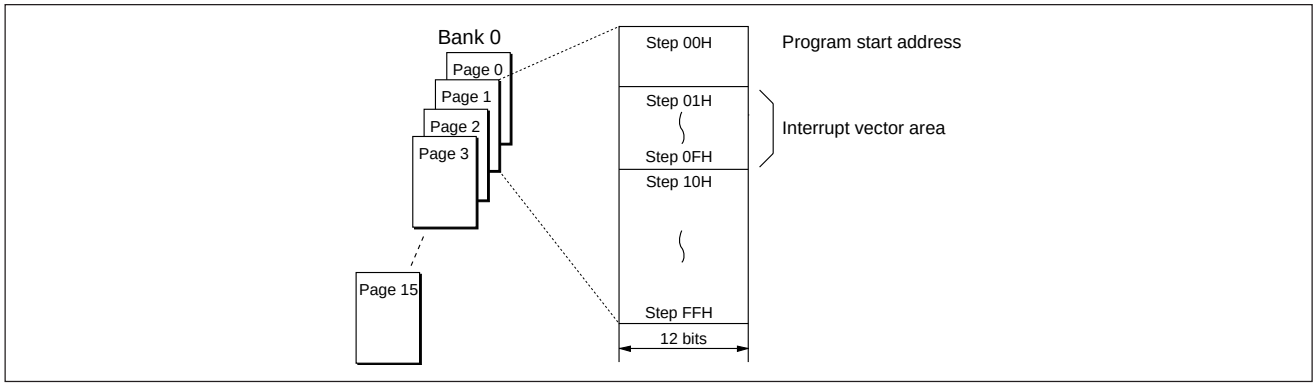
Note: The S1C60R08 does not support the S1C60L08.

■ S1C60R08 ROM EMULATOR/ROM EMULATOR PROGRAMMER

The S1C60R08 has a built-in ROM emulator, which is constructed by RAM, to emulate mask ROM. The ROM emulator is programmed from outside through the serial interface (programmer) circuit and then its data is read by the CPU. This chapter explain the ROM emulator and the Programmer circuit.

● Configuration of ROM Emulator

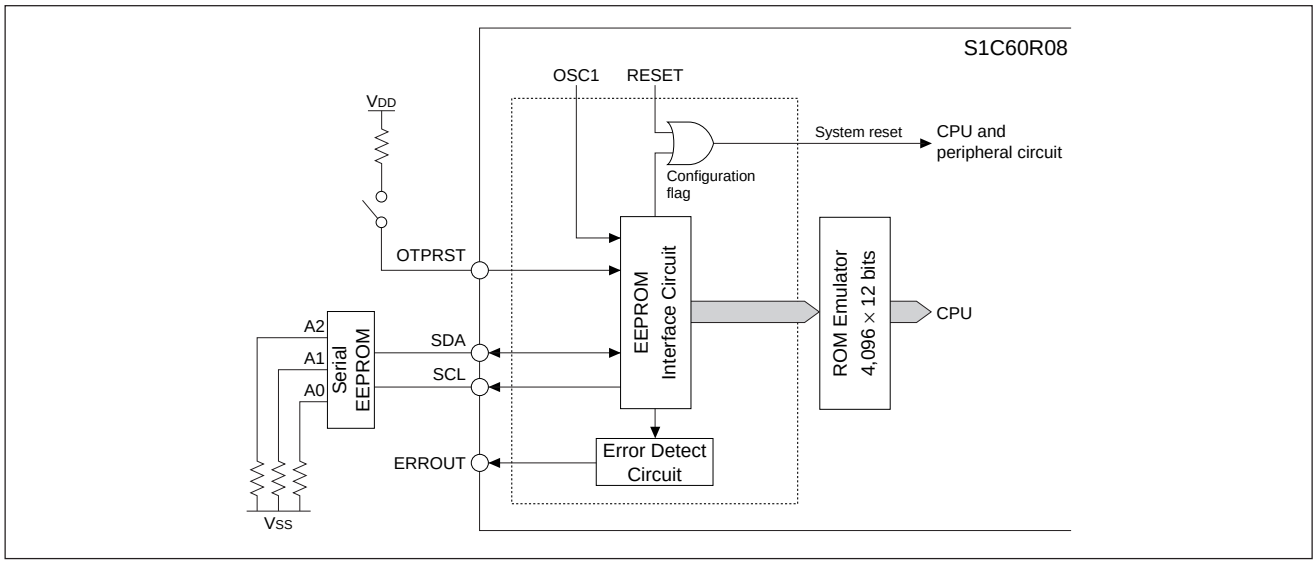
The built-in ROM emulator is the same structure with the mask ROM built-in S1C60N08. And used for loading the user-program. That has a capacity of 4,096 steps × 12 bits. The program area consists of 16 (0–15) pages × 256 (00H–FFH) steps. After initial reset, the program beginning address is set to bank 0, page 1, step 00H. The interrupt vector is allocated to page 1, steps 01H–0FH.



The ROM emulator data is downloaded from an external Serial EEPROM through the Programmer circuit. After power on or a HIGH pulse is input to the OTPRST pin, the ROM emulator data is initialized and downloading will be started.

● Configuration of ROM Emulator Programmer

The ROM emulator data is written through the Programmer. The Programmer supports data transmit/receive communication with Serial EEPROM, interface data error check and system reset signal generation.



Terminals

The Programmer uses the following input/output terminals.

SCL:	Serial EEPROM control clock output terminal
SDA:	Serial EEPROM data transmit/receive terminal
ERROUT:	Data check result output terminal
OTPRST:	Data re-loading start input terminal

● **Operation**

The S1C60R08 has two operation modes,

- Programming mode: Load the data from the Serial EEPROM
- Normal mode: Work as if the mask ROM type

The following describes how to operate the S1C60R08.

1) Make an application software.
2) Convert the software to the Serial EEPROM format with winedg in the S1C60R08 package.
3) Write the program which is converted to the Serial EEPROM format to the Serial EEPROM.
4) Set up the S1C60R08, the Serial EEPROM and the other peripheral components on the user target application. (The example is described in "BASIC EXTERNAL CONNECTION DIAGRAM".)
5) The application power on.
6) The S1C60R08 enters to the Programming mode, and starts data loading from the Serial EEPROM to the built-in ROM emulator automatically. In the loading, internal circuit is kept as system reset condition except the Programmer. And data error checking is done at the same time.
7) If the data error happens, the ERROUT pin goes HIGH level and data loading is terminated.
8) If the data has loaded without any error, the S1C60R08 enters to the Normal mode automatically. Then the CPU read the ROM emulator data as the instruction and start to run as if the mask ROM type.
9) If you want to re-load the data, input a HIGH pulse to the OTPRST pin. Then the S1C60R08 enters to Programming mode and starts re-loading.

■ SUMMARY OF NOTES

● **Target Type for S1C60N08 Series**

The S1C60N08 has 3 types (S1C60N08, S1C60A08 and S1C60L08).
In these models, the S1C60R08 supports the following 2 types as the ROM emulator model.

S1C60N08 V_{DD} = 3.0 V (Typ.), OSC1
S1C60A08 V_{DD} = 3.0 V (Typ.), OSC1/OSC3

Refer the "S1C60N08/60R08 Technical Manual".

● **Mask/Segment Option**

The S1C60R08 can load ROM emulator data. But cannot load the mask option and segment option. Therefore customer must make the function option data and segment option data by the S1C60R08 development tool at first. Then send the data to SEIKO EPSON and order the mask. SEIKO EPSON makes the S1C60R08 with a customized option according to this request.

● **Serial EEPROM**

The external Serial EEPROM is necessary for programming the ROM emulator data, and this component is recommended.

Recommended component: AK6010A/12A (AKM)
M24C64/32 (SGS-THOMSON)
BR24C64 (ROHM)
24AA64 (Microchip)

Note: Use larger EEPROM than program memory size.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

S1C60N08/60A08/60R08

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package.

S1C60L08

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package.

● Recommended Operating Conditions

S1C60N08

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

S1C60L08

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.7	-1.5	-1.1	V
		V_{DD}=0V, with software control *1	-1.7	-1.5	-0.9 *2	V
		V_{DD}=0V, when analog comparator is used	-1.7	-1.5	-1.2	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

*1: When switching to heavy load protection mode.
*2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

S1C60A08/60R08

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-2.2 *1	V
Oscillation frequency (1)	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%, V_{SS}=-2.2 to -3.5V	50	500	600	kHz

*1: -1.8V when the S1C60R08 is used as the S1C60N08.

● DC Characteristics

S1C60N08/60A08/60R08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23, P00–03, P10–13 SIN, (SDA) *1	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST, (OTPRST) *1	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23, P00–03, P10–13 SIN, (SDA) *1	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST, (OTPRST) *1	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull-down	K00–03, K10, K20–23, P00–03, P10–13 SIN, SCLK, AMPP, AMPM (SDA) *1	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull-down	K00–03, K10, K20–23 SIN, SCLK	4		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull-down	P00–03, P10–13, RESET, TEST (OTPRST) *1	25		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, K20–23, P00–03, P10–13 SIN, SCLK, AMPP, AMPM, RESET, TEST (OTPRST), (SDA) *1	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R10, R11, R13			-1.8	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R00–03, R12, P00–03, P10–13, SOUT SCLK, (SDA), (ERROUT), (SCL) *1			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R10, R11, R13	6.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R00–03, R12, P00–03, P10–13, SOUT SCLK, (SDA), (ERROUT), (SCL) *1	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·V_{SS}	SEG0–47			-200	µA
	I_{OL5}	V_{OL5}=0.9·V_{SS}		200			µA

*1: ( ) indicate the S1C60R08 pins.

S1C60L08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23, P00–03, P10–13 SIN	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23, P00–03, P10–13 SIN	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull-down	K00–03, K10, K20–23, P00–03, P10–13 SIN, SCLK AMPP, AMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull-down	K00–03, K10, K20–23 SIN, SCLK	2		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull-down	P00–03, P10–13 RESET, TEST	12		60	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, K20–23, P00–03, P10–13 SIN, SCLK, AMPP, AMPM RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R10, R11, R13			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R10, R11, R13	1400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·V_{SS}	SEG0–47			-100	µA
	I_{OL5}	V_{OL5}=0.9·V_{SS}		100			µA

● Analog Circuit Characteristics and Current Consumption

S1C60N08 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.0	µA
		During operation *2			2.2	4.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

S1C60N08 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		10	20	µA
		During operation *2			12	25	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

S1C60L08 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V V_{IM}=V_{IP}±30mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.0	µA
		During operation *2			2.2	4.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

S1C60L08 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.85	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V V_{IM}=V_{IP}±30mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			8.5	15	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

S1C60A08 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.1	2.0	µA
		During operation *2			3.0	5.0	µA
		During operation at 500kHz *2			50	70	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

S1C60A08 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			8.5	15	µA
		During operation at 500kHz *2			55	75	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

S1C60R08 (Normal Operating Mode) Target: S1C60N08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.0	µA
		During operation *2			6.5	9.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

S1C60R08 (Heavy Load Protection Mode) Target: S1C60N08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			11.5	20	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

S1C60R08 (Normal Operating Mode) Target: S1C60A08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.1	2.0	µA
		During operation *2			7.5	10	µA
		During operation at 500kHz *2			115	150	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

S1C60R08 (Heavy Load Protection Mode) Target: S1C60A08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			12.5	20	µA
		During operation at 500kHz *2			120	160	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

● Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, boad pattern). Use the following characteristics are as reference values.

S1C60N08/60R08 (OSC1 Crystal Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: Q13MC146, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-1.8 to -3.5V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

S1C60L08 (OSC1 Crystal Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: Q13MC146, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-1.1 (-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-1.1 (-0.9)*1 to -1.7V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-1.7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

*1: Parentheses indicate value for operation in heavy load protection mode.

S1C60A08 (OSC1 Crystal Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: Q13MC146, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-2.2 to -3.5V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

S1C60A08/60R08 (OSC3 CR Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	480kHz	30	%
Oscillation start voltage	Vsta	(V_{SS})	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			3	msec
Oscillation stop voltage	Vstp	(V_{SS})	-2.2			V

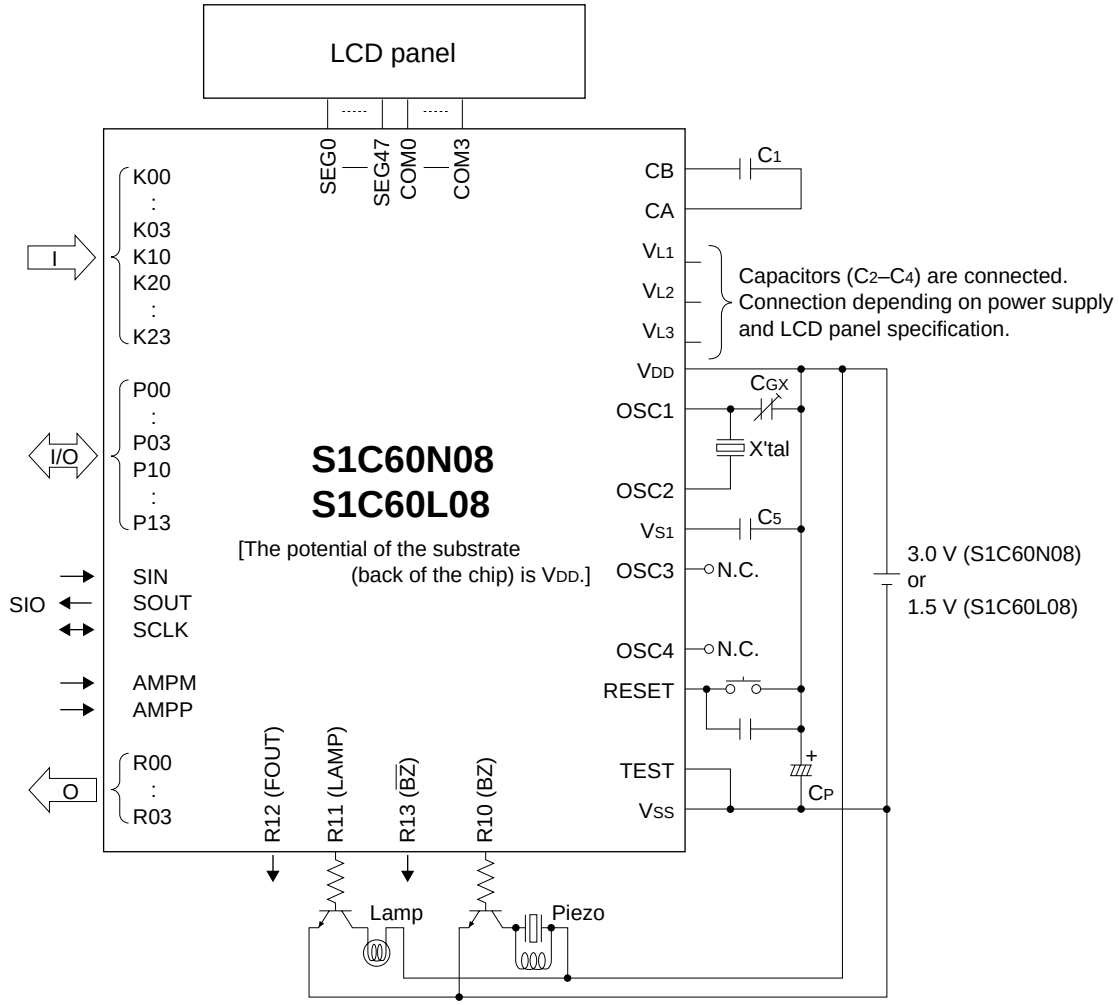
S1C60A08/60R08 (OSC3 Ceramic Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Ceramic oscillator: 500kHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

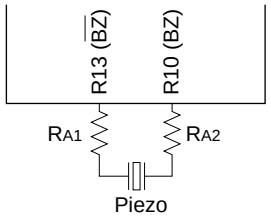
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{SS})	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			5	msec
Oscillation stop voltage	Vstp	(V_{SS})	-2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

S1C60N08 and S1C60L08



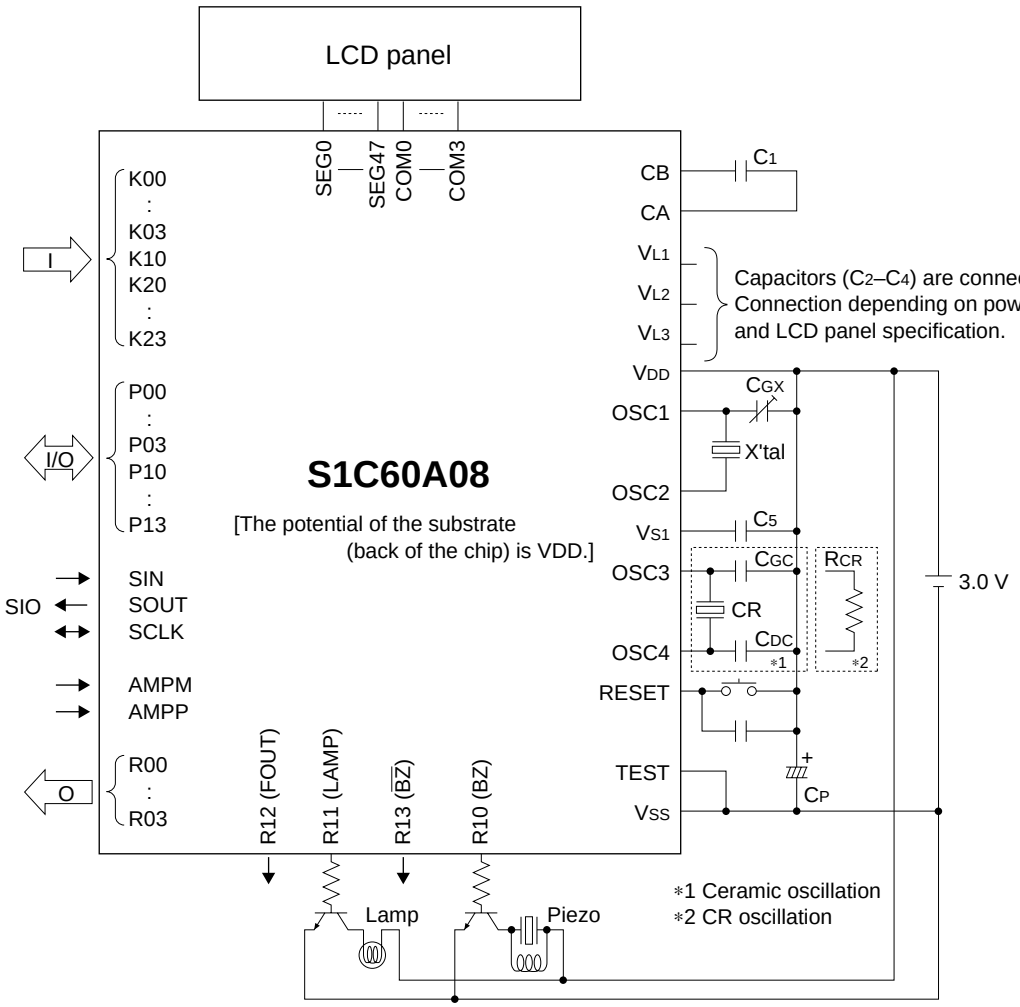
X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω



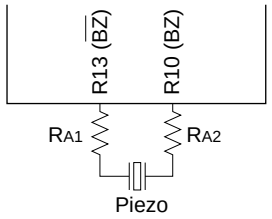
When the piezoelectric buzzer is driven directly

Note: The above tables are simply an example, and are not guaranteed to work.

S1C60A08



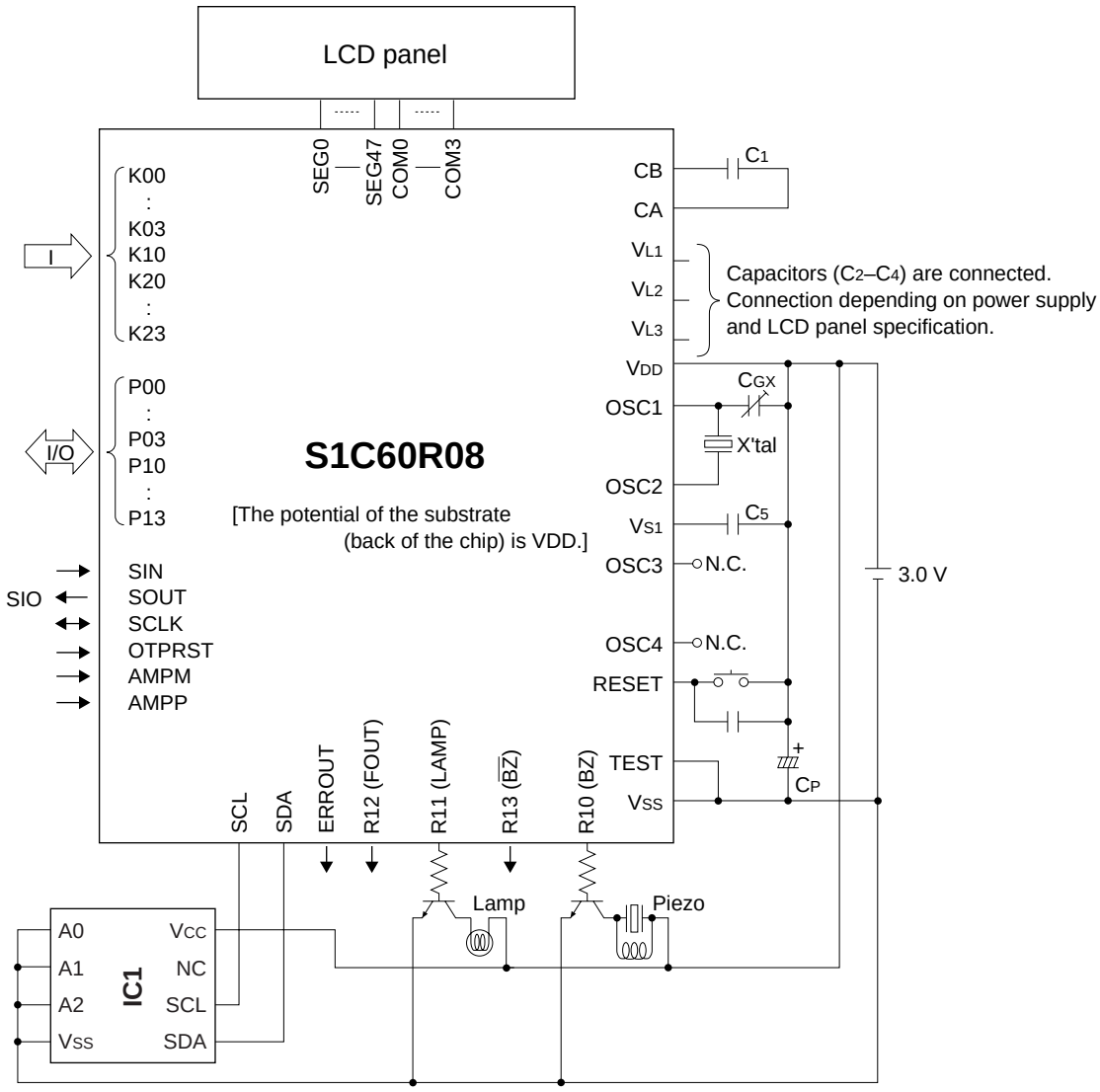
X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	500 kHz
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for CR oscillation	82 kΩ
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω



When the piezoelectric buzzer is driven directly

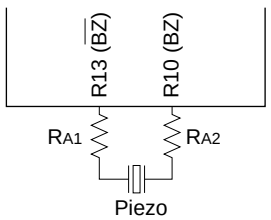
Note: The above tables are simply an example, and are not guaranteed to work.

S1C60R08 (Target for S1C60N08)



X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz
C_{GX}	Trimmer capacitor	5–25 pF
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω
IC1	Serial EEPROM	*

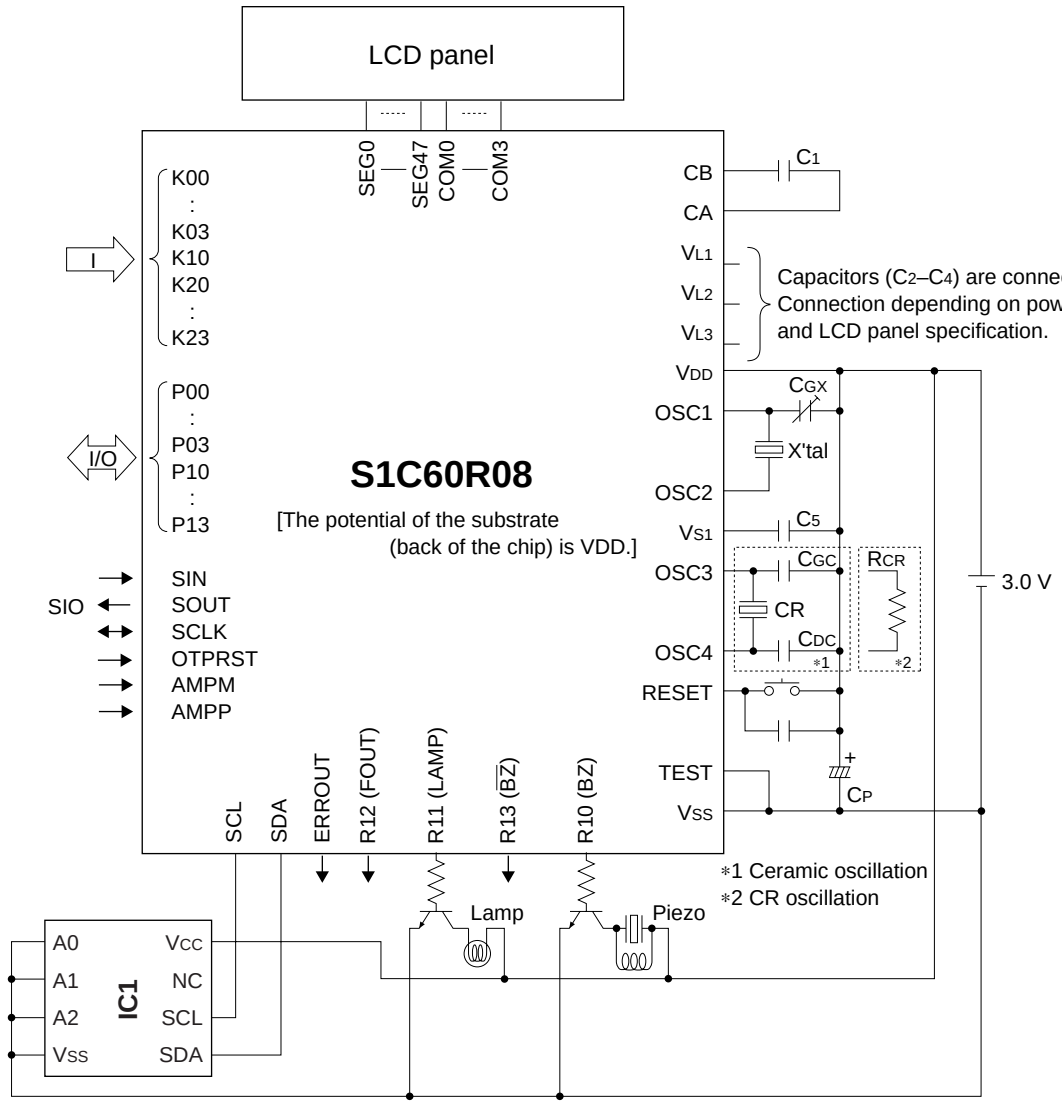
*: See "Serial EEPROM"



When the piezoelectric buzzer is driven directly

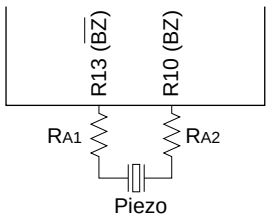
Note: The above tables are simply an example, and are not guaranteed to work.

S1C60R08 (Target for S1C60A08)



X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	500 kHz
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for CR oscillation	82 kΩ
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω
IC1	Serial EEPROM	*

*: See "Serial EEPROM"

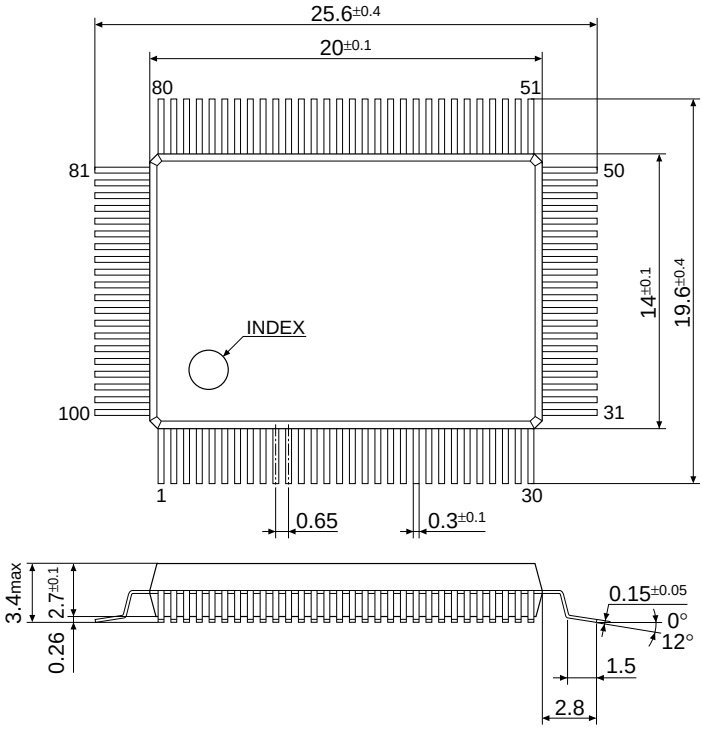


When the piezoelectric buzzer is driven directly

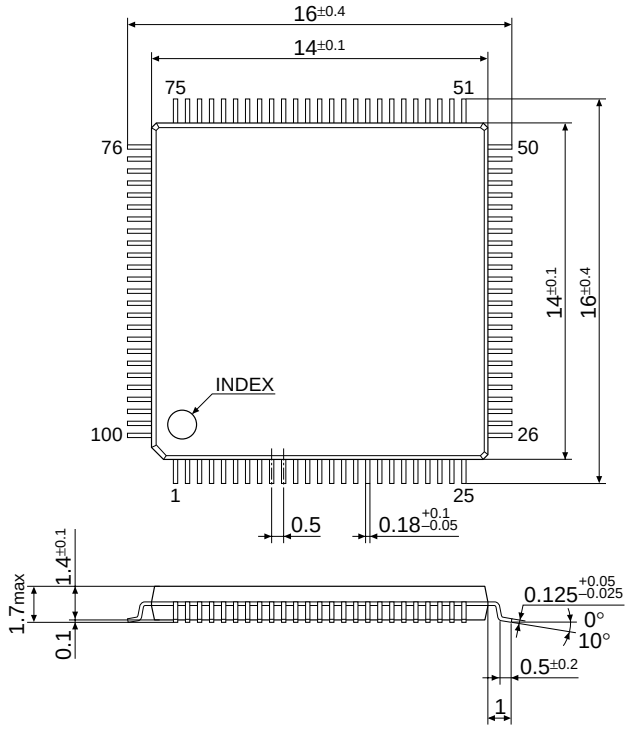
Note: The above tables are simply an example, and are not guaranteed to work.

■ PACKAGE

Plastic QFP5-100pin



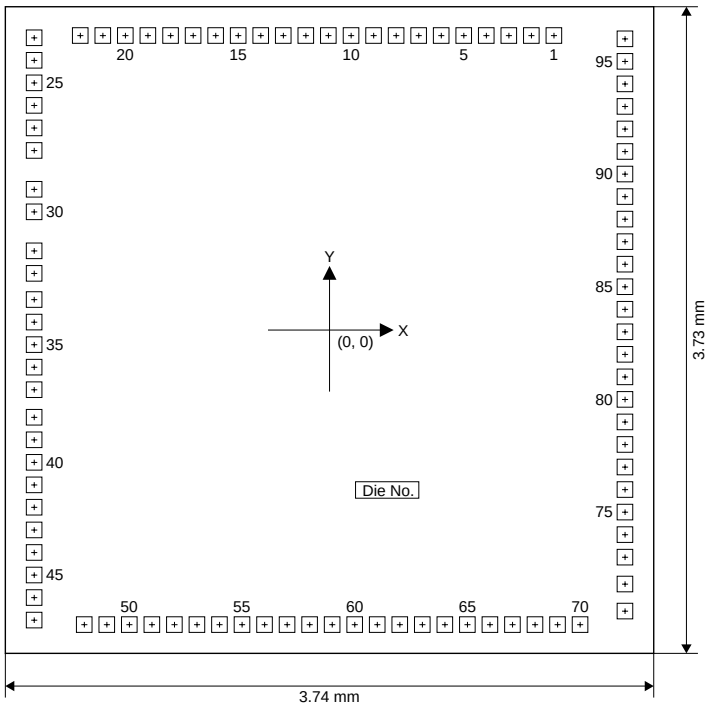
Plastic QFP15-100pin



Unit: mm

■ PAD LAYOUT

● S1C60N08/60L08/60A08 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 95 µm

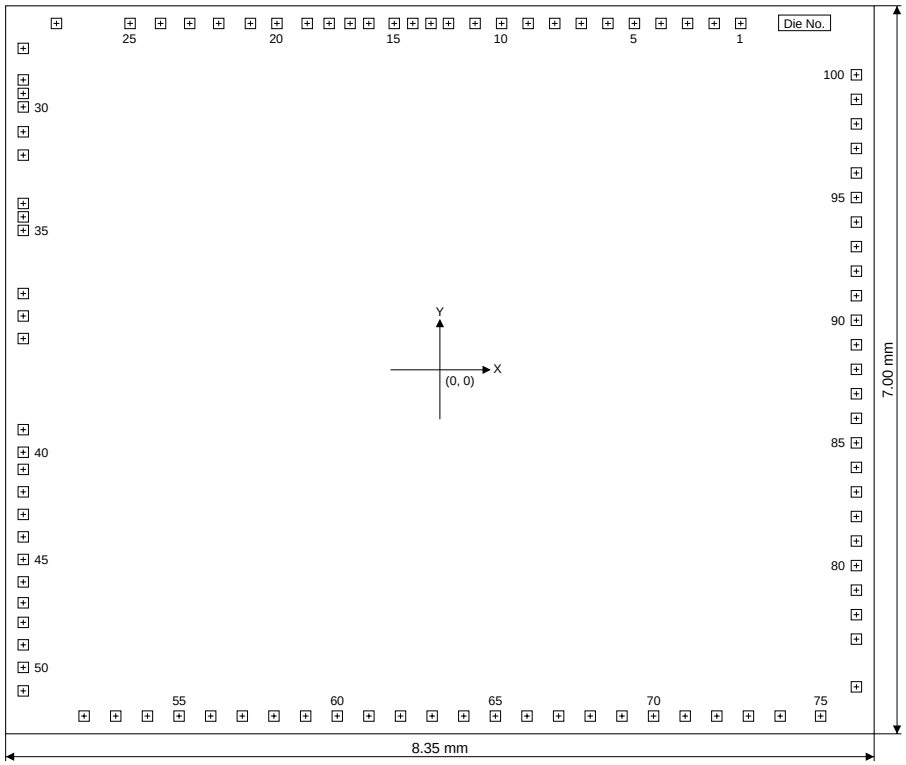
● S1C60N08/60L08/60A08 Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	AMPP	1,294	1,699	33	OSC4 *	-1,704	176	65	SEG30	795	-1,699
2	AMPM	1,164	1,699	34	OSC3 *	-1,704	46	66	SEG29	925	-1,699
3	K23	1,034	1,699	35	V_{S1}	-1,704	-84	67	SEG28	1,055	-1,699
4	K22	904	1,699	36	OSC2	-1,704	-214	68	SEG27	1,185	-1,699
5	K21	774	1,699	37	OSC1	-1,704	-344	69	SEG26	1,315	-1,699
6	K20	644	1,699	38	V_{DD}	-1,704	-503	70	SEG25	1,445	-1,699
7	K10	514	1,699	39	V_{L3}	-1,704	-633	71	SEG24	1,704	-1,621
8	K03	384	1,699	40	V_{L2}	-1,704	-763	72	TEST	1,704	-1,465
9	K02	254	1,699	41	V_{L1}	-1,704	-893	73	SEG23	1,704	-1,310
10	K01	124	1,699	42	CA	-1,704	-1,022	74	SEG22	1,704	-1,180
11	K00	-7	1,699	43	CB	-1,704	-1,153	75	SEG21	1,704	-1,050
12	SIN	-137	1,699	44	COM3	-1,704	-1,283	76	SEG20	1,704	-920
13	SOUT	-267	1,699	45	COM2	-1,704	-1,413	77	SEG19	1,704	-790
14	SCLK	-397	1,699	46	COM1	-1,704	-1,543	78	SEG18	1,704	-660
15	P03	-527	1,699	47	COM0	-1,704	-1,673	79	SEG17	1,704	-530
16	P02	-657	1,699	48	SEG47	-1,415	-1,699	80	SEG16	1,704	-400
17	P01	-787	1,699	49	SEG46	-1,285	-1,699	81	SEG15	1,704	-270
18	P00	-917	1,699	50	SEG45	-1,155	-1,699	82	SEG14	1,704	-140
19	P13	-1,048	1,699	51	SEG44	-1,025	-1,699	83	SEG13	1,704	-10
20	P12	-1,178	1,699	52	SEG43	-895	-1,699	84	SEG12	1,704	120
21	P11	-1,308	1,699	53	SEG42	-765	-1,699	85	SEG11	1,704	250
22	P10	-1,438	1,699	54	SEG41	-635	-1,699	86	SEG10	1,704	380
23	R03	-1,704	1,686	55	SEG40	-505	-1,699	87	SEG9	1,704	510
24	R02	-1,704	1,556	56	SEG39	-375	-1,699	88	SEG8	1,704	640
25	R01	-1,704	1,426	57	SEG38	-245	-1,699	89	SEG7	1,704	770
26	R00	-1,704	1,296	58	SEG37	-115	-1,699	90	SEG6	1,704	900
27	R12	-1,704	1,166	59	SEG36	15	-1,699	91	SEG5	1,704	1,030
28	R11	-1,704	1,036	60	SEG35	145	-1,699	92	SEG4	1,704	1,160
29	R10	-1,704	812	61	SEG34	275	-1,699	93	SEG3	1,704	1,290
30	R13	-1,704	682	62	SEG33	405	-1,699	94	SEG2	1,704	1,420
31	V_{SS}	-1,704	457	63	SEG32	535	-1,699	95	SEG1	1,704	1,550
32	RESET	-1,704	327	64	SEG31	665	-1,699	96	SEG0	1,704	1,680

*: S1C60A08 only

● S1C60R08 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 95 µm

● S1C60R08 Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	AMPP	2,893	3,330	35	REST	-4,005	1,340	69	SEG30	1,751	-3,330
2	AMPM	2,638	3,330	36	OSC4	-4,005	733	70	SEG29	2,055	-3,330
3	K23	2,382	3,330	37	OSC3	-4,005	517	71	SEG28	2,359	-3,330
4	K22	2,127	3,330	38	V_{S1}	-4,005	300	72	SEG27	2,663	-3,330
5	K21	1,871	3,330	39	OSC2	-4,005	-576	73	SEG26	2,967	-3,330
6	K20	1,616	3,330	40	OSC1	-4,005	-793	74	SEG25	3,272	-3,330
7	K10	1,360	3,330	41	V_{DD}	-4,005	-958	75	SEG24	3,661	-3,330
8	K03	1,105	3,330	42	V_{L3}	-4,005	-1,174	76	TEST	4,005	-3,049
9	K02	849	3,330	43	V_{L2}	-4,005	-1,391	77	SEG23	4,005	-2,590
10	K01	594	3,330	44	V_{L1}	-4,005	-1,607	78	SEG22	4,005	-2,355
11	K00	339	3,330	45	CA	-4,005	-1,824	79	SEG21	4,005	-2,119
12	SIN	83	3,330	46	CB	-4,005	-2,040	80	SEG20	4,005	-1,883
13	SOUT	-85	3,330	47	ERROUT	-4,005	-2,241	81	SEG19	4,005	-1,647
14	OTPRST	-260	3,330	48	COM3	-4,005	-2,429	82	SEG18	4,005	-1,411
15	SCLK	-438	3,330	49	COM2	-4,005	-2,645	83	SEG17	4,005	-1,175
16	P03	-683	3,330	50	COM1	-4,005	-2,862	84	SEG16	4,005	-939
17	P02	-863	3,330	51	COM0	-4,005	-3,088	85	SEG15	4,005	-703
18	P01	-1,064	3,330	52	SEG47	-3,420	-3,330	86	SEG14	4,005	-467
19	P00	-1,275	3,330	53	SEG46	-3,116	-3,330	87	SEG13	4,005	-231
20	SCL	-1,566	3,330	54	SEG45	-2,811	-3,330	88	SEG12	4,005	4
21	SDA	-1,821	3,330	55	SEG44	-2,507	-3,330	89	SEG11	4,005	240
22	P13	-2,126	3,330	56	SEG43	-2,203	-3,330	90	SEG10	4,005	476
23	P12	-2,405	3,330	57	SEG42	-1,899	-3,330	91	SEG9	4,005	712
24	P11	-2,685	3,330	58	SEG41	-1,595	-3,330	92	SEG8	4,005	948
25	P10	-2,978	3,330	59	SEG40	-1,290	-3,330	93	SEG7	4,005	1,184
26	R03	-3,686	3,330	60	SEG39	-986	-3,330	94	SEG6	4,005	1,420
27	R02	-4,005	3,090	61	SEG38	-682	-3,330	95	SEG5	4,005	1,656
28	R01	-4,005	2,787	62	SEG37	-378	-3,330	96	SEG4	4,005	1,892
29	R00	-4,005	2,657	63	SEG36	-74	-3,330	97	SEG3	4,005	2,128
30	R12	-4,005	2,527	64	SEG35	230	-3,330	98	SEG2	4,005	2,364
31	R11	-4,005	2,288	65	SEG34	534	-3,330	99	SEG1	4,005	2,600
32	R10	-4,005	2,064	66	SEG33	838	-3,330	100	SEG0	4,005	2,836
33	R13	-4,005	1,599	67	SEG32	1,142	-3,330				
34	V_{SS}	-4,005	1,470	68	SEG31	1,446	-3,330				

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