Preliminary

MTC8104M32-xx2A1-01

DRAM CARD

DESCRIPTION

The MTC8104M32-xx2A1-01 is a 4M-byte dynamic RAM card composed of 1M-word × 32-bit, being a 88-pin 2-piece type card proposed by the DRAM card guide-line of JEIDA. This provides a built-in buffer IC together with the DRAM device.

FEATURES

- 1,048,576-word × 32-bit Organization
- Buffer built-in IC
- Card Size : 85.6 (Length) × 54.0 (Width) × 3.3 (Thickness) [mm]
- Connecter : 88 pins 2 pieces
- Power Supply Voltage : Single 5 [V] supply, ±5% tolerance
- Input : $V_{IH} \geq 2.4$ [V], $V_{IL} \leq 0.8$ [V]
- Output : TTL compatible/3-state
- Refresh : 1024 cycles /128ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh capability
- PD Pin (Presence Detect Pin)

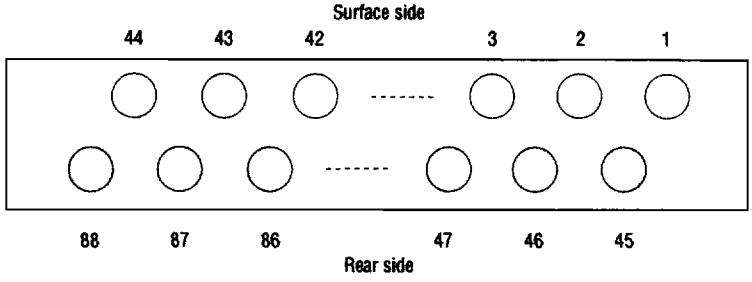
	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1
MTC8104M32-702A1-01	NC	NC	G	NC	G	G	NC	G
MTC8104M32-802A1-01	NC	G	NC	NC	G	G	NC	G
MTC8104M32-102A1-01	NC	G	G	NC	G	G	NC	G

"NC" indicates that PD pin is an open state in the card and "G" indicates that it is connected to GND.

PRODUCT FAMILY

Family	Access Time			Power Consumption	
	t_{RAC}	t_{AA}	t_{CAC}	Operating	Standby (MOS)
MTC8104M32-702A1-01	70ns	45ns	30ns	4200mW	9.5mW
MTC8104M32-802A1-01	80ns	50ns	30ns	3780mW	9.5mW
MTC8104M32-102A1-01	100ns	60ns	35ns	3360mW	9.5mW

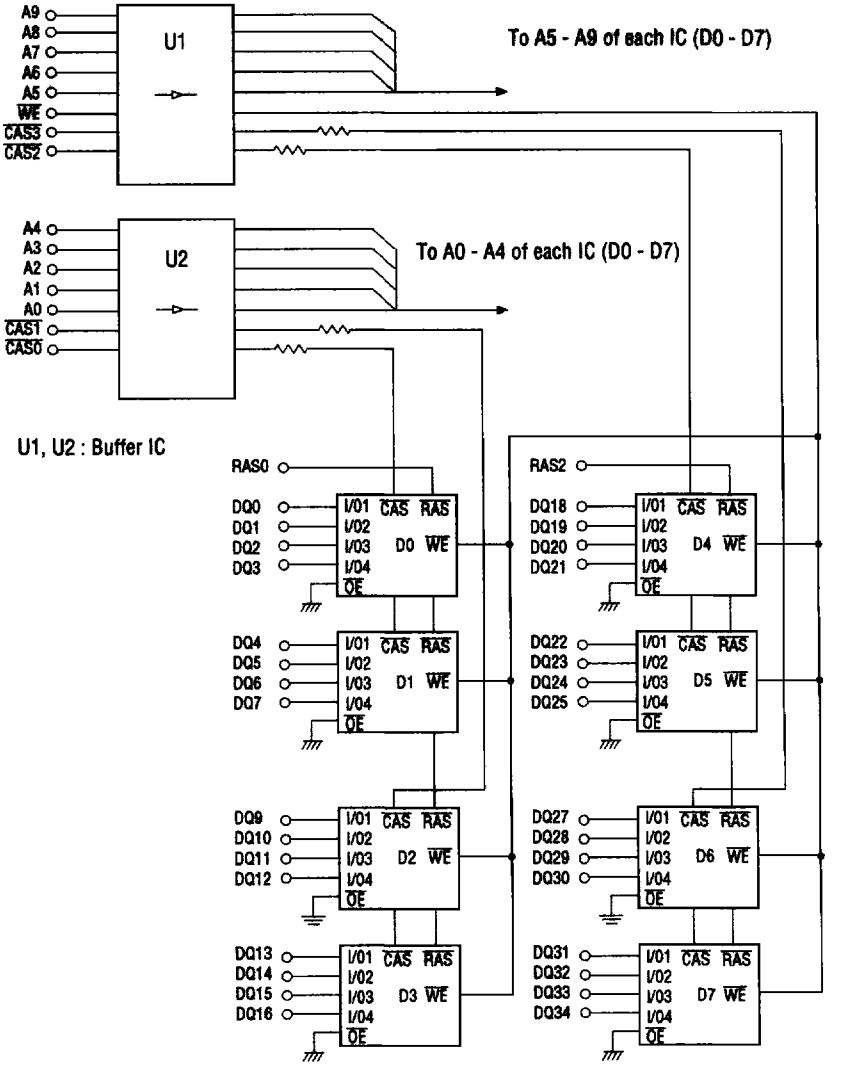
PIN CONFIGURATION



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	31	NC	61	A9
2	DQ0	32	NC	62	NC
3	DQ1	33	NC	63	GND
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	V_{CC}	67	GND
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	V_{CC}	39	DQ12	69	NC
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1
12	NC	42	DQ15	72	PD3
13	A0	43	DQ16	73	GND
14	A2	44	GND	74	PD5
15	V_{CC}	45	GND	75	PD7
16	A4	46	DQ18	76	PD8
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	NC
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	NC	84	DQ31
25	NC	55	NC	85	DQ32
26	$\overline{RAS2}$	56	GND	86	DQ33
27	V_{CC}	57	A1	87	DQ34
28	PD2	58	A3	88	GND
29	PD4	59	A5		
30	PD6	60	A7		

Notes:
- DQn : Data Bus (Input and Output)
- A0 - A9 : Address Input
- $\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe Input
- $\overline{CAS0}$ - $\overline{CAS3}$: Column Address Strobe Input
- PD1 - PD8 : Presence Detect Pin

BLOCK DIAGRAM



D0 - D7 : MSM514400BL

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Pin Voltage	V_T	Ta = 25°C	−0.5 to 7.0	V
Short Circuit Output Current	I_{OS}	Ta = 25°C	50	mA
Operating Temperature	T_{opr}	—	0 to 55	°C
Storage Temperature	T_{stg}	—	−20 to 65	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 55°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.
Power Supply Voltage	V_{CC}	—	4.75	5.0	5.25	V
	V_{SS}	—	0	0	0	V
Input High Voltage	V_{IH}	—	2.4	—	V_{CC}	V
Input Low Voltage	V_{IL}	—	0	—	0.8	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 5V ± 5%, Ta = 0 to 55°C)

Parameter	Symbol	Condition		MTC8104M32 -702A1-01		MTC8104M32 -802A1-01		MTC8104M32 -102A1-01		Unit	Note
				Min.	Max.	Min.	Max.	Min.	Max.		
Input Leakage Current (Except $\overline{RAS}$)	I_{LI1}	0V ≤ V_I ≤ V_{CC} All other pins not under test=0V		−10	10	−10	10	−10	10	µA	
Input Leakage Current ($\overline{RAS}$)	I_{LI2}	0V ≤ V_I ≤ V_{CC} All other pins not under test = 0V		−40	40	−40	40	−40	40	µA	
Output Leakage Current	I_{LO}	DQn = disable 0V ≤ V_O ≤ V_{CC}		−10	10	−10	10	−10	10	µA	
Output High Voltage	V_{OH}	I_{OH}=−5.0mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL}=4.2mA		0	0.4	0	0.4	0	0.4	V	
Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$ $\overline{CAS}$ cycling t_{RC} = min		−	800	−	720	−	640	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH}	TTL	−	16.2	−	16.2	−	16.2	mA	
		DQn = H_Z	MOS	−	1.8	−	1.8	−	1.8		
Power Supply Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min		−	800	−	720	−	640	mA	1, 2
Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling		−	800	−	720	−	640	mA	1, 2
Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = min		−	650	−	570	−	490	mA	1,3

Notes: 1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, $\overline{WE}$)	C_{IN1}	—	15	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{IN2}	—	15	pF
Input Capacitance ($\overline{RAS0}$,$\overline{RAS2}$)	C_{IN3}	—	43	pF
Output Capacitance (DQn)	C_{OUT}	—	18	pF

AC Characteristics (1/2)

(Vcc = 5V ± 5%, Ta = 0 to 55°C) Note 1, 2, 3

Parameter	Symbol	MTC8104M32 -702A1-01		MTC8104M32 -802A1-01		MTC8104M32 -102A1-01		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	130	–	150	–	180	–	ns	
Fast Page Mode Cycle Time	t_{PC}	55	–	60	–	65	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	4, 5
Access Time from $\overline{CAS}$	t_{CAC}	–	30	–	30	–	35	ns	4, 5
Access Time from Column Address	t_{AA}	–	45	–	50	–	60	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	–	50	–	55	–	60	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Output Turn-off Delay Time	t_{OFF}	0	30	0	30	0	30	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	–	128	–	128	–	128	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10K	80	10K	100	10K	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	30	–	30	–	35	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10K	20	10K	25	10K	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$, $\overline{RAS}$ Precharge Time	t_{CRP}	15	–	15	–	15	–	ns	
$\overline{RAS}$, $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	65	ns	5
$\overline{RAS}$, Column Address Delay Time	t_{RAD}	15	25	15	30	20	40	ns	6
Row Address Set-up Time	t_{ASR}	10	–	10	–	10	–	ns	
Row Address Hold Time	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Set-up Time	t_{ASC}	5	–	5	–	5	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	55	–	60	–	75	–	ns	
Column Address, $\overline{RAS}$ Lead Time	t_{RAL}	45	–	50	–	60	–	ns	
Read Command Set-up Time	t_{RCS}	5	–	5	–	5	–	ns	
Read Command Hold Time	t_{RCH}	5	–	5	–	5	–	ns	8
Read Command Hold Time from $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	8
Write Command Set-up Time	t_{WCS}	5	–	5	–	5	–	ns	
Write Command Hold Time	t_{WCH}	20	–	20	–	25	–	ns	

AC Characteristics (2/2)

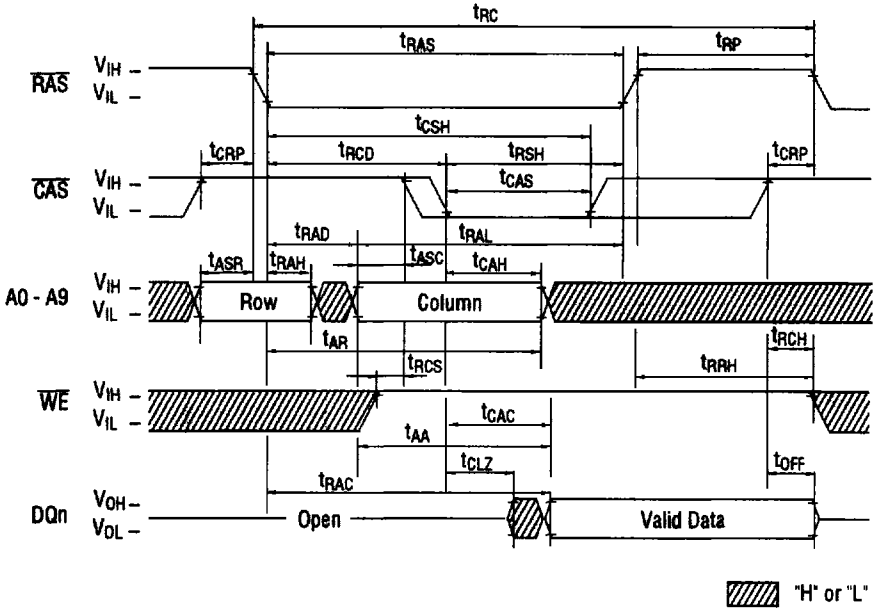
(V_{CC} = 5V ± 5%, Ta = 0 to 55°C) Note 1, 2, 3

Parameter	Symbol	MTC8104M32 -702A1-01		MTC8104M32 -802A1-01		MTC8104M32 -102A1-01		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WP}	20	–	20	–	25	–	ns	
Data Input Set-up Time	t_{DS}	10	–	10	–	10	–	ns	
Data Input Hold Time	t_{DH}	15	–	15	–	20	–	ns	
Data Input Hold Time from $\overline{RAS}$	t_{DHR}	55	–	60	–	75	–	ns	
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CSR}	20	–	20	–	20	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{WE}$, $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{WRP}	20	–	20	–	20	–	ns	
$\overline{WE}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{WRH}	10	–	10	–	10	–	ns	

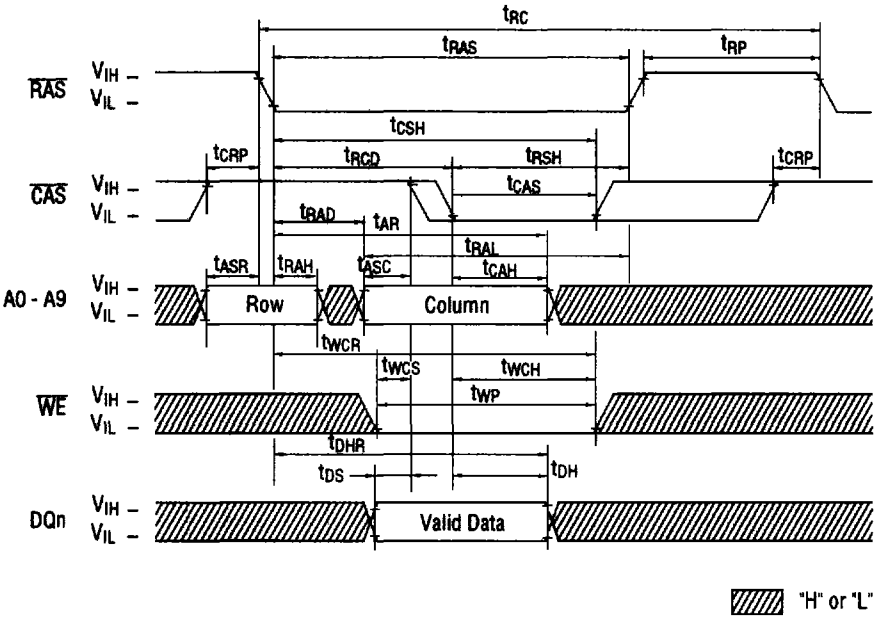
Notes:
1. An initial pause of 200µs is required after V_{CC} achieves to the specified voltage since power-up and is followed by a minimum of 8 refresh cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle)
2. The AC characteristics assume t_T = 5ns.
3. The input refresh levels for timing regulation are V_{IH} (min.) and V_{IL} (max.). Transition time (t_T) is a time to be transited between V_{IH} and V_{IL}.
4. Measured with a load circuit equipment to 2TTL loads and 100PF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{OFF} (max.) defined the time at which the output achieves the open circuit condition.
8. If either t_{RRH} or t_{RCH} is satisfied, a write operation is not executed.

TIMING WAVEFORM

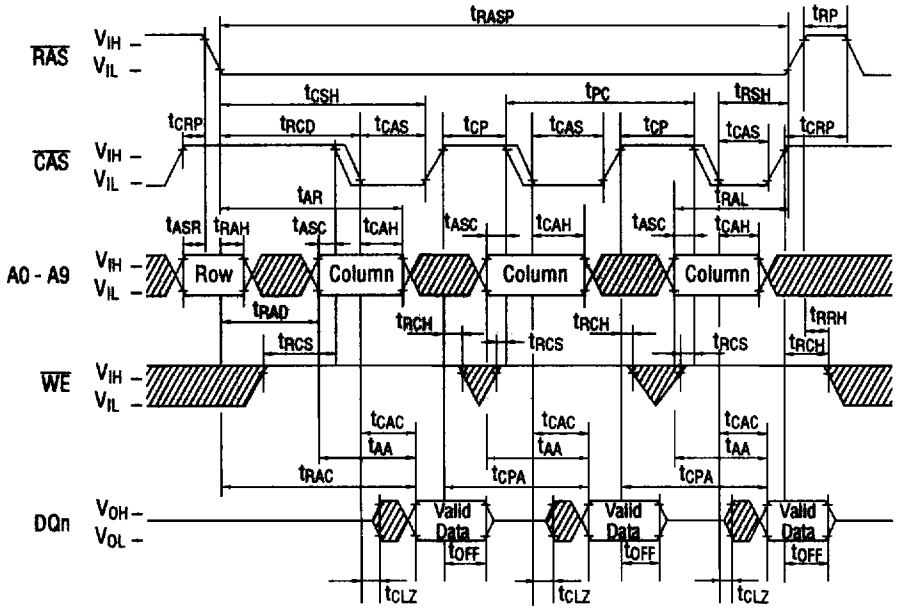
Read Cycle



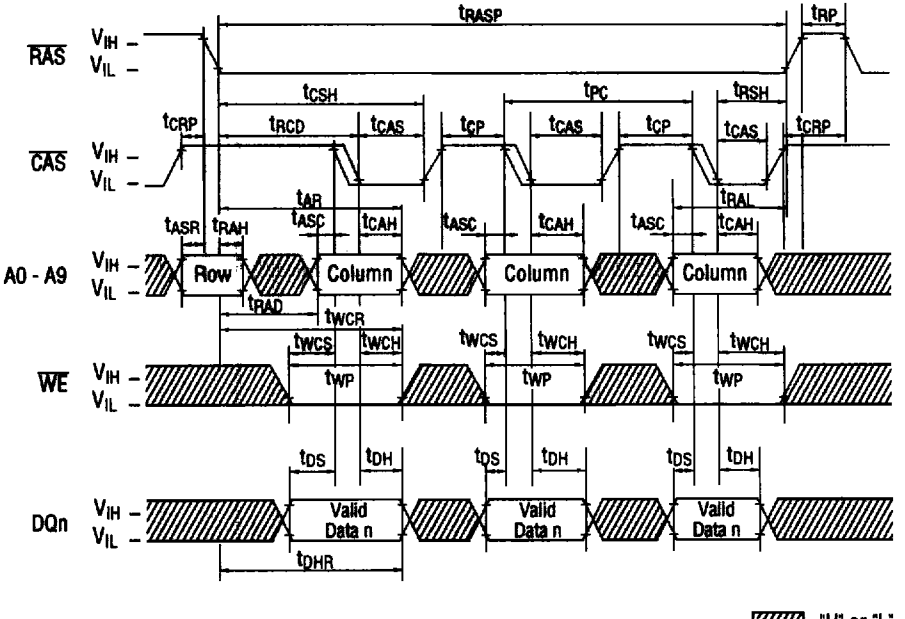
Write Cycle (Early Write)



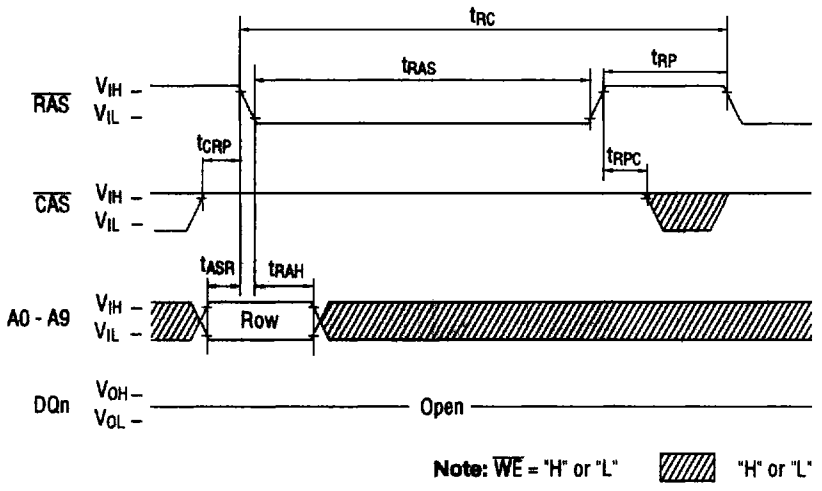
Fast Page Mode Read Cycle



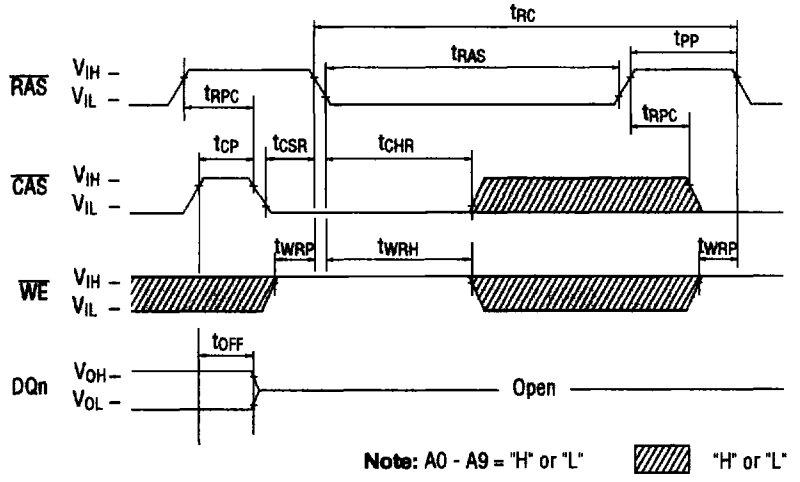
Fast Page Mode Write Cycle



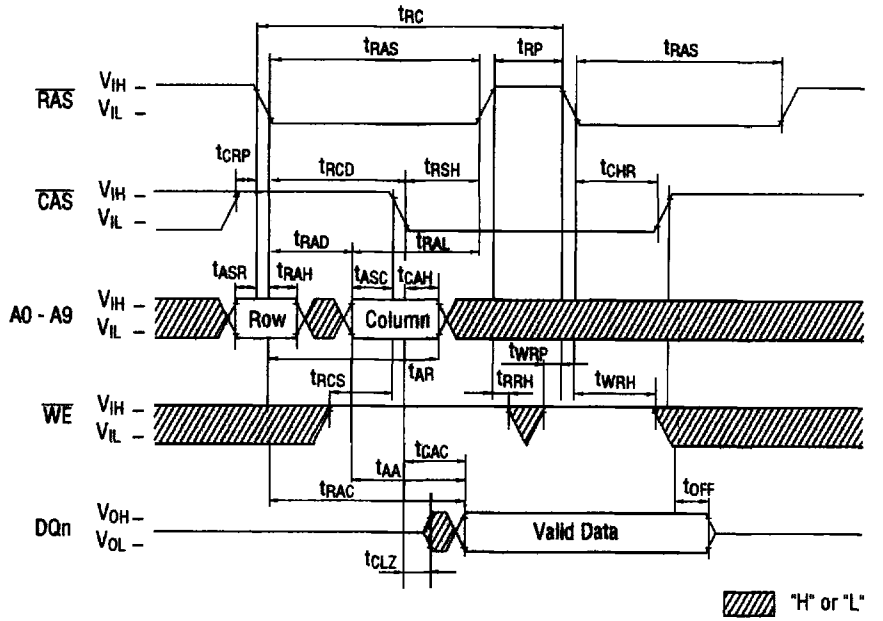
$\overline{RAS}$ Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Hidden Refresh Read Cycle



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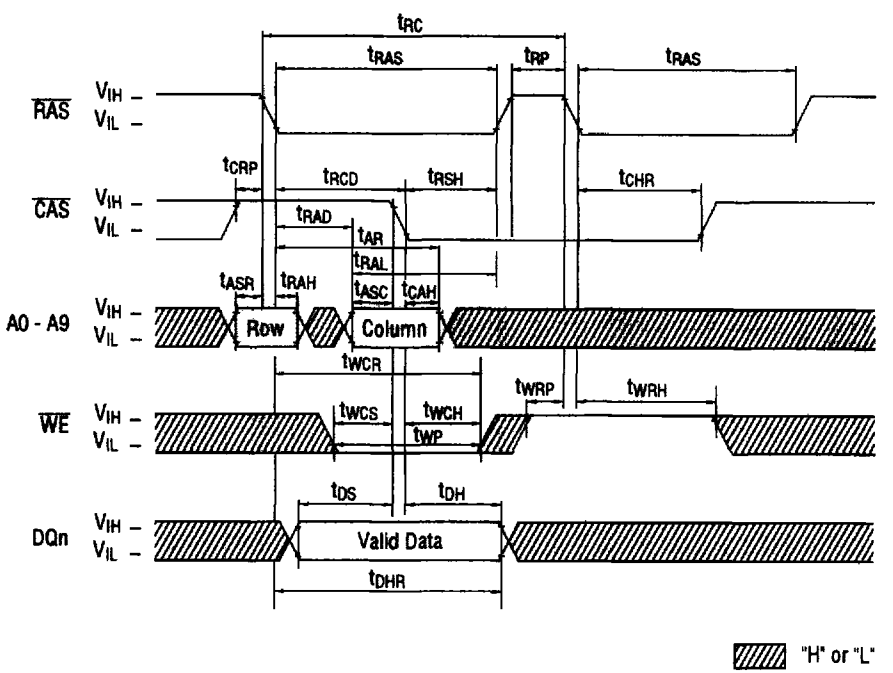
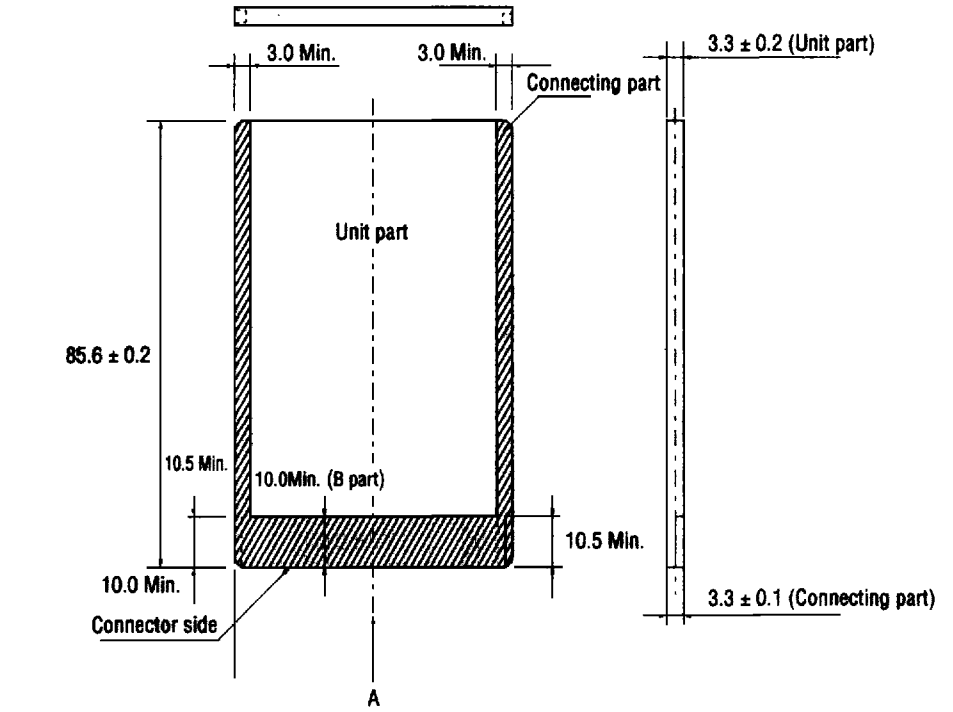


PACKAGE DIMENSIONS



Bottom View from A Arrow Side [Unit: mm]