

## Features

- Compatible with Atmel Two-wire Interface Serial Memory and I<sup>2</sup>C Compatible Devices<sup>(Note:)</sup>
- One, Two or Three Bytes for Slave Address
- Sequential Read/Write Operations
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode

Note: See [Table 1-1](#) below for details on compatibility with I<sup>2</sup>C Standard.

## 1. Description

The Atmel Two-wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format. It can be used with any Atmel Two-wire Interface bus Serial EEPROM and I<sup>2</sup>C compatible device such as Real Time Clock (RTC), Dot Matrix/Graphic LCD Controllers and Temperature Sensor, to name but a few. The TWI is programmable as a master or a slave with sequential or single-byte access. Multiple master capability is supported. Arbitration of the bus is performed internally and puts the TWI in slave mode automatically if the bus arbitration is lost.

A configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies.

Below, [Table 1-1](#) lists the compatibility level of the Atmel Two-wire Interface in Master Mode and a full I<sup>2</sup>C compatible device.

**Table 1-1.** Atmel TWI compatibility with i2C Standard

I <sup>2</sup> C Standard	Atmel TWI
Standard Mode Speed (100 KHz)	Supported
Fast Mode Speed (400 KHz)	Supported
7 or 10 bits Slave Addressing	Supported
START BYTE <sup>(1)</sup>	Not Supported
Repeated Start (Sr) Condition	Supported
ACK and NACK Management	Supported
Slope control and input filtering (Fast mode)	Not Supported
Clock stretching	Supported

Note: 1. START + b000000001 + Ack + Sr



## 32-bit Embedded ASIC Core Peripheral

## Two-wire Interface (TWI2)

## Summary

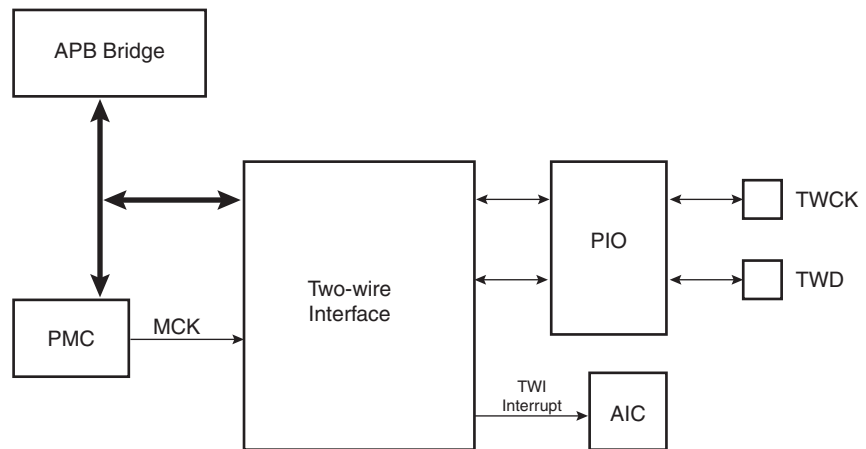
**NOTE:** This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

6212BS-ATARM-21-May-07



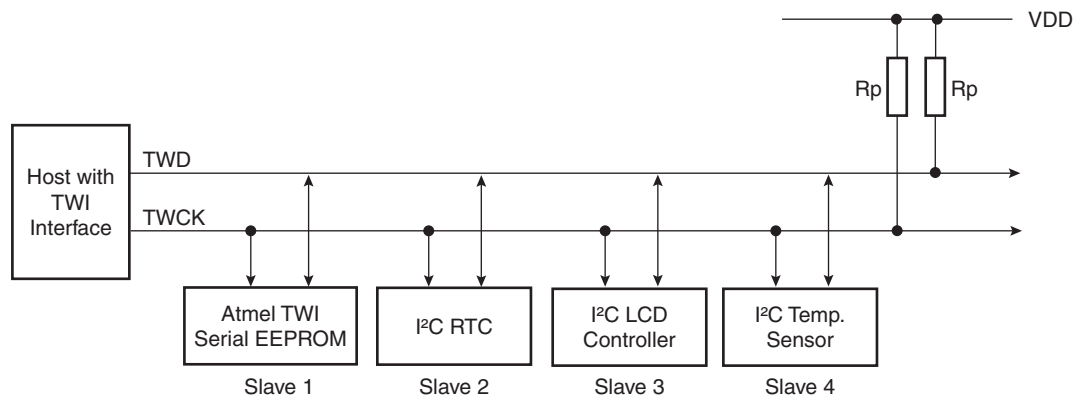
## 2. Block Diagram

Figure 2-1. TWI Block Diagram



## 3. Application Block Diagram

Figure 3-1. TWI Application Block Diagram



R<sub>p</sub>: Pull up value as given by the I<sup>2</sup>C Standard

## Revision History

**Table 3-1.** Revision History

Doc. Rev	Comments	Change Request Ref.
6212AS	First issue	
6212BS	"Features" on page 1, and Description updated with details on Atmel TWI compatibility with I2C standard. Figure 2-1 Block Diagram updated. Table 1-1 and Figure 3-1 Application Block added	4373



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## Literature Requests

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