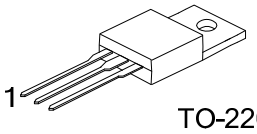
200 A, 20 V N-CHANNEL POWER MOSFET



TO-220

■ DESCRIPTION

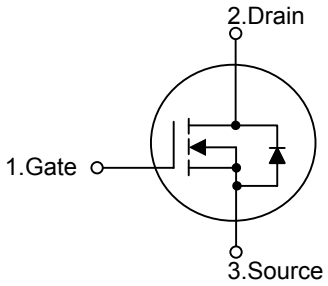
The UTC **UTT200N02** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

The UTC **UTT200N02** is generally applied in synchronous Rectification or DC to DC convertor.

■ FEATURES

* V_{DS} = 20V
* I_D= 200A
* $R_{DS(ON)}$=2.0mΩ(Typ.) @ V_{GS}=10V
* Low Gate Charge (Typical 84nC)
* High Switching Speed
* High Power and Current Handling Capability
* RoHS Compliant

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT200N02L-TA3-T	UTT200N02G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT200N02L-TA3-T

(1)Packing Type	(1) T: Tube
(2)Package Type	(2) TA3: TO-220
(3)Lead Free	(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous (Silicon Limited)	I_D	200 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	800	A
Single Pulsed Avalanche Energy (Note 4)		E_{AS}	864	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	6.0	V/ns
Power Dissipation		P_D	214	W
Derate above 25°C			1.43	W/°C
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{STG}	-55~+175	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 100A.
3. Repetitive Rating: Pulse width limited by maximum junction temperature
4. L = 3mH, I_{AS} =24A, V_{DD} = 20V, R_G = 25Ω, Starting T_J = 25°C
5. I_{SD} ≤ 200A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	°C/W
Junction to Case	θ_{JC}	0.7	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	20			V
Breakdown Voltage Temperature Coefficient		$\triangle BV_{DSS}/\triangle T_J$	Reference to 25°C, I_D=250μA		30		mV/°C
Drain-Source Leakage Current		I_{DSS}	V_{DS}=20V, V_{GS}=0V			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=80A		2.0	2.4	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		5490	7300	pF
Output Capacitance		C_{OSS}			1220	1620	pF
Reverse Transfer Capacitance		C_{RSS}			155	233	pF
SWITCHING PARAMETERS							
Total Gate Charge at 10V		$Q_{G(tot)}$	V_{GS}=10V, V_{DS}=16V, I_D=80A (Note 1, 2)		84	109	nC
Gate to Source Charge		Q_{GS}			19		nC
Gate Charge Threshold to Plateau		Q_{GS2}			9.5		nC
Gate to Drain Charge		Q_{GD}			12		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=10V, I_D=80A, R_{GEN}=4.7Ω, V_{GS}=10V (Note 1, 2)		17	44	ns
Rise Time		t_R			8	26	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			71	152	ns
Fall-Time		t_F			17	44	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				200	A
Maximum Body-Diode Pulsed Current		I_{SM}				800	A
Drain-Source Diode Forward Voltage		V_{SD}	I_{SD}=200A, V_{GS}=0V			1.3	V

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature Typical Characteristics

■ TEST CIRCUITS AND WAVEFORMS

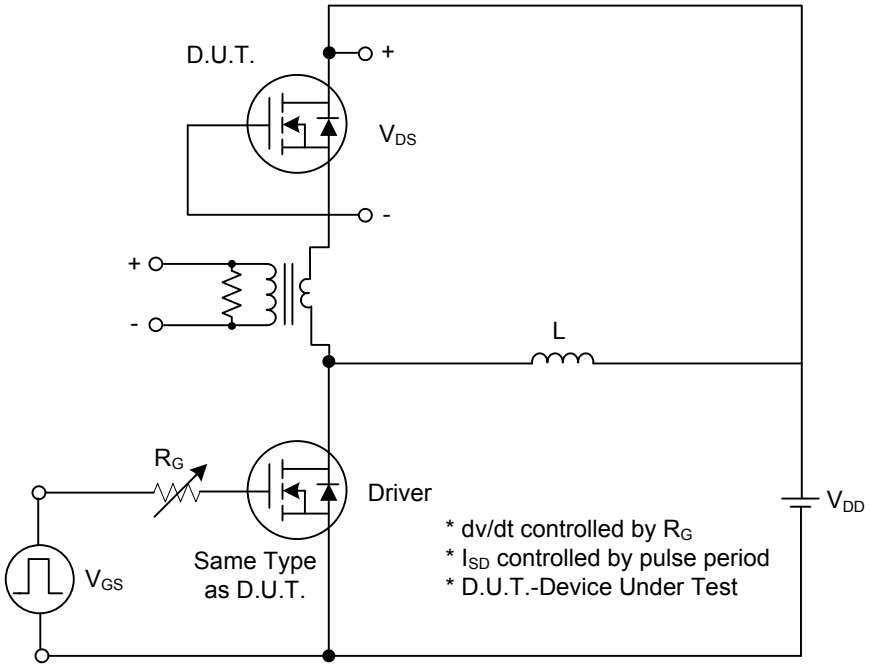


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

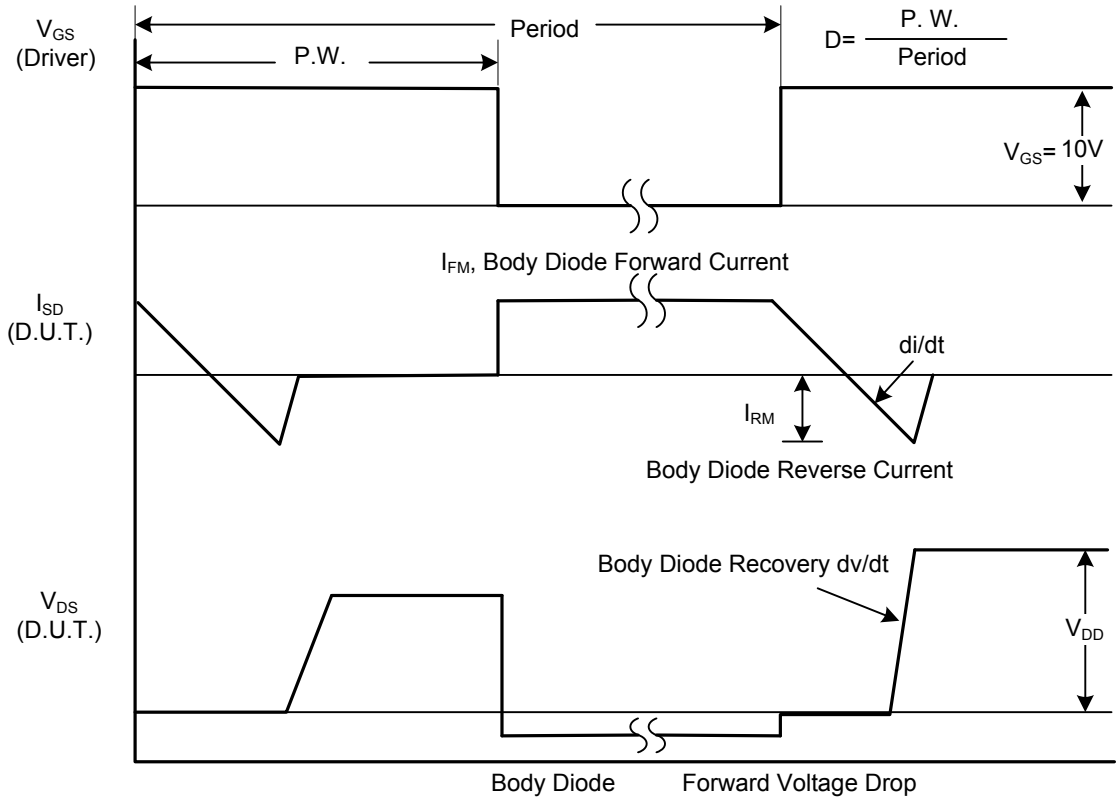


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

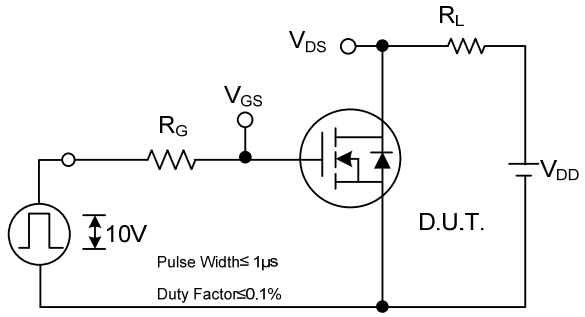


Fig. 2A Switching Test Circuit

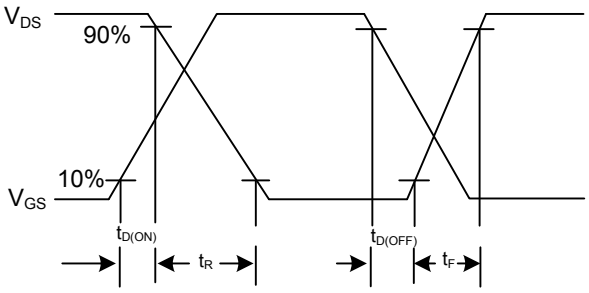


Fig. 2B Switching Waveforms

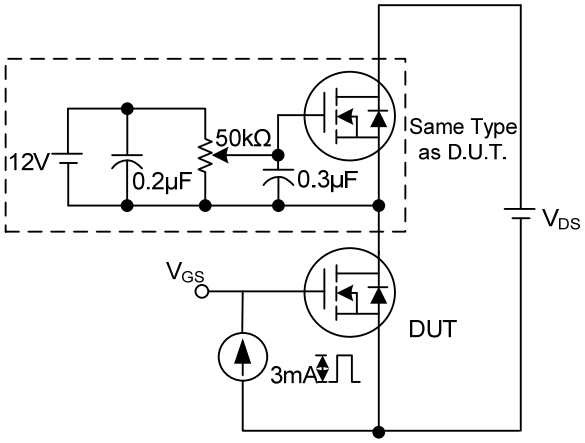


Fig. 3A Gate Charge Test Circuit

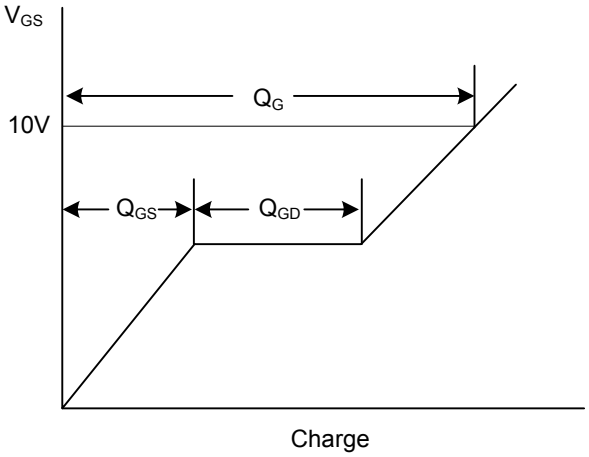


Fig. 3B Gate Charge Waveform

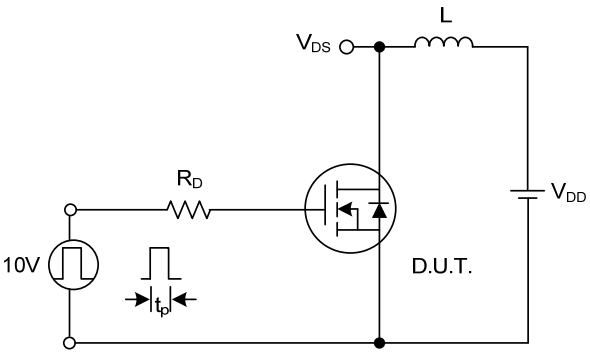


Fig. 4A Unclamped Inductive Switching Test Circuit

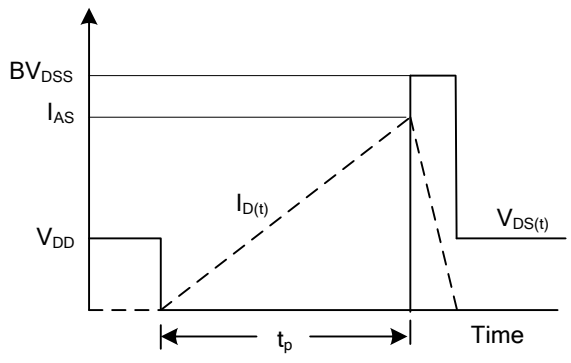


Fig. 4B Unclamped Inductive Switching Waveforms