Am25LS2548

Chip Select Address Decoder with Acknowledge

DISTINCTIVE CHARACTERISTICS

- One-of-Eight Decoder provides eight chip select outputs
- Acknowledge output responds to enables and read or write command
- Open-collector Acknowledge output for wired-OR application
- Inverting and non-inverting enable inputs for upper address decoding

GENERAL DESCRIPTION

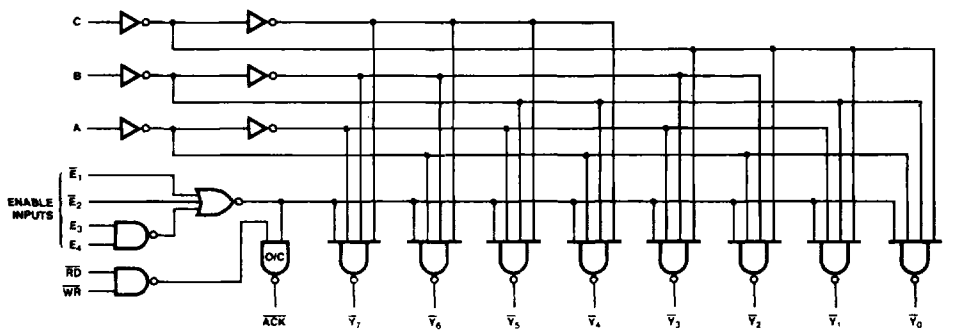
The Am25LS2548 Address Decoder combines a three-line to eight-line decoder with four qualifying enable inputs (two active HIGH and two active LOW) and the acknowledge output required for "ready" or "wait state" control of all popular MOS microprocessors.

The acknowledge output, $\overline{ACK}$, is active LOW and responds to the combination of all enables active and a read ($\overline{RD}$) or write ($\overline{WR}$) input command.

The eight chip select outputs are individually active LOW in response to the combination of all enables active and the corresponding 3-bit input code at inputs A, B, and C.

The Am25LS2548 is intended for chip select decoding in small, medium or large systems where multiple chip selects *must be generated and address space must be allocated* conservatively.

BLOCK DIAGRAM



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RELATED PRODUCTS

Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1-of-10 Decoder
Am25LS2538	1-of-8 Decoder
Am25LS2539	Dual 1-of-4 Decoder
Am2921	1-of-8 Decoder
Am2924	3-to-8 Line Decoder/Demultiplexer

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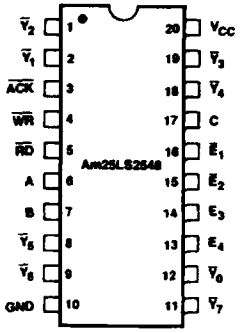
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-20-1



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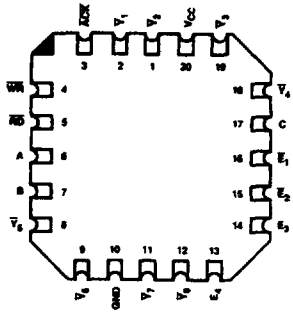

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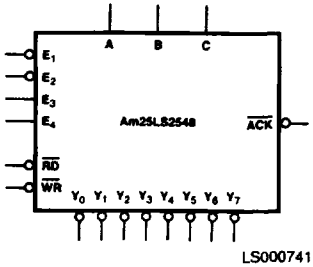
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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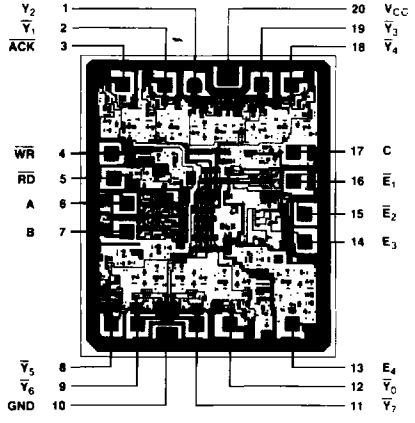
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.081" x 0.096"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2548 **D** **C** **B**

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D– 20-pin CERDIP; F – 20-pin flatpak; L – 20-pin leadless chip carrier; P – 20-pin plastic DIP; X – Dice
- Am25LS2548 — Device type: Address Decoder

Valid Combinations	
Am25LS2548	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
6, 7, 17	A, B, C	I	Three-line to eight-line chip select decoder inputs.
16, 15	$\overline{E}_1$, $\overline{E}_2$	I	The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled, and forces $\overline{ACK}$ HIGH.
14, 13	E_3, E_4	I	The active HIGH enable inputs. A LOW on either the E_3 or E_4 input forces all the decoded functions to be inhibited, and forces $\overline{ACK}$ HIGH.
4, 5	$\overline{WR}$, $\overline{RD}$	I	The write input, $\overline{WR}$, and read input, $\overline{RD}$, are active LOW inputs used as conditions for an active LOW output at the acknowledge, $\overline{ACK}$, output.
3	$\overline{ACK}$	O	The acknowledge output, $\overline{ACK}$, is an active LOW output used to signal the microprocessor that specific devices have been selected. $\overline{ACK}$ goes LOW only when $\overline{E}_1$ and $\overline{E}_2$ are LOW, E_3 and E_4 are HIGH and $\overline{WR}$ or $\overline{RD}$ is LOW.
	$\overline{Y}_i$	O	The eight active LOW chip select outputs.

FUNCTION TABLES

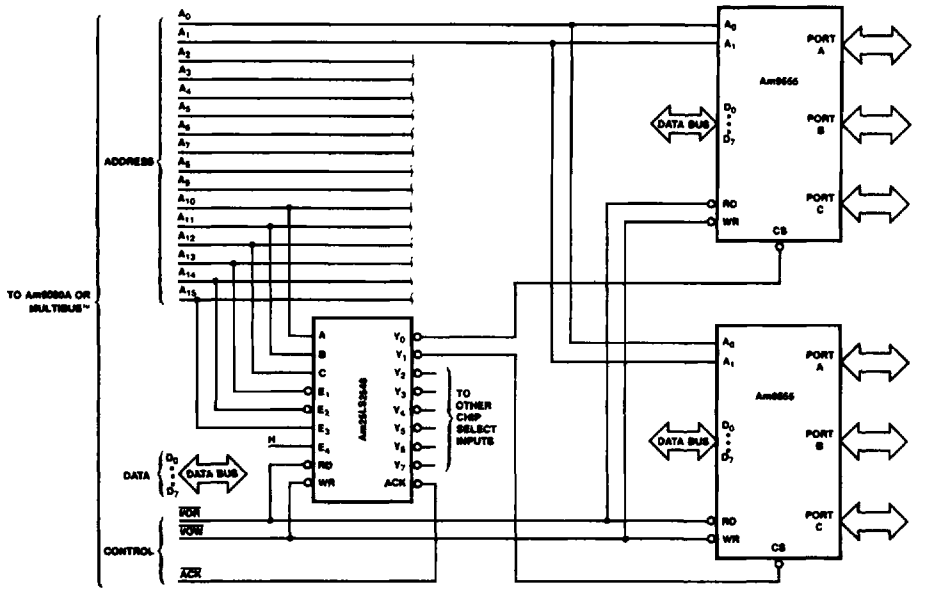
CHIP SELECT OUTPUTS Y_i

C	B	A	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	L	H	H
H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	H	L
X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	X	H	H	H	H	H	H	H	H
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H

ACKNOWLEDGE OUTPUT $\overline{ACK}$

$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

APPLICATIONS



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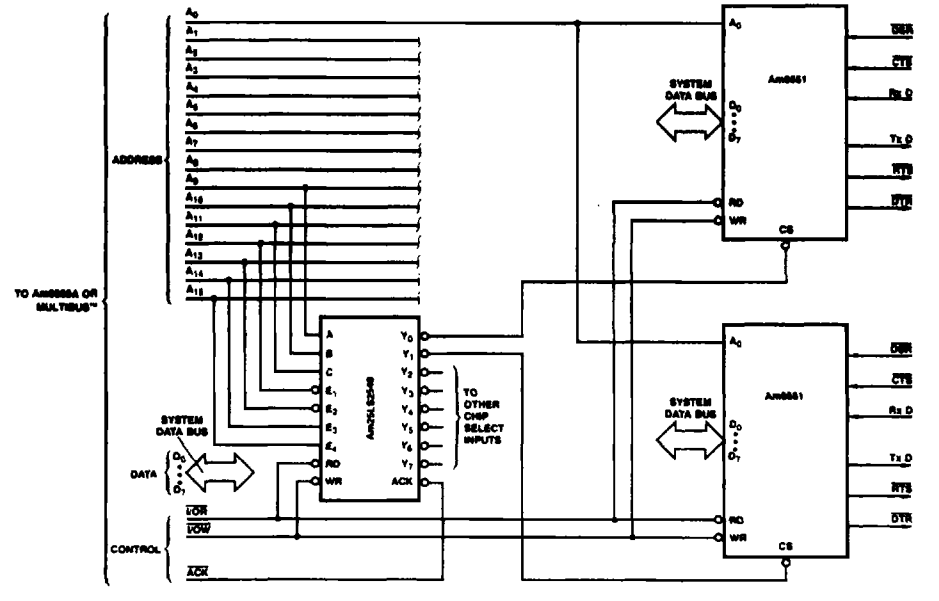

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			15	20	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1$ = $\overline{E}_2$ = GND: RD = WR = E_3 = E_4 = 4.5V.

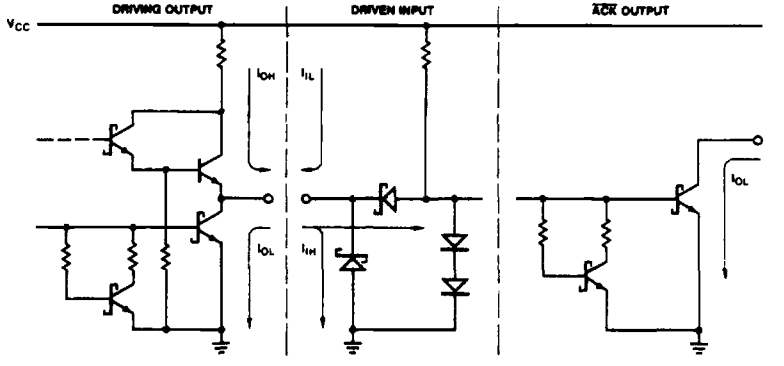
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B or C to $\overline{Y}_i$ (Three Level Delay)	C_L = 15pF, R_L = 2.0kΩ		14	20	ns
t_{PHL}				19	27	ns
t_{PLH}	A, B, or C to $\overline{Y}_i$ (Two Level Delay)			13	18	ns
t_{PHL}				15	21	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$			13	18	ns
t_{PHL}				16	23	ns
t_{PLH}	E_3, E_4 to $\overline{Y}_i$			15	21	ns
t_{PHL}				19	27	ns
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$			25	35	ns
t_{PHL}				16	22	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$			29	40	ns
t_{PHL}				25	35	ns
t_{PLH}	E_3, E_4 to $\overline{ACK}$			29	40	ns
t_{PHL}				25	35	ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am25LS2548 Min	COMMERCIAL Am25LS2548 Max	MILITARY Am25LS2548 Min	MILITARY Am25LS2548 Max	Units
t_{PLH}	A, B or C to Y_i (Three Level Delay)	C_L = 50pF, R_L = 2.0kΩ		27		30	ns
t_{PHL}				34		36	ns
t_{PLH}	A, B or C to Y_i (Two Level Delay)			23		25	ns
t_{PHL}				28		31	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$			23		25	ns
t_{PHL}				29		31	ns
t_{PLH}	E_3, E_4 to $\overline{Y}_i$			27		28	ns
t_{PHL}				34		36	ns
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$			45		45	ns
t_{PHL}				31		35	ns
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$			45		45	ns
t_{PHL}				39		40	ns
t_{PLH}	E_3, E_4 to $\overline{ACK}$			45		45	ns
t_{PHL}				39		40	ns

Am25LS2548
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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