PROCESS CP704V

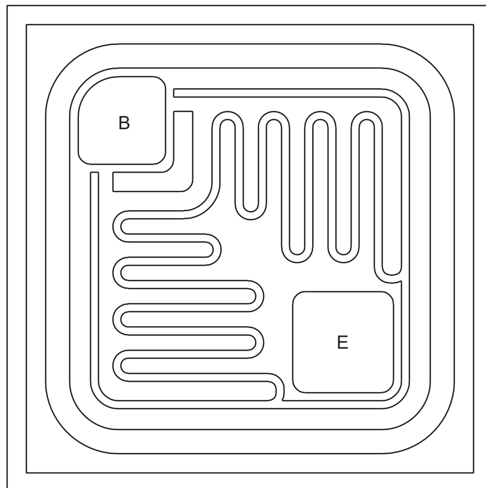
Small Signal Transistors

PNP - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	22 x 22 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	3.7 x 3.7 MILS
Emitter Bonding Pad Area	4.2 x 4.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 5 INCH WAFER

35,100

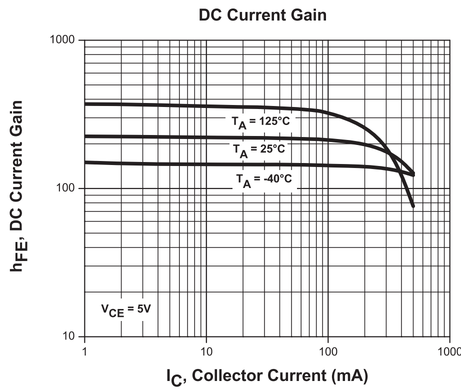
PRINCIPAL DEVICE TYPES

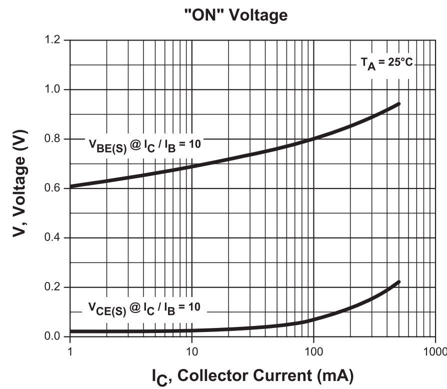
MPSA55
MPSA56

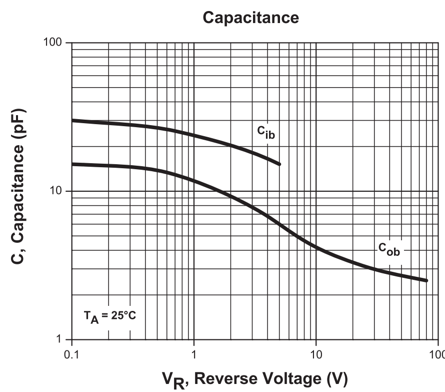
R1 (22-March 2010)

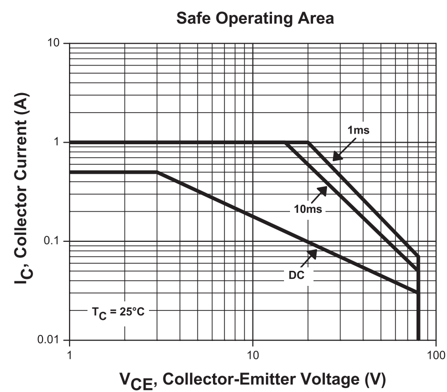
PROCESS CP704V

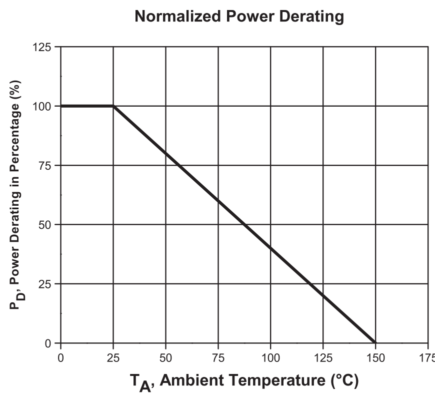
Typical Electrical Characteristics

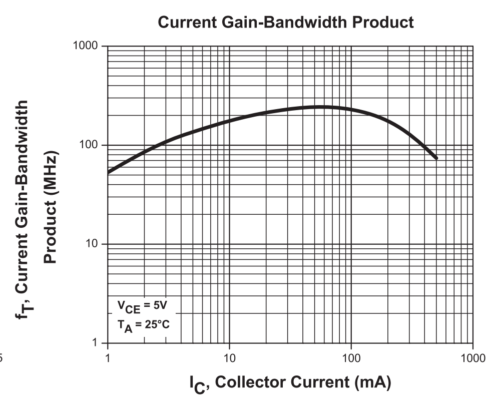












R1 (22-March 2010)