Integrated Device Technology, Inc.

128KB/256KB SECONDARY CACHE MODULES FOR THE INTEL® i486™ PROCESSOR

IDT7MP6121
IDT7MP6122

FEATURES

- 128KB/256KB secondary cache module family
- Ideal for use with many Intel i486 CPU-based systems that use the industry standard chipsets
- Operates with external i486 processor speeds of 50MHz
- 64 position dual read-out SIMM (Single In-line Memory Module) with 128 leads
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity

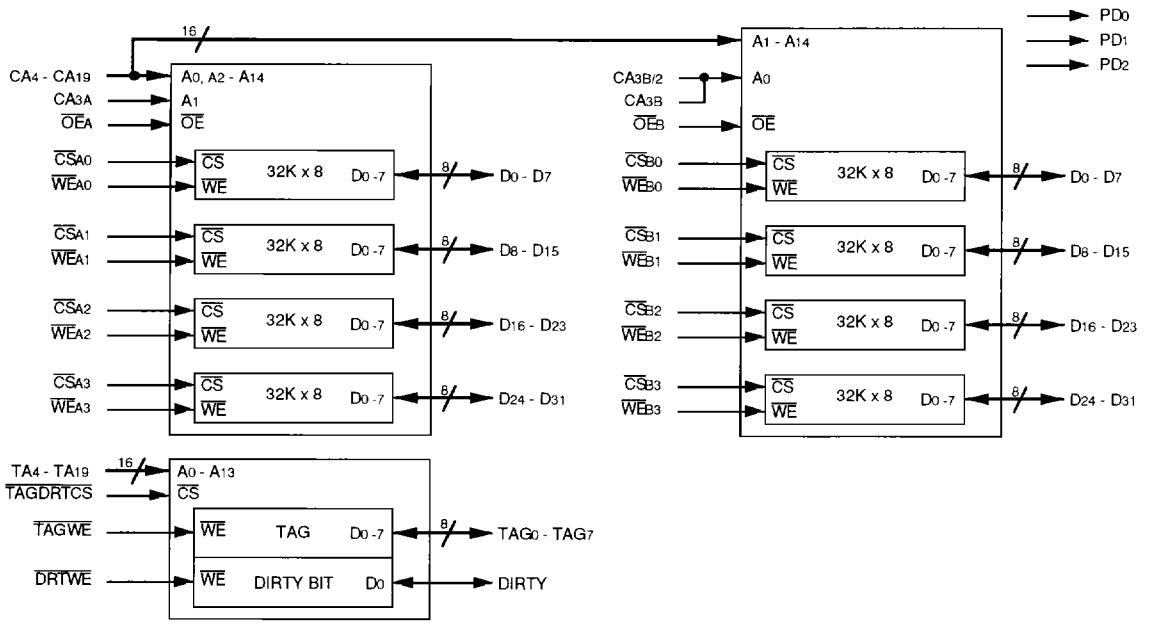
DESCRIPTION

The IDT7MP6121/22 are members of a family of secondary caches that are ideal for use with many Intel i486 CPU-based systems. The IDT7MP6121/22 use IDT's asynchronous SRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. High speeds at optimum costs are achieved using IDT's high-performance, high-reliability CMOS technology.

The dual read-out SIMM package configuration allows 128 signal leads to be placed on a package 3.85" long. Depending on which cache configuration is used, the module is a maximum of 0.35" thick and a maximum of 1.05" tall.

The IDT7MP6121/22 operate from single 5V power supply. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

FUNCTIONAL BLOCK DIAGRAM
IDT7MP6122 – 256KB VERSION



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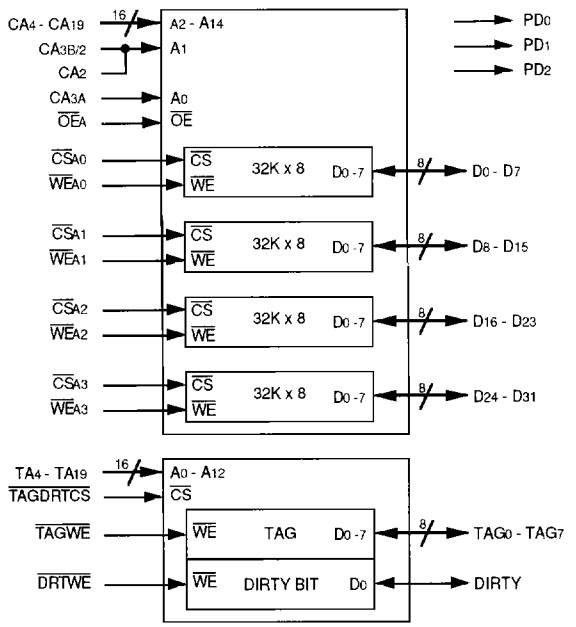
FUNCTIONAL BLOCK DIAGRAM
IDT7MP6121 – 128KB VERSION



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PIN NAMES

$CA_4 - CA_{19}$	Cache Address Inputs
CA_2, $CA_{3B/2}$, CA_{3A}, CA_{3B}	Bank Cache Address Inputs
$D_0 - D_{31}$	Cache Data Inputs/Outputs
$\overline{CS}_{A0} - \overline{CS}_{A3}$	Bank A Byte Chip Select Inputs
$\overline{CS}_{B0} - \overline{CS}_{B3}$	Bank B Byte Chip Select Inputs
$\overline{WE}_{A0} - \overline{WE}_{A3}$	Bank A Byte Write Enable Inputs
$\overline{WE}_{B0} - \overline{WE}_{B3}$	Bank B Byte Write Enable Inputs
$\overline{OE}_A$	Bank A Output Enable Input
$\overline{OE}_B$	Bank B Output Enable Input
$TA_4 - TA_{19}$	Tag, Dirty Bit Address Inputs
$TAG_0 - TAG_7$	Tag Data Inputs/Outputs
DIRTY	Dirty Bit Input/Output
$\overline{TAGDRTCS}$	Tag/Dirty Chip Select Input
$\overline{TAGWE}$	Tag Write Enable Input
$\overline{DRTWE}$	Dirty Bit Write Enable Input
$PD_0 - PD_2$	Presence Detect Pins
N.C.	No Connect
GND	Ground
V_{CC}	Power Supply

2927 tbl 01

PIN CONFIGURATION[3]

PD0	1	65	PD1
PD2	2	66	GND
D0	3	67	D1
D2	4	68	D3
D4	5	69	VCC
D6	6	70	D5
D8	7	71	D7
GND	8	72	D9
D10	9	73	D11
D12	10	74	D13
D14	11	75	D15
D16	12	76	D17
D18	13	77	D19
D20	14	78	D21
GND	15	79	GND
D22	16	80	D23
D24	17	81	D25
VCC	18	82	VCC
D26	19	83	D27
D28	20	84	D29
D30	21	85	D31
(1) N.C.	22	86	N.C.(1)
(1) N.C.	23	87	N.C.(1)
GND	24	88	GND
$\overline{CS}_{A0}$	25	89	$\overline{CS}_{B0}$(2)
$\overline{CS}_{A1}$	26	90	$\overline{CS}_{B1}$(2)
$\overline{CS}_{A2}$	27	91	VCC
$\overline{CS}_{A3}$	28	92	$\overline{CS}_{B2}$(2)
GND	29	93	$\overline{CS}_{B3}$(2)
$\overline{OE}_A$	30	94	$\overline{OE}_B$ (2)
$\overline{WE}_{A0}$	31	95	$\overline{WE}_{B0}$(2)
$\overline{WE}_{A1}$	32	96	$\overline{WE}_{B1}$(2)
$\overline{WE}_{A2}$	33	97	$\overline{WE}_{B2}$(2)
$\overline{WE}_{A3}$	34	98	$\overline{WE}_{B3}$(2)
$\overline{TAGWE}$	35	99	$\overline{DRTWE}$
$\overline{TAGDRTCS}$	36	100	VCC
(1) N.C.	37	101	N.C.(1)
(1) N.C.	38	102	N.C.(1)
CA3A	39	103	CA3B/2
CA2	40	104	CA3B
GND	41	105	GND
CA4	42	106	CA5
CA6	43	107	CA7
CA8	44	108	CA9
CA10	45	109	CA11
CA12	46	110	CA13
CA14	47	111	CA15
CA16	48	112	CA17
CA18	49	113	CA19
GND	50	114	GND
TA4	51	115	TA5
TA6	52	116	TA7
TA8	53	117	TA9
TA10	54	118	TA11
TA12	55	119	TA13
TA14	56	120	TA15
TA16	57	121	TA17
TA18	58	122	TA19
GND	59	123	GND
TAG0	60	124	TAG1
TAG2	61	125	TAG3
TAG4	62	126	TAG5
TAG6	63	127	TAG7
DIRTY	64	128	VCC

DUAL READ-OUT SIMM
TOP VIEW

2927 drw 03

NOTES:
1. These pins are reserved for future use. Please consult the factory for details.
2. These pins are N.C. (no connect) on the IDT7MP6121 module.
3. The module pinout supports cache sizes up to 1MB.

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PRESENCE DETECT TABLE

PD2	PD1	PD0	Size	Module
N.C	N.C.	N.C.	—	no cache present
N.C.	N.C.	GND	—	reserved
N.C.	GND	N.C.	—	reserved
N.C.	GND	GND	128KB	IDT7MP6121
GND	N.C.	N.C.	256KB	IDT7MP6122
GND	N.C.	GND	—	reserved
GND	GND	N.C.	—	reserved
GND	GND	GND	—	reserved

2927 tbl 02

CAPACITANCE[1, 2]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	7MP6121/22	Unit
C_{IN1}	Input Capacitance (Data Address)	V_{IN} = 0V	50/95	pF
C_{IN2}	Input Capacitance (Tag Address, $\overline{TAGDRTCS}$)	V_{IN} = 0V	20	pF
C_{IN3}	Input Capacitance ($\overline{OE_A}$, $\overline{OE_B}$)	V_{IN} = 0V	50	pF
C_{IN4}	Input Capacitance (All other controls)	V_{IN} = 0V	14	pF
$C_{I/O1}$	Data I/O Capacitance	V_{OUT} = 0V	14/25	pF
$C_{I/O2}$	Tag I/O Capacitance	V_{OUT} = 0V	12	pF

NOTES:
2927 tbl 03
1. These parameters are guaranteed by design but not tested.
2. These parameters are maximum values.

RECOMMENDED DC OPERATING CONDITIONS[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
2927 tbl 04
1. V_{IL} = –3.0V for pulse width less than 5ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V

2927 tbl 05

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
2927 tbl 06
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	7MP6121/22 Min.	7MP6121/22 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Data)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10/20	µA
$\|I_{LI}\|$	Input Leakage Current (Data Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	40/80	µA
$\|I_{LI}\|$	Input Leakage Current (Tag Address, $\overline{TAGDRTCS}$)	V_{CC} = Max, V_{IN} = GND to V_{CC}		20	µA
$\|I_{LI}\|$	Input Leakage Current ($\overline{OE_A}$, $\overline{OE_B}$)	V_{CC} = Max, V_{IN} = GND to V_{CC}		40	µA
$\|I_{LI}\|$	Input Leakage Current (Control)	V_{CC} = Max, V_{IN} = GND to V_{CC}		10	µA
$\|I_{LO}\|$	Output Leakage Current (Data)	V_{OUT} = 0V to V_{CC}, V_{CC} = Max., $\overline{CS} \geq V_{IH}$	—	10/20	µA
$\|I_{LO}\|$	Output Leakage Current (Tag)	V_{OUT} = 0V to V_{CC}, V_{CC} = Max., $\overline{CS} \geq V_{IH}$	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, f = f_{MAX}, Outputs Open	—	935/1525	mA
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, f = f_{MAX}, Outputs Open	—	300/510	mA
I_{SB1}	Full Standby Supply Current	V_{CC} = Max., $\overline{CS} \geq V_{CC}$ – 0.2V, f =0, $V_{IN} > V_{CC}$ – 0.2V or < 0.2V	—	115/200	mA

2927 tbl 07

SRAM CYCLE TIMES[1, 2]

Module Speed	Size	Data	Tag	Dirty
33MHz	128KB	20ns	15ns	15ns
33MHz	256KB	20ns	15ns	15ns

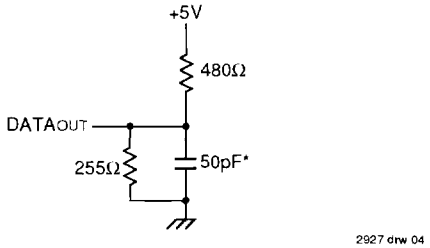
2927 tbl 08

NOTES:
1. Cycle times are for the SRAMs themselves used on the module. Modules are tested for function only.
2. Please consult the factory regarding other speeds.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2927 tbl 09



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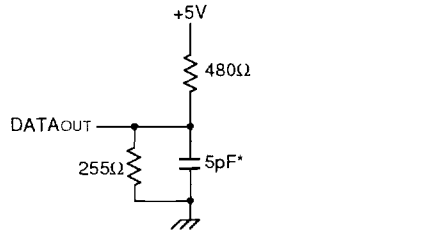
*including scope and jig capacitances

Figure 1. Output Load



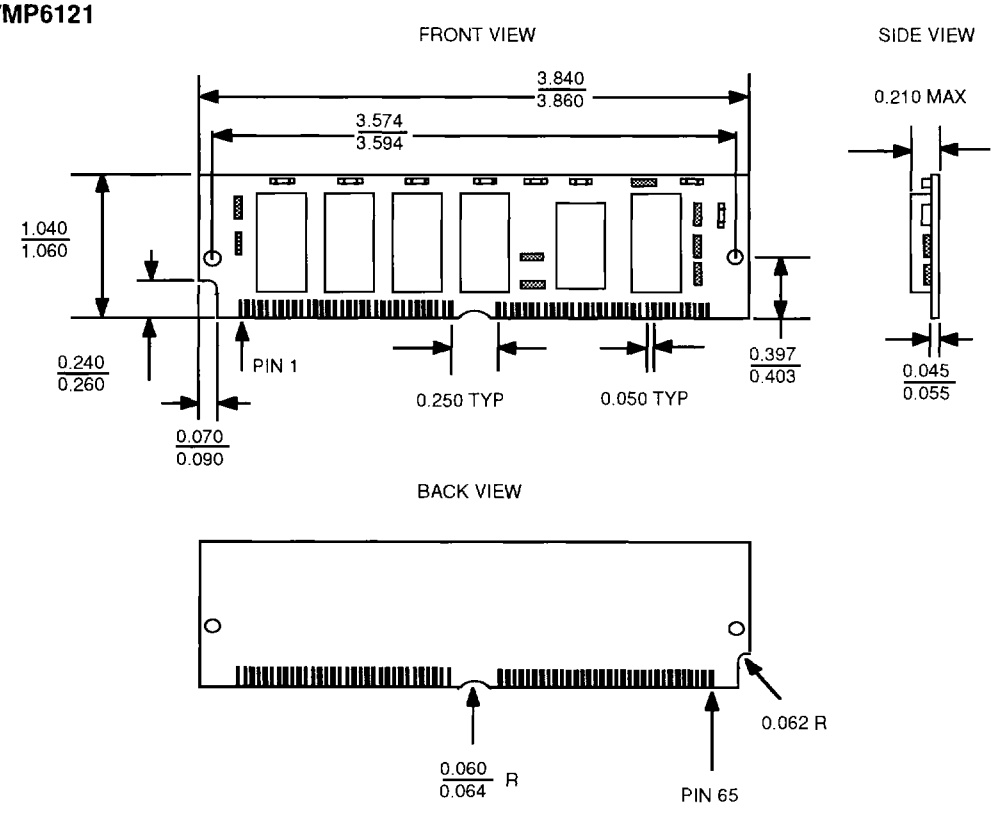
2927 drw 05

*including scope and jig capacitances

Figure 2. Output Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

PACKAGE DIMENSIONS

7MP6121



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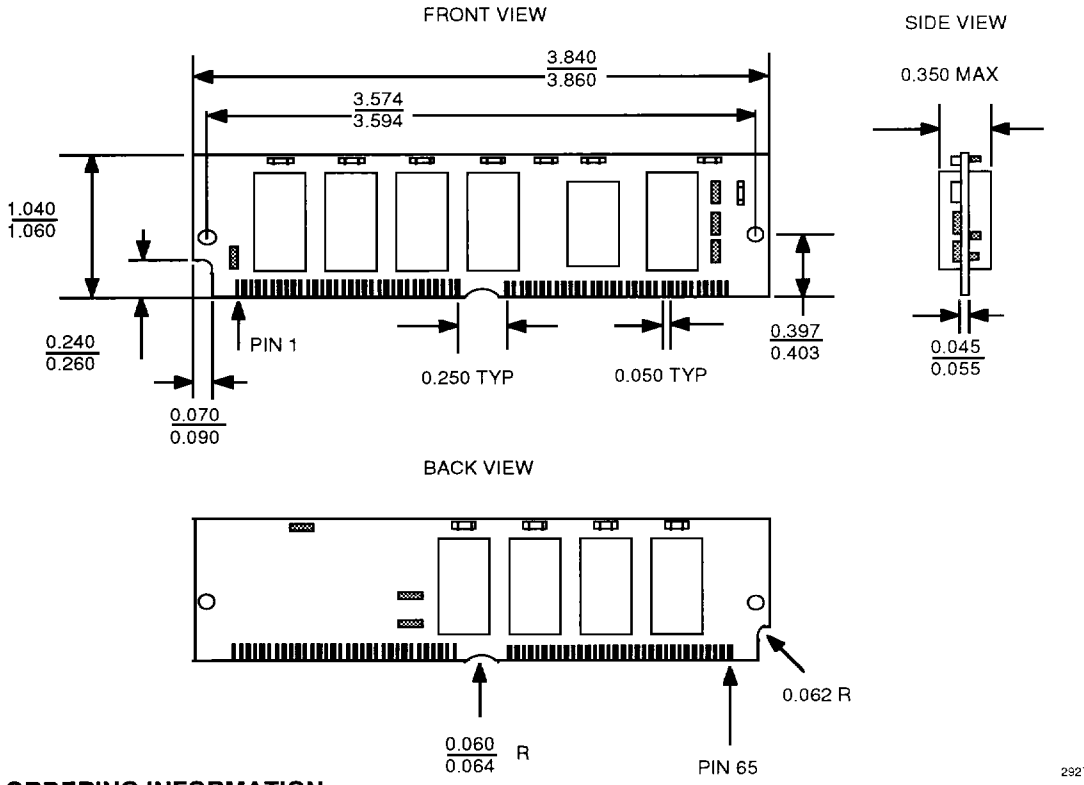
7MP6122



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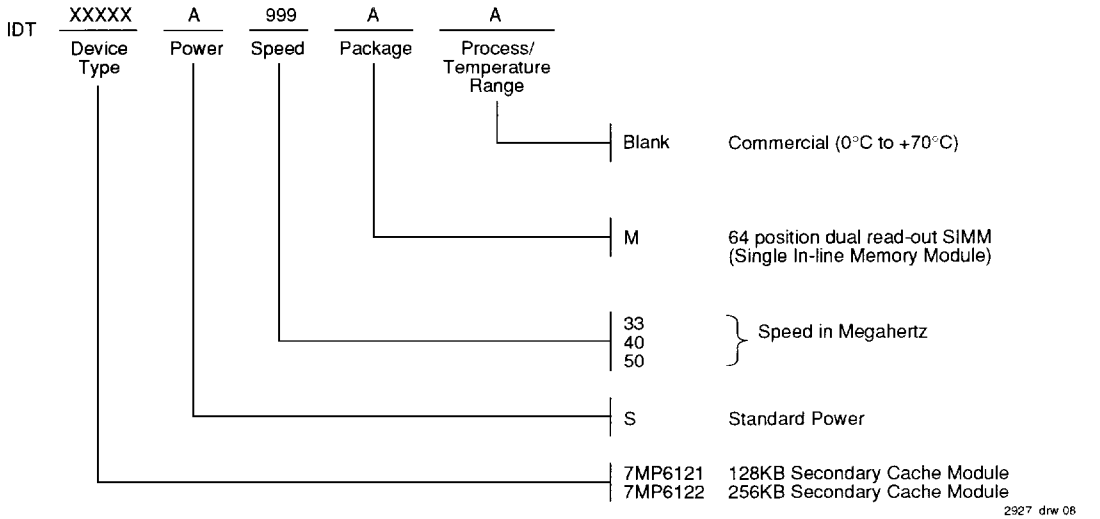
ORDERING INFORMATION



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