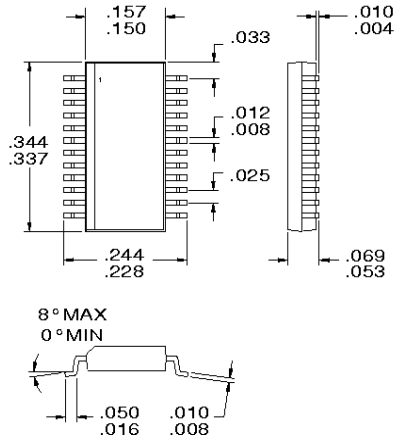
CDMA/FM LOW NOISE AMPLIFIER/MIXER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Down Converter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

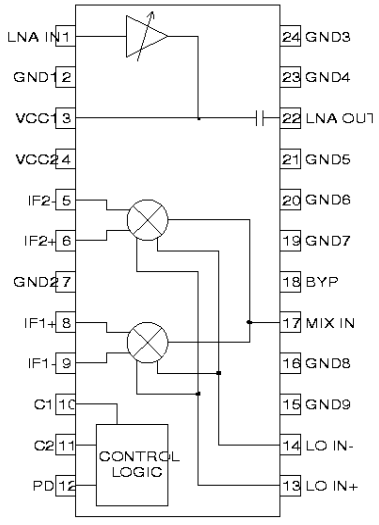
The RF2404 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and down-convert RF signals while providing 20dB of stepped gain control range and features digital control of LNA gain and IF selection. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Receive LNA/Mixer, a Receive IF AGC Amp, a Transmit IF AGC Amp, and a Transmit Upconverter. The IC is manufactured on an advanced Silicon Bipolar process, and is packaged in a standard miniature 24-lead plastic SSOP package.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Stepped LNA Gain Control
- Single 2.7 to 4.0V Power Supply
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation

Ordering Information

RF2404	CDMA/FM Low Noise Amplifier/Mixer
RF2404 PCBA	Fully Assembled Evaluation Board

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Greensboro, NC 27409, USA

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http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +4.5	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

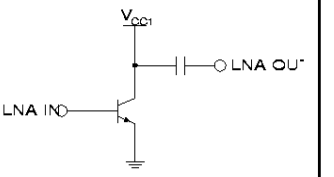
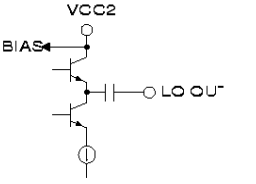
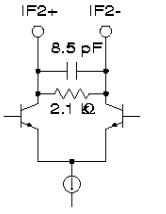
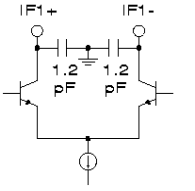
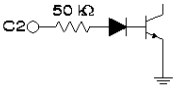
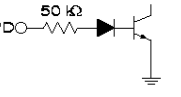
Caution! ESD sensitive device.

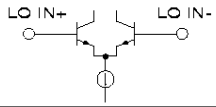
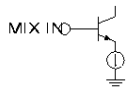
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T = 25 ° C, V_{CC}=3.0V, RF=881MHz, LO=966MHz @ 0dBm See Mode Control Logic Table
RF Frequency Range		500 to 1100		MHz	
LO Frequency Range		500 to 1100		MHz	
IF Frequency Range		0.1 to 250		MHz	
Cascaded Perform. to IF1					1kΩ balanced load, 3.0dB Image Filter Loss; CDMA Max. Gain
Cascade Conversion Gain	23.5	24.5		dB	
Cascade Input IP3 to IF1	-7	-5		dBm	
Cascade Noise Figure		4.5		dB	
Cascaded Perform. to IF2					870Ω load, 3.0dB Image Filter Loss FM
Cascade Conversion Gain	16	18		dB	
Cascade Input IP3	-10	-5		dBm	
Cascade Noise Figure		4.5		dB	
First Section (LNA)					
Gain		14.5		dB	FM and CDMA Max. Gain
		7.5		dB	CDMA Nom. Gain
		-5		dB	CDMA Min. Gain
Noise Figure		2.5		dB	FM and CDMA Max. Gain
		4.6		dB	CDMA Nom. Gain
		9.1			CDMA Min. Gain
Input IP3		+5		dBm	FM and CDMA Max. Gain
		+14		dBm	CDMA Nom. Gain
		+20		dBm	CDMA Min. Gain
Input P1dB		-12		dBm	FM and CDMA Max. Gain
Reverse Isolation		23		dB	FM and CDMA Max. Gain
Input VSWR		4:1			Internally matched for optimum noise figure from a 50Ω source.
Output VSWR		<1.5:1			With partial external matching network.
Second Section (Mixer, IF1 or IF2 Output)					
Conversion Gain		15		dB	IF 1, 1kΩ balanced load.
		6.5		dB	IF 2, 870Ω load.
Noise Figure		11.5		dB	Single sideband.
Input VSWR		<1.5:1			With external matching network.
Input IP3 to IF1		+7		dBm	
Input IP3 to IF2		+7		dBm	
Input P1dB, IF1		-8		dBm	
Input P1dB, IF2		-4		dBm	
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.

LO Input					
LO Input Range		-6 to 0		dBm	
LO IN to LNA Input Rejection		37		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			With external matching network.
Power Supply					
Voltage		2.7 to 4.0		V	
Current Consumption		19		mA	FM
		24		mA	CDMA Max. Gain
		21		mA	CDMA Min. Gain
		< 20		µA	Power Down

Mode Control Logic

MODE	C1	C2	PD
FM (IF2)	L	H	H
CDMA Max Gain (IF1)	H	H	H
CDMA Nom. Gain (IF1)	H	L	H
CDMA Min. Gain (IF1)	L	L	H
Power Down	X	X	L

Pin	Function	Description	Interface Schematic
1	LNA IN	RF Input pin. This pin is internally matched for optimum noise fgure from a 50Ω source. This pin is internally DC biased and, if connected to a device with DC present, should be DC blocked with a capacitor suitable for the frequency of operation.	
2	GND1	Ground connection for the LNA circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VCC1	Supply Voltage for the LNA. External inductance, ~12nH, is required in addition to internal inductance to achieve optimum LNA performance. This extra inductance can be easily achieved with a thin microstrip line. The value of this inductance will change with the frequency of operation. RF and IF bypassing is required on the supply side of the inductance. The ground side of the bypass capacitors should connect immediately to ground plane.	See pin 1.
4	VCC2	Supply Voltage for the LO buffer amplifier, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	IF2-	Same as pin 6, except complementary output. For typical single ended operation, this pin is connected directly to V_{CC}.	See pin 6.
6	IF2+	FM IF Output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about 870Ω at 85 MHz. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
7	GND2	Ground connection for the logic and bias circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
8	IF 1+	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85 MHz is higher than 1kΩ, even though the part is designed to drive a 1kΩ load. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
9	IF 1-	Same as pin 8, except complementary output.	See pin 8.
10	C1	Control line for mode/gain select. See specification table for details. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	
11	C2	Control line for mode/gain select. See specification table for details. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	
12	PD	Power down pin. A logic "low" turns the part off. A logic "high" (>1.6V) turns the part on. In addition, pin 10 (C1) should also be taken low during power down.	

13	LO IN+	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 14 is bypassed to ground.	
14	LO IN-	LO bypass.	See pin 13.
15	GND9	Die flag ground. Keep traces physically short and connect immediately to ground plane for best performance.	
16	GND8	Ground connection for the mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
17	MIX IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
18	BYP	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
19	GND7	Same as pin 7.	
20	GND6	Ground connection for the LNA circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
21	GND5	Same as pin 7.	
22	LNA OUT	LNA Output pin. This pin is internally DC blocked and externally matched to 50Ω at pin 3 in order to facilitate an easy interface to a 50Ω Image Filter.	See pin 1.
23	GND4	Same as pin 21.	
24	GND3	Same as pin 21.	