

# □ MN103S73 Series

Type	MN103SF73N	MN103SF73R
Internal ROM type	FLASH	
ROM (byte)	512K	1024K
RAM (byte)	32K	
Package (Lead-free)	QFP100-P-1818B	
Minimum Instruction Execution Time	25 ns (at 2.7 V to 3.6 V, 40 MHz)	

## ■ Interrupts

RESET. IRQ × 8. NMI. Timer × 28. I<sup>2</sup>C × 3. SIF × 10. DMA × 12. WDT. A/D. Time base timer × 2. System error. Remote control × 4

## ■ Timer Counter

8-bit timer × 10

Reload-down count. Cascade connection possible (usable as a 16-bit to 32-bit timer)

16-bit timer × 6

Up-down count. Input capture. PWM output. Compare/capture register 2 channels

Time base timer × 1

Watchdog timer × 1

## ■ Serial interface

UART/Synchronous/Multi-master I<sup>2</sup>C interface selective × 3

UART/Synchronous interface selective × 2

## ■ Remote Control Interface

Remote control reception: Correspondence with AEHA (Association for Electric Home Appliances) format. Queued reception by low speed clock

## ■ DMA controller

Number of channels: 4 channels

Unit of transfer: 8/16/32 bits

Maximum transfer cycles: 65535

Starting factor: External interrupt. Timer. Serial transmission/reception. A/D conversion finish. I<sup>2</sup>C transmission/reception. Software.

Remote control data reception

Transfer method: 2-bus cycle transfer

Addressing modes: Fixed. Increment. Decrement

Transfer mode: Word transfer. Burst transfer. Intermittent transfer

## ■ I/O Pins

I/O 22 : (5 V I/O) Common use

59 : (3 V I/O) Common use

Input 1 : (3 V I/O) Common use

## ■ A/D converter

10-bit × 8 channels. 5 V input

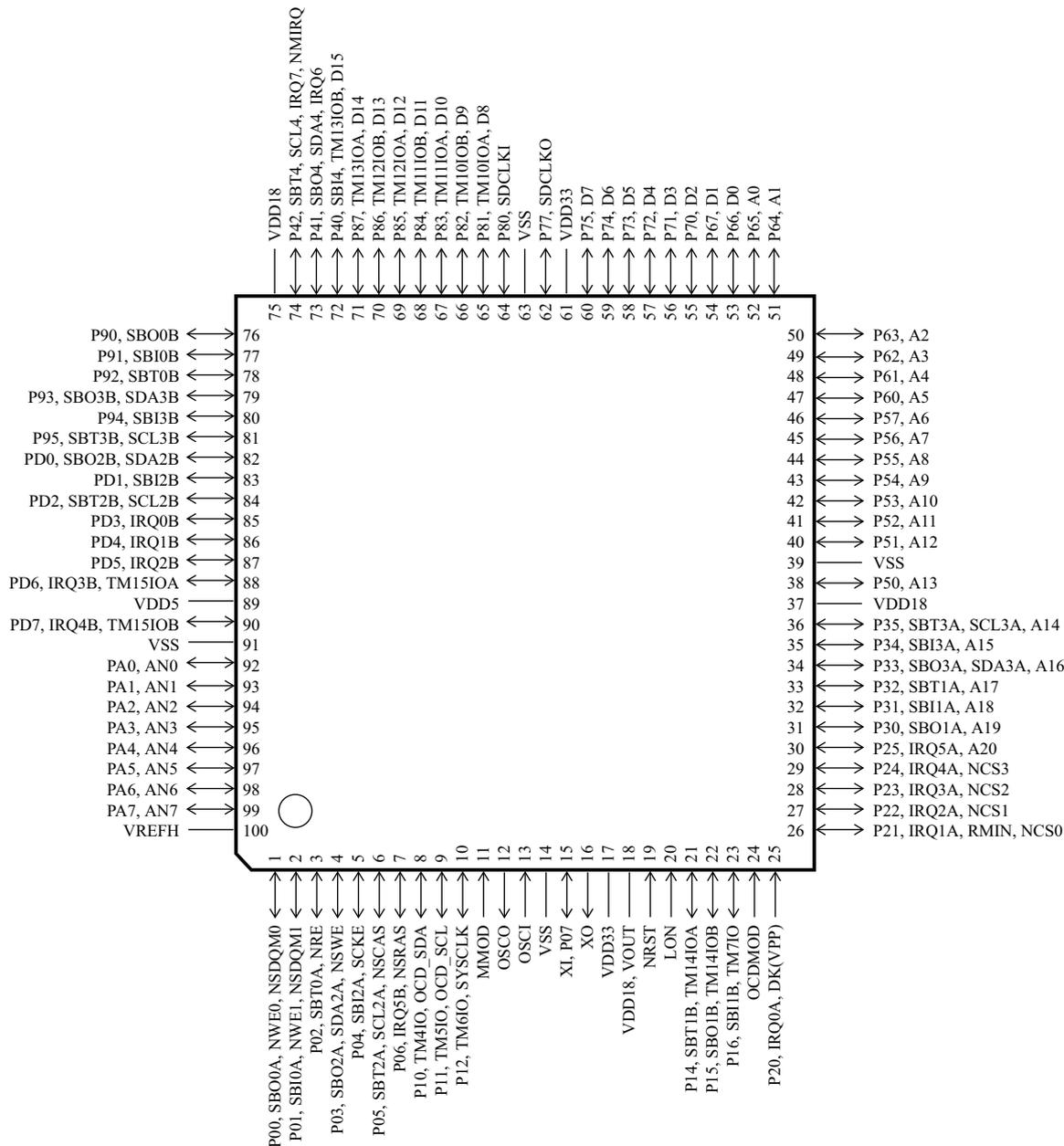
## ■ ROM Correction

8 channels

## ■ Electrical Characteristics (A/D converter characteristics)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
Non-linear error		VDD5 = VREFH = 3.3 V. VSS = 0 V			±4	LSB
Differential non-linearity error		VDD5 = VREFH = 5.0 V. VSS = 0 V			±4	LSB

■ Pin Assignment  
QFP100-P-1818B



Note) VDD5 = VDD33 to 5.5 V. VDD33 = 2.7 V to 3.6 V

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