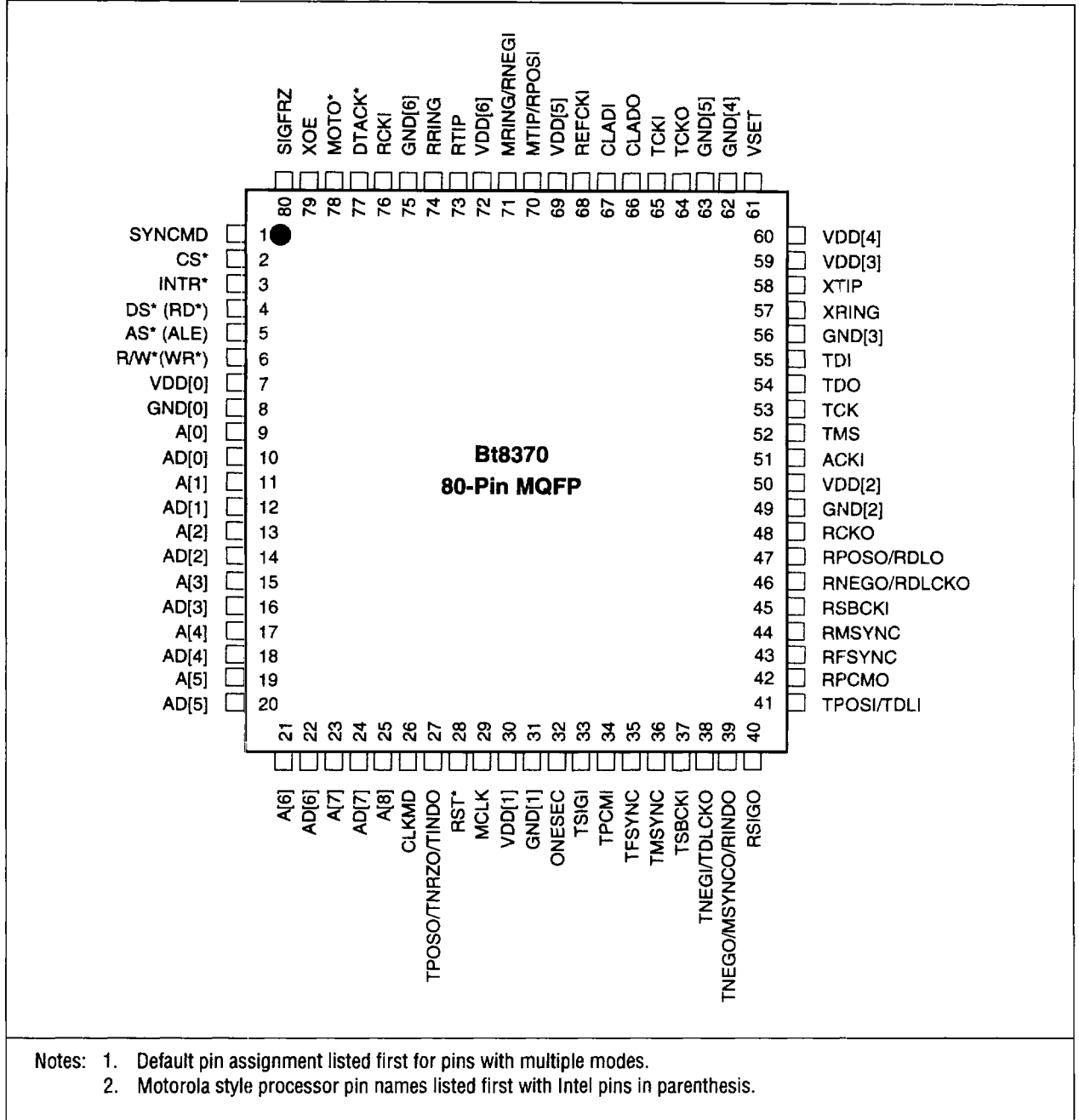# Pin Descriptions

Pin Assignments

Bt8370 is packaged in an 80-pin Metric Quad Flat Pack (MQFP). A pinout diagram of this device is illustrated in Figure 1. Figure 2 details a Bt8370 Logic Diagram. Pin labels, names, input/output functions, and descriptions are provided in Table 1.

The following input pins contain an internal pullup resistor (>50 KOhms) and may remain unconnected if the active high input state is desired:

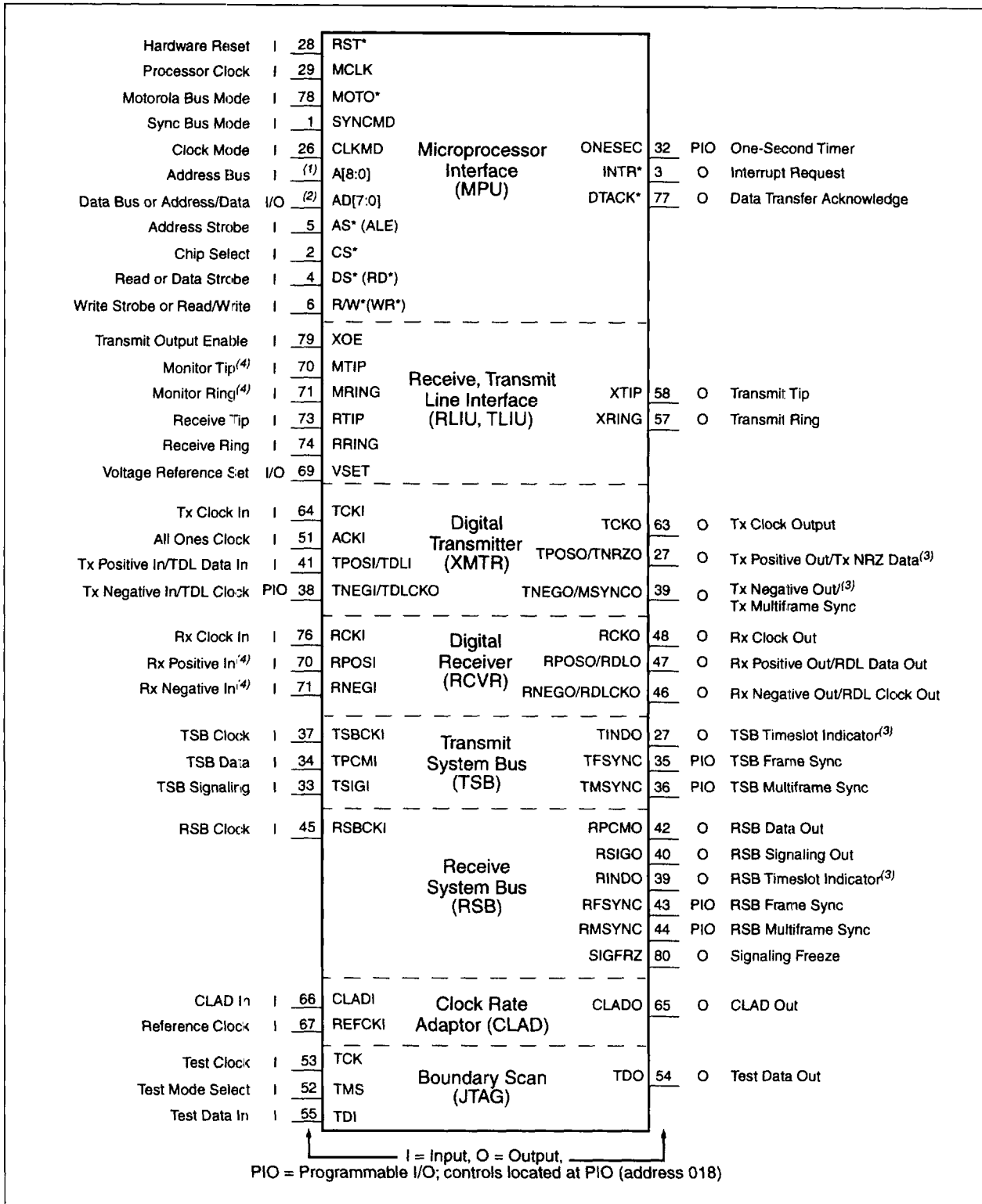|		
1	A[7:0];	Address lines unused in INTEL bus mode
2	XOE;	Active high enables analog bipolar output
3	MOTO*;	Pullup selects INTEL bus mode if unconnected
4	SYNCMD;	Pullup selects synchronous processor interface
5	RCKI;	Receive clock unused if analog inputs enabled
6	TDI;	Unused if JTAG not connected
7	TMS;	Disables JTAG if not connected
8	TCK;	Unused if JTAG not connected
9	RST*;	Disables hardware reset if not connected
10	TDLI;	Unused if no external data link
11	TSIGI;	Unused if not system supplied signaling

Figure 1. Bt8370 Pinout Diagram

Notes: 1. Default pin assignment listed first for pins with multiple modes.
2. Motorola style processor pin names listed first with Intel pins in parenthesis.

Figure 2. Bt8370 Logic Diagram

Hardware Reset	I	28	RST*					
Processor Clock	I	29	MCLK					
Motorola Bus Mode	I	78	MOTO*					
Sync Bus Mode	I	1	SYNCMD					
Clock Mode	I	26	CLKMD	Microprocessor	ONESEC	32	PIO	One-Second Timer
Address Bus	I	(1)	A[8:0]	Interface	INTR*	3	O	Interrupt Request
Data Bus or Address/Data	I/O	(2)	AD[7:0]	(MPU)	DTACK*	77	O	Data Transfer Acknowledge
Address Strobe	I	5	AS* (ALE)					
Chip Select	I	2	CS*					
Read or Data Strobe	I	4	DS* (RD*)					
Write Strobe or Read/Write	I	6	R/W*(WR*)					
Transmit Output Enable	I	79	XOE					
Monitor Tip[4]	I	70	MTIP	Receive, Transmit				
Monitor Ring[4]	I	71	MRING	Line Interface	XTIP	58	O	Transmit Tip
Receive Tip	I	73	RTIP	(RLIU, TLIU)	XRING	57	O	Transmit Ring
Receive Ring	I	74	RRING					
Voltage Reference Set	I/O	69	VSET					
Tx Clock In	I	64	TCKI	Digital	TCKO	63	O	Tx Clock Output
All Ones Clock	I	51	ACKI	Transmitter	TPOSO/TNRZO	27	O	Tx Positive Out/Tx NRZ Data[3]
Tx Positive In/TDL Data In	I	41	TPOSI/TDLI	(XMTR)				
Tx Negative In/TDL Clock	PIO	38	TNEGI/TDLCKO		TNEGO/MSYNCO	39	O	Tx Negative Out[3] Tx Multiframe Sync
Rx Clock In	I	76	RCKI	Digital	RCKO	48	O	Rx Clock Out
Rx Positive In[4]	I	70	RPOSI	Receiver	RPOSO/RDLO	47	O	Rx Positive Out/RDL Data Out
Rx Negative In[4]	I	71	RNEGI	(RCVR)	RNEGO/RDLCKO	46	O	Rx Negative Out/RDL Clock Out
TSB Clock	I	37	TSBCKI	Transmit	TINDO	27	O	TSB Timeslot Indicator[3]
TSB Data	I	34	TPCMI	System Bus	TFSYNC	35	PIO	TSB Frame Sync
TSB Signaling	I	33	TSIGI	(TSB)	TMSYNC	36	PIO	TSB Multiframe Sync
RSB Clock	I	45	RSBCKI		RPCMO	42	O	RSB Data Out
					RSIGO	40	O	RSB Signaling Out
				Receive	RINDO	39	O	RSB Timeslot Indicator[3]
				System Bus	RFSYNC	43	PIO	RSB Frame Sync
				(RSB)	RMSYNC	44	PIO	RSB Multiframe Sync
					SIGFRZ	80	O	Signaling Freeze
CLAD In	I	66	CLADI	Clock Rate	CLADO	65	O	CLAD Out
Reference Clock	I	67	REFCKI	Adaptor (CLAD)				
Test Clock	I	53	TCK	Boundary Scan				
Test Mode Select	I	52	TMS	(JTAG)	TDO	54	O	Test Data Out
Test Data In	I	55	TDI					

I = Input, O = Output,
PIO = Programmable I/O; controls located at PIO (address 018)

Notes: (1). Pins for A[8:0] = 9, 11, 13, 15, 17, 19, 21, 23, 25
(2). Pins for AD[7:0] = 10, 12, 14, 16, 18, 20, 22, 24
(3). Pins 27 and 39 shown twice for clarity, pin function controlled by PIO (addr 018).
(4). Pins 70 and 71 shown twice for clarity, pin function controlled by RDIGI (addr 020).

Table 1. Hardware Signal Definitions (1 of 8)

Pin Label	Signal Name	I/O	Definition
RST*	Hardware Reset	I	RST* low-to-high transition forces default registers to their power-up state and all PIO pins to the input state. RST* is not mandatory, since internal power on reset circuit performs an identical function. RST* may be applied asynchronously, but must remain asserted for a minimum of 2 clock cycles (external MCLK or internal 32 MHz) for the low-to-high transition to be sampled and detected (see also [RESET; addr 001]).
MCLK	Processor Clock	I	System applies MCLK in range of 8–36 MHz for external clock (CLKMD = 1) and synchronous bus modes (SYNCMD = 1). During internal clock modes (CLKMD = 0), Bt8370 uses an internally generated 32 MHz clock to control processor timing and MCLK input is ignored.
MOTO*	Motorola Bus Mode	I	Selects Intel- or Motorola-style microprocessor interface. DS*, R/W*, A[8:0], and AD[7:0] functions are affected. 0 = Motorola; AD[7:0] is data, A[8:0] is address, DS* is data strobe, and R/W* indicates the read (high) or write (low) data direction. 1 = Intel; AD[7:0] is multiplexed address/data, A[7:0] ignored, A[8] is address line, DS* is read strobe (RD*), and R/W* is write strobe (WR*).
SYNCMD	Sync Mode	I	Selects whether read/write cycle timing is synchronous with respect to MCLK. Supports Intel- or Motorola-style buses: 0 = Asynchronous Bus; Read data enable and write data input latch are asynchronously controlled by CS*, DS*, and R/W* signals. Latched write data is still synchronized internally to 32 MHz clock for transfer to addressed register. 1 = Synchronous Bus; Applicable only if the external clock is also selected (CLKMD = 1). MCLK rising edge samples CS*, DS*, and R/W* to determine valid read/write cycle timing. Allows zero wait state processor cycles for MCLK speeds up to 36 MHz, for M68000 type buses.
CLKMD	Clock Mode	I	Selects whether MCLK is enabled (high) or ignored (low). When enabled, MCLK frequency determines update rate of internal registers and sampling rate of CS*, DS*, and R/W* signals.
A[8:0]	Address Bus	I	AS* falling edge asynchronously latches A[8:0] (Motorola), or A[8] (Intel) to identify one register for subsequent read/write data transfer cycle.
AD[7:0]	Data Bus or Address Data	I/O	Multiplexed address/data (Intel) or only data (Motorola). Refer to MOTO* signal definition.
AS* (ALE)	Address Strobe	I	For all processor bus modes, AS* falling edge asynchronously latches address from A[8:0] (Motorola) or from A[8] and AD[7:0] (Intel). For sync modes (SYNCMD = 1), each read/write data cycle requires both AS* and CS* active low on MCLK rising edge.

(Left side vertical label: Microprocessor Interface (MPU))

Table 1. Hardware Signal Definitions *(2 of 8)*

	Pin Label	Signal Name	I/O	Definition
Microprocessor Interface (MPU)	CS*	Chip Select	I	Active-low enables read/write decoder. Active high ends current read or write cycle and places data bus output in high impedance.
	DS*(RD*)	Data Strobe or Read Strobe	I	Active-low read data strobe (RD*) for MOTO* = 1, or read/write data strobe (DS*) for MOTO* = 0.
	R/W*(WR*)	Read/Write Direction or Write Strobe	I	Active-low write data strobe (WR*) for MOTO* = 1, or read/write data select (R/W*) for MOTO = 0.
	ONESEC	One Second Timer	PIO	Controls or marks one-second interval used for status reporting. When input, the timer is aligned to ONESEC rising edge. When output, rising edge indicates start of each one-second interval. Typically one device in a multiline system is configured to output ONESEC to synchronize other Bt8370 status reports on a common one-second interval.
	INTR*	Interrupt Request	O	Open drain active low output signifies one or more pending interrupt requests. INTR* goes to high-impedance state with weak (>50 kOhm) internal pullup resistance after processor has serviced all pending interrupt requests.
	DTACK*	Data Transfer Acknowledge	O	Open drain active low output signifies in-progress data transfer cycle. DTACK* remains asserted (low) for as long as AS* and CS* are both active-low.
Line Interface Unit (LIU)	XOE	Transmit Output Enable	I	Active high input enables XTIP and XRING output drivers. Otherwise, both outputs are placed in high-impedance state. XOE contains internal pullup so that systems that don't require three-stated outputs can leave XOE unconnected.
	MTIP, MRING	Monitor Tip/Ring	I	Differential AMI inputs provide signal level monitoring at programmable short or long haul pulse template levels see [DPM_CSU; addr 020]. MTIP and MRING are typically connected to a backup or local XTIP/XRING output. If unused, MTIP and MRING are grounded. Optionally, MTIP/MRING are programmed to accept dual-rail digital data inputs at TTL/CMOS levels see [RDIGI; addr 020].
	RTIP, RRING	Receive Tip/Ring	I	Differential AMI data inputs for direct connection to receive transformer.
	VSET	Voltage Reference Set	I/O	Constant voltage output must be connected to an external 1% resistor equal to 12.4 kOhms to ground. Attached resistor sets internal precision current reference of 100 μA. A 15pF capacitor to ground, in parallel with the resistor, is optionally connected to improve noise immunity.
	XTIP, XRING	Transmit Tip/Ring	O	Complementary AMI data outputs for direct connection to transmit transformer. Optionally, both outputs are three-stated when XOE is negated.

Table 1. Hardware Signal Definitions (3 of 8)

Pin Label	Signal Name	I/O	Definition
TCKI	Tx Clock Input	I	Primary TX line rate clock applied on TCKI or the system chooses from one of four different clocks to act as TX clock source (see [CMUX; addr 01A]). The selected source is used to clock digital transmitter signals; TPOSI, TNEGI, TPOSO, TNEGO, TNRZO, MSYNCO, TDLI, and TDLCKO. If TSLIP bypassed, selected source also clocks TSB signals.
ACKI	All Ones Clock	I	System optionally applies ACKI to use for AIS transmission, in case the selected primary transmit clock source fails. ACKI is either manually or automatically switched to replace TCKI (see [AISCLK; addr 068]). Systems without an AIS clock should tie ACKI to ground.
TPOSI	TX Positive Rail Input	I	Line rate data input on falling edge of TCKI replaces all data that normally would be supplied by ZCS encoder. Bt8370 default power on state selects TPOSI/TNEGI as source for all transmitted XTIP/XRING output pulses, encoded as follows: TPOSI TNEGI TX Pulse Polarity 0 0 No pulse 0 1 Negative AMI pulse 1 0 Positive AMI pulse 1 1 Invalid Note: Software must set TDL_IO (addr 018) to enable normal data from internal transmitter.
TNEGI	TX Negative Rail Input	I	Line rate data input on TCKI falling edge, replaces all data that would otherwise be supplied by ZCS encoder. Refer to TPOSI signal definition.
TPOSO	TX Positive Rail Output	O	Line rate data output from ZCS encoder or JAT on rising edge of TCKO. Active-high marks transmission of a positive AMI pulse. Used to monitor transmit data or for systems that employ an external line interface unit.
TNEGO	TX Negative Rail Output	O	Line-rate data output from ZCS encoder or JAT on rising edge of TCKO. Active high marks transmission of a negative AMI pulse. Used to monitor transmit data or for systems that employ an external line interface unit.
TDLI	TX Data Link Input	I	Selected timeslot bits are sampled on TDLCKO falling edge for insertion into the transmit output stream during external data link applications.
TDLCKO	TX Data Link Clock	O	Gapped version of TCKI for external data link applications. TDLCKO high clock pulse coincides with low TCKI pulse interval during selected timeslot bits, else TDLCKO low (see [DL3_TS; addr 015]).
TCKO	TX Clock Output	O	Line rate clock used to align XTIP/XRING outputs. If transmit jitter attenuator (TJAT) is disabled, TCKO equals selected TCKI or ACKI. If TJAT is enabled, TCKO equals the jitter attenuated clock (JCLK).
TNRZO	TX Non Return to Zero Data	O	Line-rate data output from transmitter on rising edge of TCKI. TNRZO does not include ZCS encoded bipolar violations.
MSYNCO	TX Multiframe Sync	O	Active high for one TCKI clock cycle to mark the first bit of TX multiframe coincident with TNRZO. Output on rising edge of TCKI.

Row label (vertical): **Digital Transmitter (XMTR)**

Table 1. Hardware Signal Definitions *(4 of 8)*

	Pin Label	Signal Name	I/O	Definition
Digital Receiver (RCVR)	RCKI	RX Clock Input	I	Line rate clock samples RPOSI and RNEGI when RLIU configured to accept dual-rail digital data (see [RDIGI; addr 020]). Otherwise, RCKI is ignored.
	RPOSI	RX Positive Rail Input	I	Line rate data input on rising edge of RCKI. RPOSI and RNEGI levels are interpreted as received AMI pulses, encoded as follows: RPOSI RNEGI RX Pulse Polarity 0 0 No pulse 0 1 Negative AMI pulse 1 0 Positive AMI pulse 1 1 Invalid
	RNEGI	RX Negative Rail Input	I	Line rate data input on rising edge of RCKI. See RPOSI signal definition.
	RCKO	RX Clock Output	O	RPLL recovered line rate clock (RXCLK) or jitter attenuated clock (JCLK) output, based on programmed clock selection (see [JAT_CR; addr 002]).
	RPOSO	RX Positive Rail Output	O	Line rate data output on rising edge of RCKO. Active high indicates receipt of a positive AMI pulse on RTIP/RING inputs.
	RNEGO	RX Negative Rail Output	O	Line rate data output on rising edge of RCKO. Active high indicates receipt of a negative AMI pulse on RTIP/RING inputs.
	RDLO	RX Data Link Output	O	Line rate NRZ data output from receiver on falling edge of RCKO, all data from RLIU is represented at the RDLO pin. However, selective RDLO bit positions are also marked by RDLCKO for external data link applications.
	RDLCKO	RX Data Link Clock Output	O	Gapped version of RCKO for external data link applications. RDLCKO high clock pulse coincides with low RCKO pulse interval during selected timeslot bits, else RDLCKO low (see Figure 12, External Data Link).

Table 1. Hardware Signal Definitions (5 of 8)

	Pin Label	Signal Name	I/O	Definition
Transmit System Bus (TSB)	TSBCKI	TSB Clock Input	I	Bit clock and I/O signal timing for TSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from one of four different clocks to act as TSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals: TPCMI, TSIGI, TINDO; and sync signals: TFSYNC and TMSYNC (see [TPCM_NEG and TSYN_NEG; addr 0D4]). When configured to operate at twice the data rate, TSB clock is internally divided by 2 before clocking TSB data signals.
	TPCMI	TSB Data Input	I	Serial data formatted into TSB frames consisting of DS0 channel timeslots and optional Fbits. One group of 24 T1 timeslots or 32 E1 timeslots is selected from up to four available groups; data from the group is sampled by TSBCKI, then sent towards transmitter output. Timeslots are routed through transmit slip buffer (see [TSLIPn; addr 140–17F]) according to TSLIP mode (see [TSBI; addr 0D4]). Fbits are taken from the start of each TSB frame or from within an embedded timeslot (see [EMBED; addr 0D0]) and optionally inserted into the transmitter output (see [TFRM; addr 072] register).
	TSIGI	TSB Signaling Input	I	Serial data formatted into TSB frames containing ABCD signaling bits for each system bus timeslot. Four bits of TSIGI timeslot carry signaling state for each accompanying TPCMI timeslot. Signaling state of every timeslot is sampled during first frame of the TSB multiframe and then transferred into transmit signaling buffer [TSIGn; addr 120–13F].
	TINDO	TSB Timeslot Indicator	O	Active-high output pulse marks selective transmit system bus timeslots as programmed by SBCn [addr 0E0–0FF]. TINDO occurs on TSBCKI rising or falling edges as selected by TPCM_NEG (see [TSBI; addr 0D4]).
	TFSYNC	TSB Frame Sync	PIO	Input or output TSB frame sync (see [TFSYNC_IO; addr 018]). TFSYNC output is active high for one TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB frame and repeating once every 125 μs. When transmit framer is also enabled, TSB timebase and TFSYNC output frame alignment are established by transmit framer's examination of TPCMI serial data input. When TFSYNC is programmed as an input, the low-to-high signal transition is detected and used to align TSB timebase to programmed offset bit value. TSB timebase flywheels at 125 μs frame interval after the last TFSYNC is applied.
	TMSYNC	TSB Multiframe Sync	PIO	Input or output TSB multiframe sync (see [TMSYNC_IO; addr 018]). TMSYNC output is active high for one TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB multiframe and repeating once every 6 ms coincident with TFSYNC. When transmit framer is also enabled, TSB timebase and TMSYNC output multiframe alignment are established by transmit framer's examination of TPCMI serial data input. When TMSYNC is programmed as an input, the low-to-high signal transition is detected and used to align TSB timebase to programmed offset bit value and first frame of the multiframe. TSB timebase flywheels at 6 ms multiframe interval after the last TMSYNC is applied. If system bus applies TMSYNC input, TFSYNC input is not needed.

Table 1. **Hardware Signal Definitions** *(6 of 8)*

Pin Label	Signal Name	I/O	Definition
RSBCKI	RSB Clock Input	I	Bit clock and I/O signal timing for RSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from one of four different clocks to act as RSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals: RPCMO, RSIGO, RINDO; and sync signals: RFSYNC, RMSYNC (see [RPCM_NEG and RSYN_NEG; addr 0D1]). When configured to operate at twice the data rate, RSB clock is internally divided by 2 before clocking RSB data signals.
RPCMO	RSB Data Output	O	Serial data formatted into RSB frames consisting of DS0 channel timeslots, optional Fbits and optional ABCD signaling. Timeslots are routed through receive slip buffer (see [RSLIPn; addr 1C0–1FF]) according to RSLIP mode (see [RSBI; addr 0D1]). Data for each output timeslot is assigned sequentially from received timeslot data according to system bus channel programming (see [ASSIGN; addr 0E0–0FF]). Fbits are output at the start of each RSB frame or at the embedded timeslot location (see [EMBED; addr 0D0]). ABCD signaling is optionally inserted on a per-channel basis (see [INSERT; addr 0E0–0FF]) from the local signaling buffer (see [RLOCAL; addr 180–19F]) or from the receive signaling buffer [RSIGn; addr 1A0–1BF]. When enabled, robbed bit signaling or CAS reinsertion is performed according to T1/E1 mode: Eighth timeslot bit of every sixth T1 frame is replaced or the 4-bit signaling value in E1 timeslot 16 is replaced.
RSIGO	RSB Signaling Output	O	Serial data formatted into RSB frames consisting of ABCD signaling bits for each system bus timeslot. Four bits of RSIGO timeslot carry signaling state for each accompanying RPCMO timeslot. Local or through signaling bits are output in every frame for each timeslot and updated once per RSB multiframe, regardless of per-channel RPCMO signaling reinsertion.
RINDO	RSB Timeslot Indicator	O	Active high output pulse marks selective receive system bus timeslots as programmed by SBCn [addr 0E0–0FF]. RINDO occurs on RSBCKI rising or falling edges as selected by RPCM_NEG (see [RSBI; addr 0D1]).
RFSYNC	RSB Frame Sync	PIO	Input or output RSB frame sync (see [RFSYNC_IO; addr 018]). RFSYNC output is active high for one RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB frame and repeating once every 125 us. RSB timebase and RFSYNC output frame alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RFSYNC is programmed as an input, the low-to-high signal transition is detected and used to align RSB timebase to the programmed offset. RSB timebase flywheels at 125 μs frame interval after the last RFSYNC is applied.

Notes: 1. Note: All RSB and TSB outputs can be placed in high-impedance state (see SBI_OE; addr 0D0).

Table 1. Hardware Signal Definitions (7 of 8)

Pin Label	Signal Name	I/O	Definition
RMSYNC	RSB Multiframe Sync	PIO	Input or output RSB multiframe sync (see [RMSYNC_IO; addr 018]). RMSYNC output is active high for one RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB multiframe and repeating once every 6 ms coincident with RFSYNC. RSB timebase and RMSYNC output multiframe alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RMSYNC is programmed as an input, the low to high signal transition is detected and used to align RSB timebase to programmed offset and first frame of the multiframe. RSB timebase flywheels at 6 ms multiframe interval after the last RMSYNC is applied.
SIGFRZ	Signaling Freeze	O	Active high indicates that signaling bit updates are suspended for both receive signaling buffer [RSIGn; addr 1A0–1BF] and stack [STACK; addr 0DA] Register. SIGFRZ is clocked by RSB clock, goes high coincident with receive loss of frame alignment (see RLOF; addr 047) and returns low 6–9 ms after recovery of frame alignment.
CLADI	CLAD Input	I	Optional CLAD input timing reference used to phase lock CLADO and JCLK outputs to one of 44 different input clock frequencies selected in the range of 8 kHz to 65536 kHz (see [CLAD registers; addr 090–092]).
REFCKI	Reference Clock	I	System must apply a 10 MHz $\pm$ 50 ppm clock signal to act as frequency reference for internal Numerical Controlled Oscillator (NCO). REFCKI determines frequency accuracy and stability of CLADO and jitter attenuator (JCLK) clocks when the NCO operates in free running mode (see [JFREE; addr 002]). REFCKI is the baseband reference for all CLAD/JAT functions and is used internally to generate clocks of various frequency, locked to a selected receive, transmit or external clock. Hence, REFCKI is always required.
CLADO	CLAD Output	O	CLADO is configured to operate at one of 14 different clock frequencies (see [CSEL; addr 091]) that include T1, E1 or system bus rates. CLADO is typically programmed to supply RSB and TSB clocks which are phase locked to the selected transmit, receive or CLADI timing reference (see [JEN; addr 002 and CEN; addr 090]).

Row labels (vertical): *Receive System Bus (RSB)* applies to RMSYNC and SIGFRZ; *Clock Rate Adaptor (CLAD)* applies to CLADI, REFCKI, and CLADO.

Table 1. Hardware Signal Definitions (8 of 8)

	Pin Label	Signal Name	I/O	Definition
Test Access	TDI	JTAG Test Data Input	I	Test data input per IEEE Std 1149.1-1990. Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI can be left unconnected if it is not being used because it is pulled up internally.
	TMS	JTAG Test Mode Select	I	Active low test mode select input per IEEE Std 1149.1-1990. Internally pulled-up input signal used to control the test-logic state machine. Sampled on the rising edge of TCK. TMS can be left unconnected if it is not being used because it is pulled up internally.
	TDO	JTAG Test Data Output	O	Test data output per IEEE Std 1149.1-1990. Three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
	TCK	JTAG Test Clock	I	Test clock input per IEEE Std 1149.1-1990. Used for all test interface and internal test-logic operations. If unused, TCK should be pulled low.
Power Supply	VDD[6:0]	Power	I	+5 Vdc ±5%
	GND[6:0]	Ground	I	0 Vdc

Notes: 1. I = Input, O = Output
2. PIO = Programmable I/O; controls located at address 018.
3. Multiple signal names show mutually exclusive pin functions.
4. All output pins power up in the high-impedance state (see POE; addr 019, SBI_OE; addr 0D0).