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Circuit Note
CN-0109

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Devices Connected/Referenced	
AD9958/ AD9858	500 MSPS/1 GSPS Direct Digital Synthesizer (DDS)
AD9515	Clock Distribution IC and Pin Programmable Mini-Divider
AD6645	14-Bit, 80 MSPS/105 MSPS ADC

Low Jitter Sampling Clock Generator for High Performance ADCs Using the AD9958/AD9858 500 MSPS/1GSPS DDS and AD9515 Clock Distribution IC

CIRCUIT FUNCTION AND BENEFITS

This circuit uses a direct digital synthesizer (DDS) with sub-Hertz tuning resolution as a low jitter sampling clock source for high performance ADCs. The AD9515 clock distribution IC provides PECL logic levels to the ADC. However, the AD9515 internal divider feature also allows the DDS to run at a higher frequency into the AD9515 front end, effectively increasing input slew rate. A higher slew rate into the AD9515 input squaring circuit can help reduce broadband jitter in the clock path.

Jitter on the ADC sampling clock produces degradation in the overall signal-to-noise ratio (SNR). The relationship is given by Equation 1.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f t_j}\right) \quad (1)$$

where f is the full-scale analog input frequency, and t_j is the rms jitter. "SNR" in Equation 1 is the SNR due solely to clock jitter and does not depend on the resolution of the ADC.

The following data supports low jitter attainable from a DDS in clocking applications. Further details on Equation 1 and its use for evaluating the jitter on ADC sampling clocks can be found in Application Note AN-501.

CIRCUIT DESCRIPTION

The circuit configuration in Figure 1 shows a DDS-based clock generator, consisting of a DDS followed by a reconstruction filter and an AD9515 clock distribution IC, used to provide the sampling clock for an analog-to-digital converter (ADC). The DDS sampling clock is derived from a Rohde and Schwarz SMA signal generator. The jitter measurement was made by using the clock derived from the DDS and the AD9515 as the sampling clock for the high performance AD6645 14-bit, 80 MSPS/105 MSPS ADC. The analog input signal for the ADC is a filtered 170.3 MHz sine wave derived from a low jitter Wenzel crystal oscillator (www.wenzel.com). Data was taken on two different DDSes: the AD9958 (500 MSPS) and the AD9858 (1 GSPS).

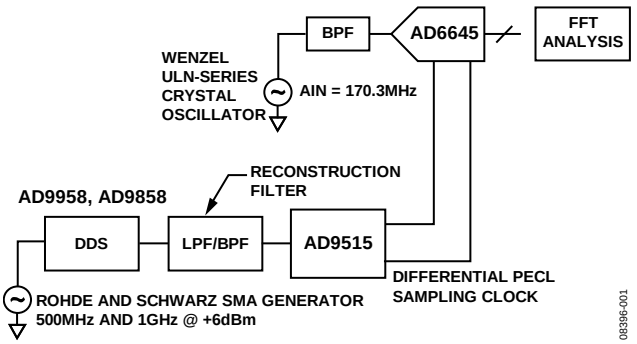

Figure 1. DDS-Based ADC Sampling Clock Generator (Simplified Diagram)

By evaluating the contribution of the ADC's differential non-linearity and thermal noise and then applying the DDS-based clock and measuring the ADC SNR, the added jitter attributable to the DDS-based clock can be derived. For more details on the measurement setup and the jitter calculations, refer to Application Note AN-823. Also, Application Note AN-837 is instructive for designing DAC reconstruction filters with optimal stop-band performance.

Table 1 shows data for the AD9958 test results. The data confirms that better jitter performance is achieved as the frequency, or slew rate, of the DDS output frequency is increased and as the DDS output filter pass band is decreased. Table 2 shows the AD9858 with a 5% band-pass filter, a 225 MHz low-pass filter, and various levels of DDS output power. As expected, lower jitter is achieved as power is increased and bandwidth reduced. With a 5% band-pass filter, the majority of the spurs from the DAC are attenuated. The jitter in this case is much more dependent on noise coupling between the DAC output and the limiter input. This is proven by the strong correlation between jitter reduction and increased

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slew rate. Note that rms jitter values consistently less than 1 ps can be achieved using the AD9858 circuit.

These circuits must be constructed on multilayer PC boards with large area ground planes using proper grounding, layout, and decoupling techniques (see MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and MT-101 Tutorial, *Decoupling Techniques*) in order to achieve these performance levels. Consult the evaluation board documentation for the AD9958, AD9858, AD9515, and AD6645 for more guidance.

Table 1. Jitter Response of AD9958 and AD9515 vs. f_{OUT}, Power, Frequency, and Filter BW

Product	DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter (MHz)	AD9515 Divider Output Setting	AD9515 Output Frequency (MHz)	Jitter (rms) (ps)
AD9958/AD9515	500	38.88	−3.6	200 LPF	1	38.88	4.1
AD9958/AD9515	500	38.88	−3.6	200 LPF	2	19.44	4.1
AD9958/AD9515	500	38.88	−4.7	47 LPF	1	38.88	2.4
AD9958/AD9515	500	38.88	−4.7	47 LPF	2	19.44	2.4
AD9958/AD9515	500	38.88	−3.3	5% BPF	1	38.88	1.5
AD9958/AD9515	500	38.88	−3.3	5% BPF	2	19.44	1.5
AD9958/AD9515	500	77.76	−3.8	200 LPF	1	77.76	2.5
AD9958/AD9515	500	77.76	−3.8	200 LPF	2, 4	38.88, 19.44	2.5
AD9958/AD9515	500	77.76	−4.9	85 LPF	1	77.76	1.5
AD9958/AD9515	500	77.76	−4.9	85 LPF	2, 4	38.88, 19.44	1.5
AD9958/AD9515	500	77.76	−3.8	5% BPF	1	77.76	1.1
AD9958/AD9515	500	77.76	−3.8	5% BPF	2, 4	38.88, 19.44	1.1
AD9958/AD9515	500	155.52	−5.5	200 LPF	2	77.76	1.5
AD9958/AD9515	500	155.52	−5.5	200 LPF	4, 8	38.88, 19.44	1.5
AD9958/AD9515	500	155.52	−5.6	5% BPF	2	77.76	0.68
AD9958/AD9515	500	155.52	−5.6	5% BPF	4, 8	38.88, 19.44	0.68

Table 2. Jitter Response of AD9858 and AD9515 vs. f_{OUT}, Power, Frequency, and Filter BW

Product	DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter (MHz)	AD9515 Divider Output Setting	AD9515 Output Frequency (MHz)	Jitter (rms) (ps)
AD9858/AD9515	1000	155.52	+7.7	225 LPF	2	77.76	0.56
AD9858/AD9515	1000	155.52	+7.7	225 LPF	4,8	38.88, 19.44	0.56
AD9858/AD9515	1000	155.52	+7.7	5% BPF	2	77.76	0.33
AD9858/AD9515	1000	155.52	+7.7	5% BPF	4, 8	38.88, 19.44	0.33
AD9858/AD9515	1000	155.52	+2.6	225 LPF	2	77.76	0.63
AD9858/AD9515	1000	155.52	+2.6	225 LPF	4, 8	38.88, 19.44	0.63
AD9858/AD9515	1000	155.52	+1.1	5% BPF	2	77.76	0.42
AD9858/AD9515	1000	155.52	+1.1	5% BPF	4, 8	38.88, 19.44	0.42
AD9858/AD9515	1000	155.52	−3.2	225 LPF	2	77.76	0.73
AD9858/AD9515	1000	155.52	−3.2	225 LPF	4, 8	38.88, 19.44	0.73
AD9858/AD9515	1000	155.52	−4.6	5% BPF	2	77.76	0.64
AD9858/AD9515	1000	155.52	−4.6	5% BPF	4, 8	38.88, 19.44	0.64

COMMON VARIATIONS

Analog Devices offers a variety of direct digital synthesizer, clock distribution chips, and clock buffers to build a DDS-based clock generator. Refer to www.analog.com/dds and www.analog.com/clock for more information.

LEARN MORE

AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*. Analog Devices.

AN-823 Application Note, *Direct Digital Synthesizers in Clocking Applications*. Analog Devices.

AN-837 Application Note, *DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance*. Analog Devices.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 6 and 7.

Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 2, "Optimizing Data Converter Interfaces."

Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 3, "DACs, DDSs, PLLs, and Clock Distribution."

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets and Evaluation Boards

AD6645 Data Sheet.

AD9515 Data Sheet.

AD9858 Data Sheet.

AD9958 Data Sheet.

AD6645 Evaluation Board.

AD9515 Evaluation Board.

AD9858 Evaluation Board.

AD9958 Evaluation Board.

REVISION HISTORY

7/09—Revision 0: Initial Version