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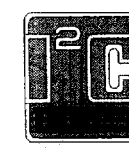


1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1 kbyte SDR-RAM. External program memory is addressable up to 128 kbytes
- +2.7 to +5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- Easy interfacing with radio circuits, operating at other supply voltages (RF supply pin with level shifter for RF signals)
- On-chip comparator for use as data-slicer
- Low power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- Up to two A-law channels
- Network echo suppressor
- Support of local corded handset with handsfree feature
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Automatic gain control
- Direct connection to universal codec PCD5096
- Conference between IOM-2 buffer(s) and two handsets.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5093 is designed as GAP-compliant basestation chip for ISDN or n lines (PCD5096) business systems. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5093H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM

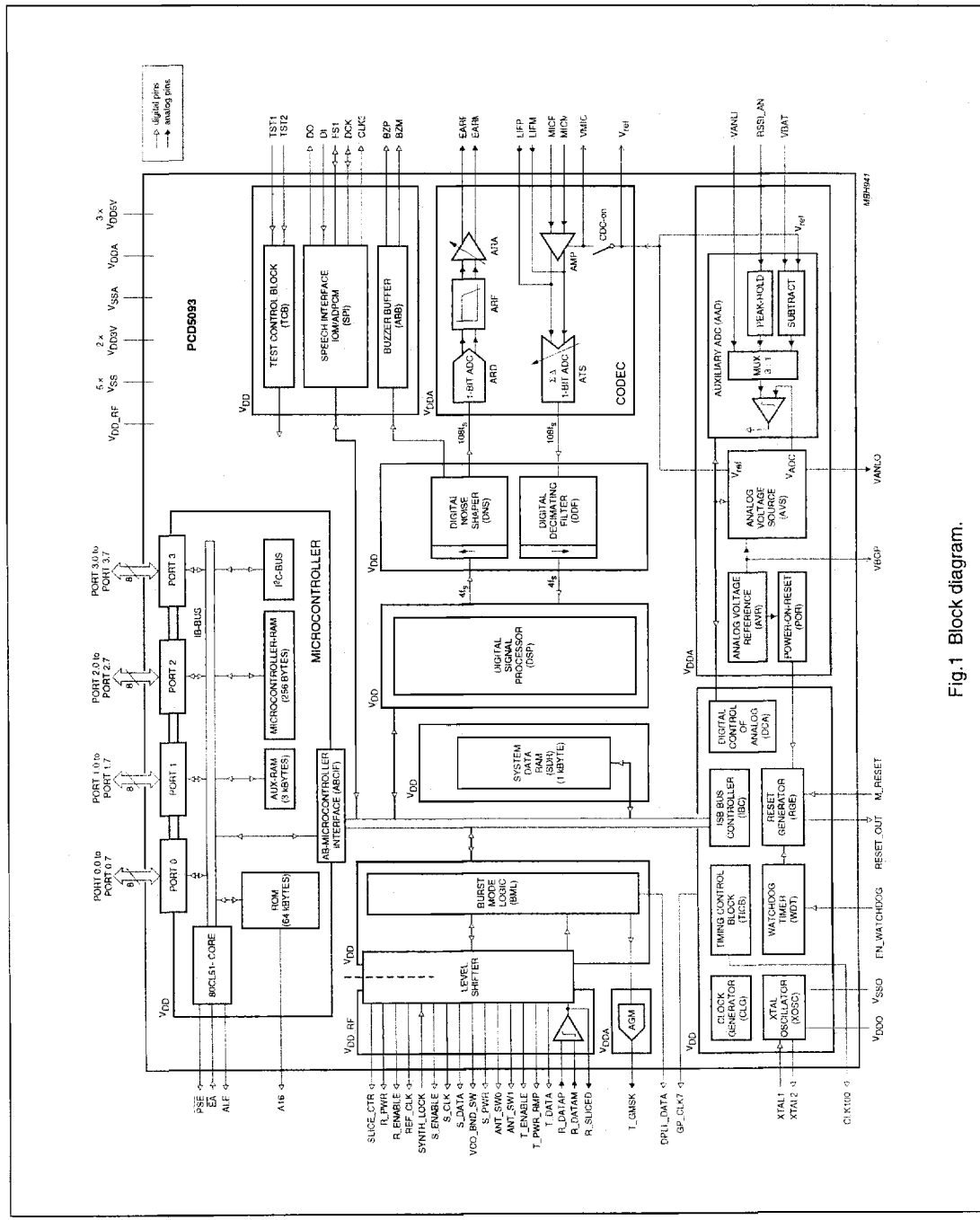


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

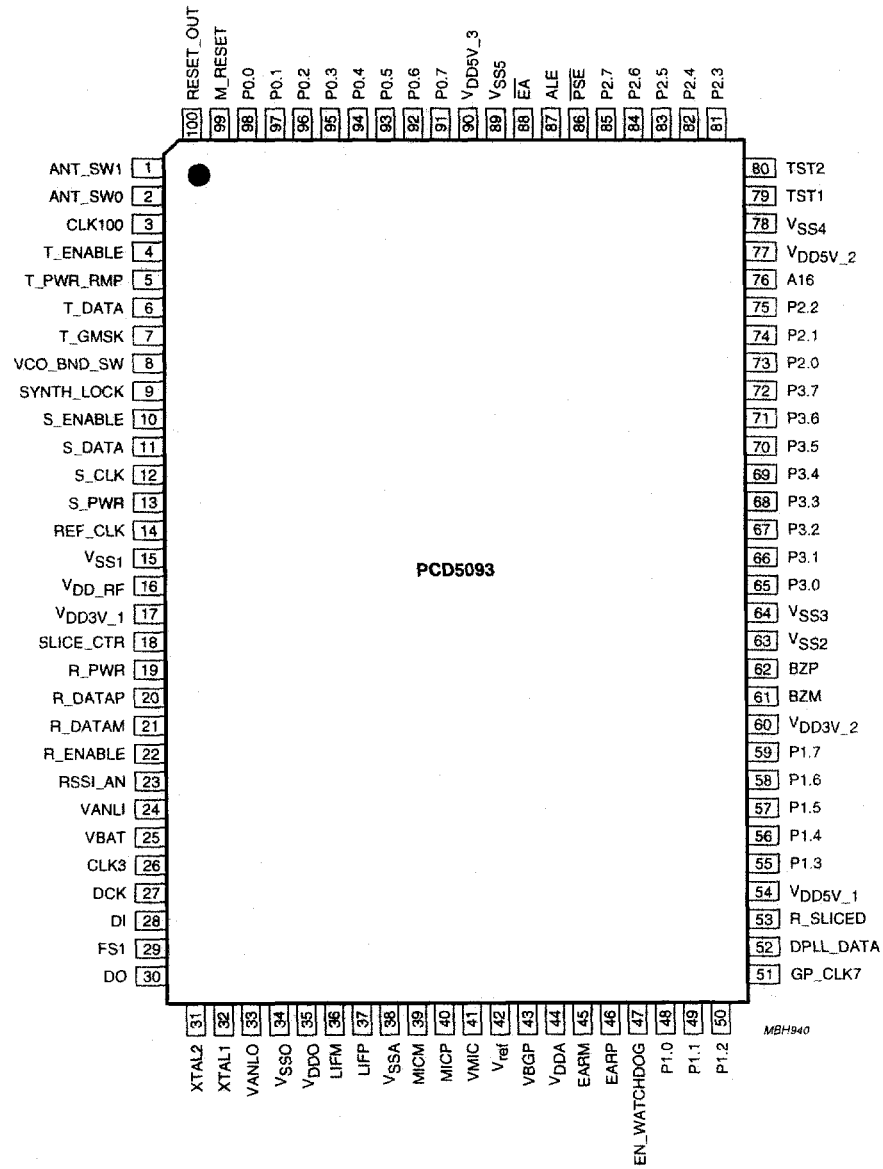


Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

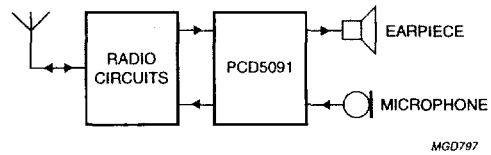
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from D/A converter

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	watchdog enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

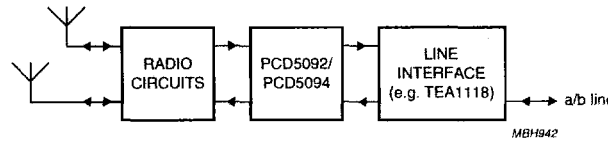
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

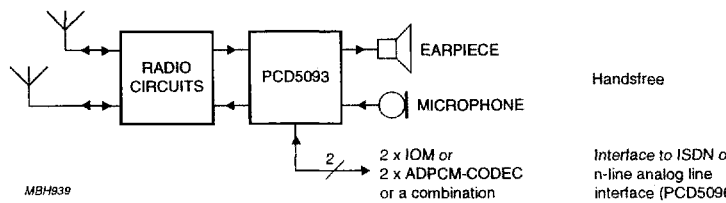
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Basestation with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base(PCD5093) with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.3 Block diagrams of DECT systems with PCX509x.