



1.0Amp. Surface Mount Schottky Barrier Diodes

CSOD120LSH

Features

- For surface mounted applications.
- For use in low voltage, high frequency inverters, free wheeling, and polarity protection applications
- Plastic material used carries Underwriters Laboratory Flammability Classification 94V-0
- Low leakage current
- High surge capability
- High temperature soldering: 250°C/10 seconds at terminals
- Exceeds environmental standards of MIL-S-19500/228
- RoHS compliant package

Mechanical Data

- Case: Molded plastic, JEDEC SOD-123.
- Terminals: Pure tin plated, solderable per MIL-STD-202 method 208
- Polarity: Indicated by cathode band.
- Weight: 0.04 gram approximately

Maximum Ratings and Electrical Characteristics

(Rating at 25°C ambient temperature unless otherwise specified.)

Parameter	Symbol	Limits	Units
Repetitive peak reverse voltage	V _{RRM}	20	V
Maximum RMS voltage	V _{RMS}	14	V
Maximum DC blocking voltage	V _R	20	V
Maximum instantaneous forward voltage, I _F =1A (Note 1)	V _F	0.45	V
Average forward rectified current	I _O	1	A
Peak forward surge current @8.3ms single half sine wave superimposed on rated load (JEDEC method)	I _{FSM}	10	A
Maximum DC reverse current V _R =V _{RRM} , T _J =25°C (Note 1) V _R =V _{RRM} , T _J =100°C (Note 1)	I _R	0.3 10	mA mA
Maximum thermal resistance, Junction to ambient	R _{th,JA}	250(typ)	°C/W
Diode junction capacitance @ f=1MHz and applied 5V reverse voltage	C _D	35 (typ)	pF
Storage temperature range	T _{stg}	-65 ~ +150	°C
Operating temperature range	T _J	-50 ~ +100	°C

Notes : 1.Pulse test, pulse width=300 μ sec, 2% duty cycle

Characteristic Curves

Fig. 1 Forward Current Derating Curve

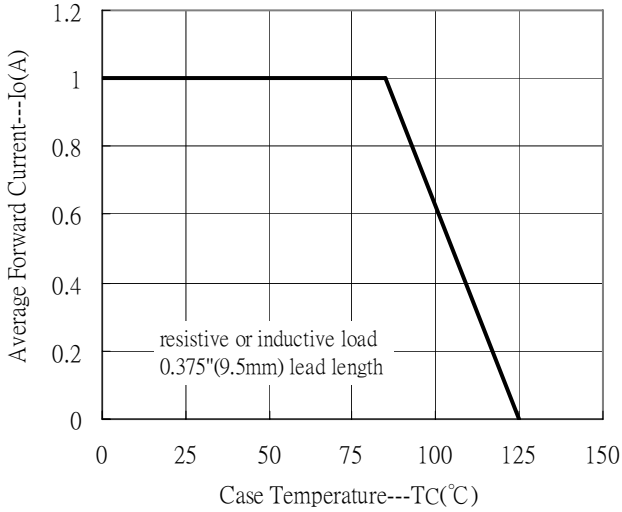


Fig 2. Forward Characteristics

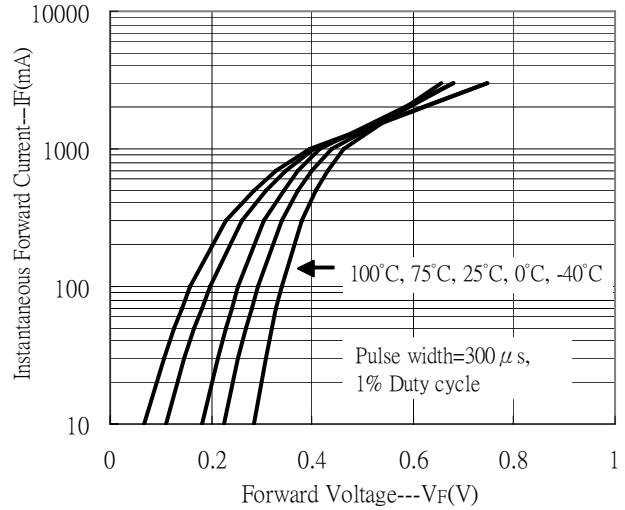


Fig. 3 Typical Junction Capacitance

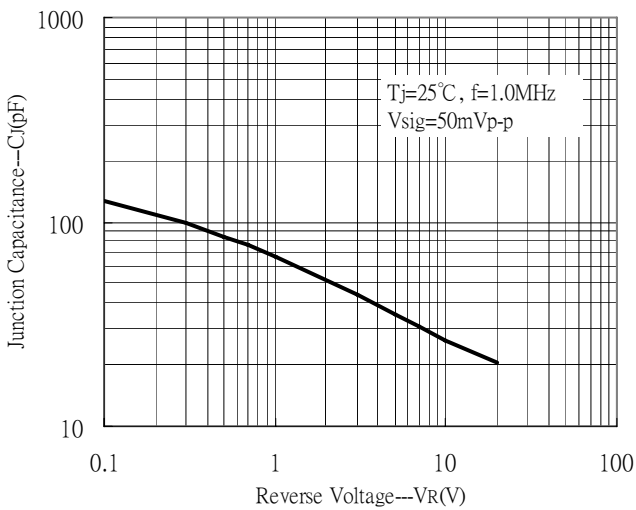
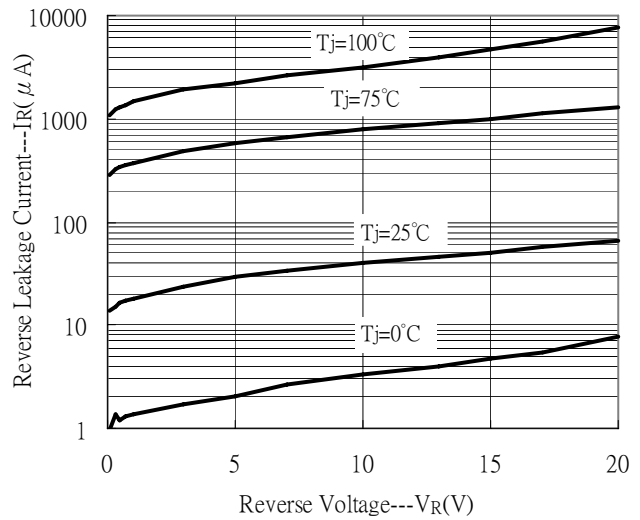
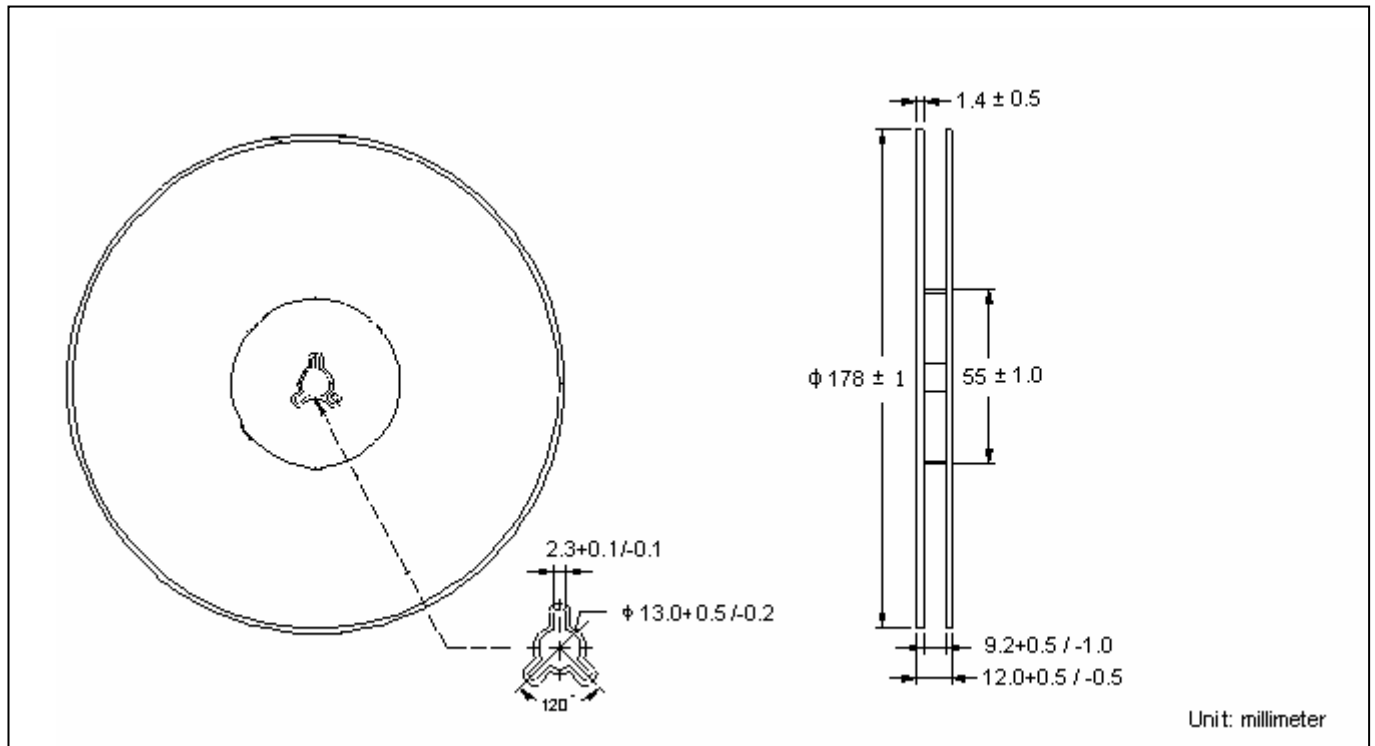


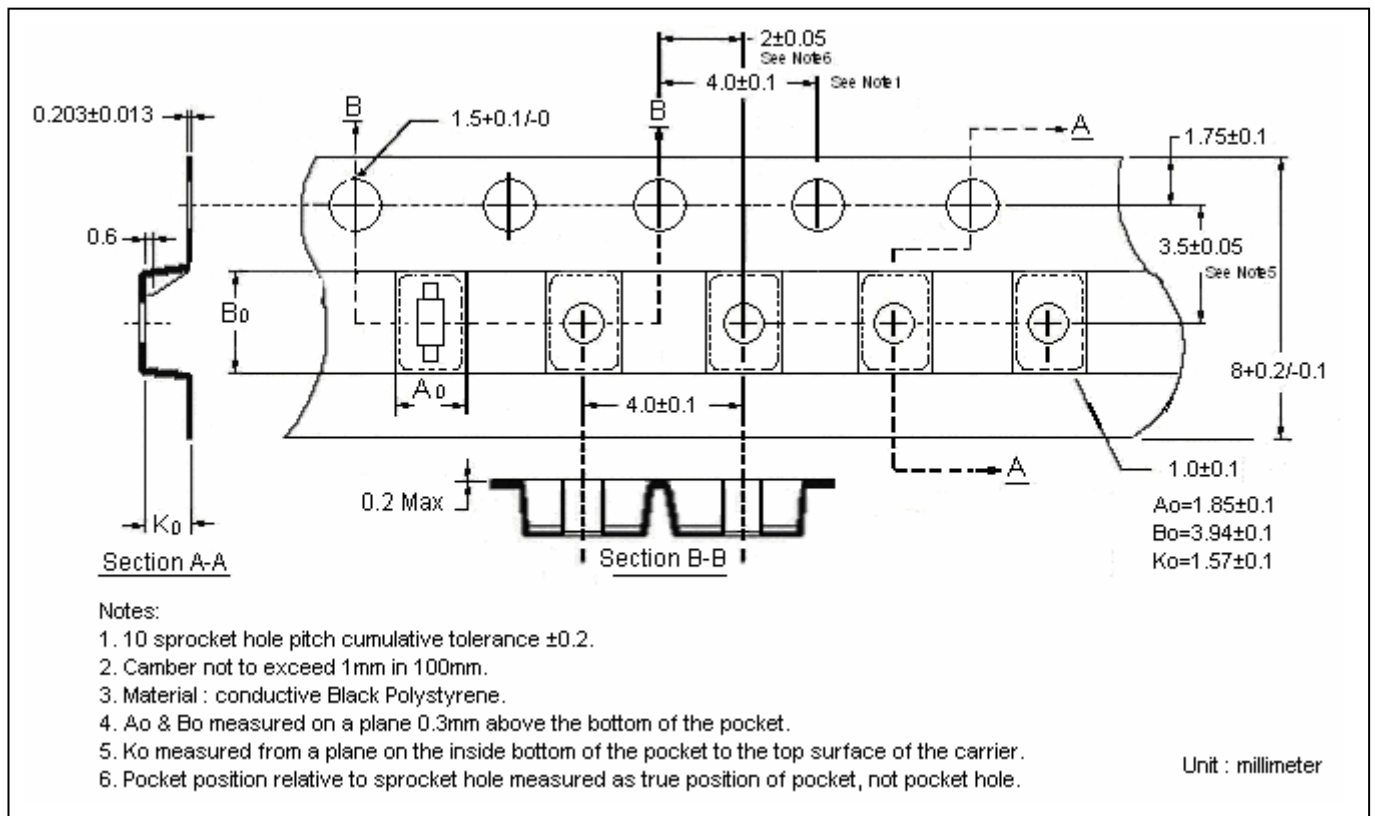
Fig. 4 Typical Reverse Characteristics



Reel Dimension



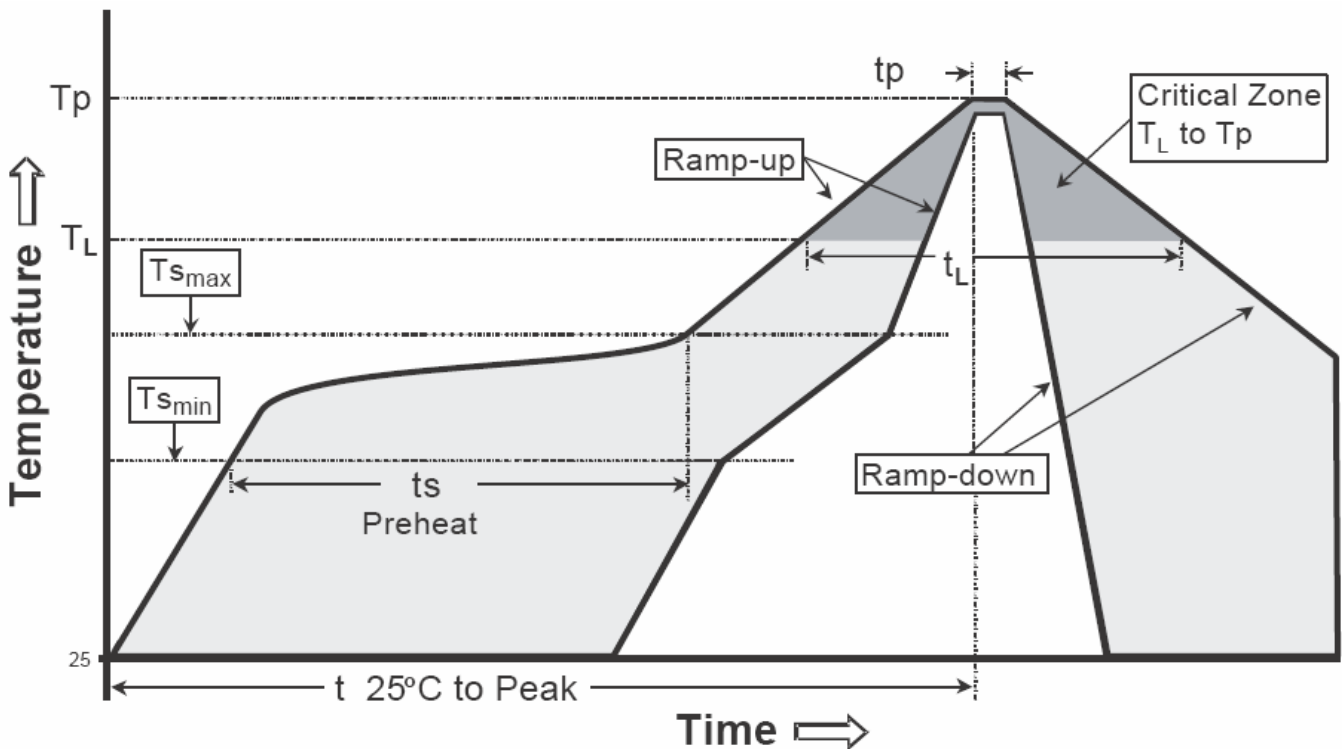
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

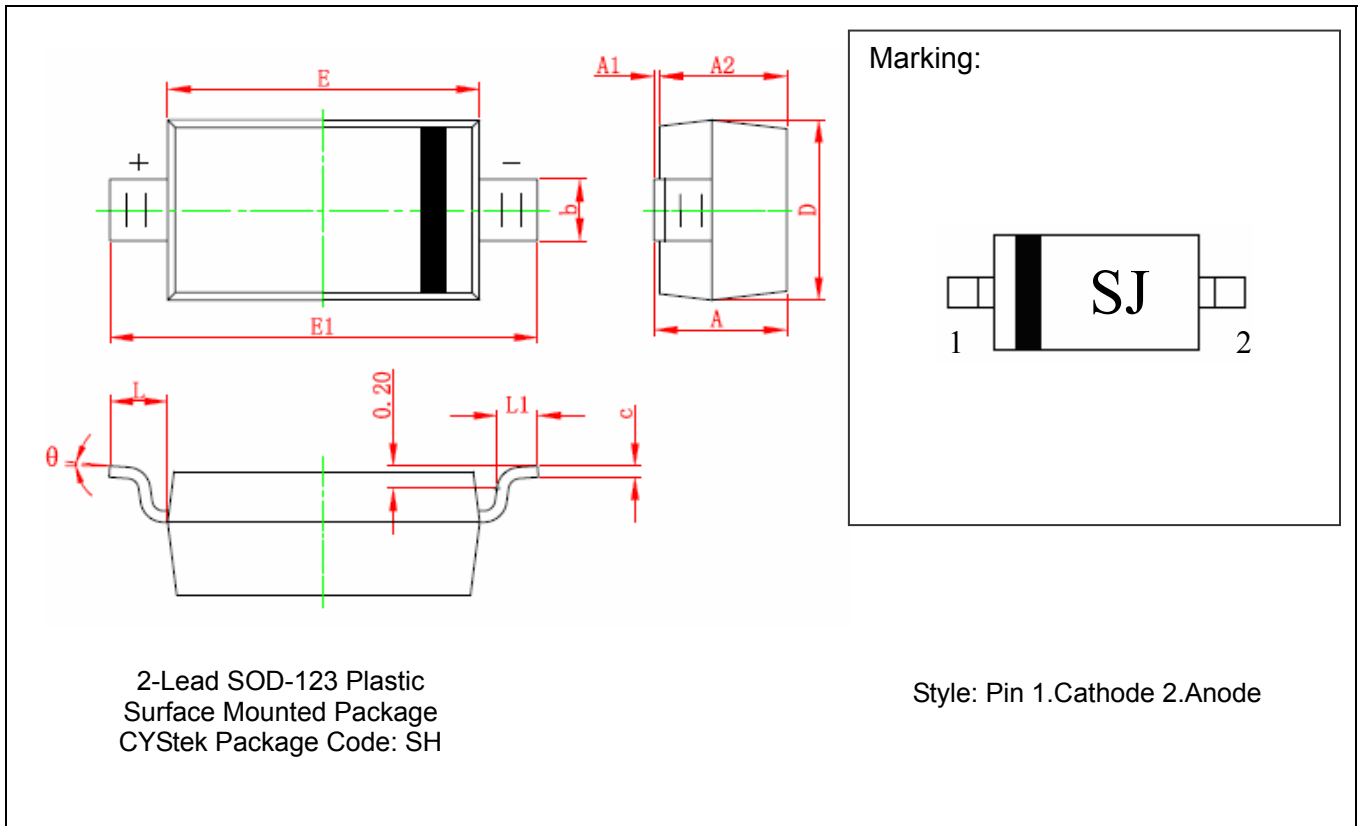
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOD-123 Dimension



2-Lead SOD-123 Plastic
 Surface Mounted Package
 CYStek Package Code: SH

Style: Pin 1.Cathode 2.Anode

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049	E	2.600	2.800	0.102	0.110
A1	0.000	0.100	0.000	0.004	E1	3.550	3.850	0.140	0.152
A2	1.050	1.115	0.041	0.045	L	0.500 REF		0.020 REF	
b	0.450	0.650	0.018	0.026	L1	0.250	0.450	0.010	0.018
c	0.080	0.150	0.003	0.006	θ	0°	8°	0°	8°
D	1.500	1.700	0.059	0.067					

Notes: 1.Controlling dimension : millimeters.
 2.Lead thickness specified per L/F drawing with solder plating.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.