TY Semicondutor®

Product specification

FDN359BN

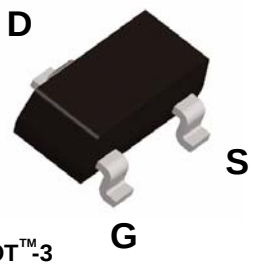
General Description

This N-Channel Logic Level MOSFET is produced using Fairchild's Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

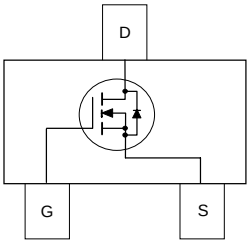
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 2.7 A, 30 V. $R_{DS(ON)}$= 0.046 Ω @ V_{GS} = 10 V
  $R_{DS(ON)}$= 0.060 Ω @ V_{GS} = 4.5 V
- Very fast switching speed.
- Low gate charge (5nC typical)
- High performance version of industry standard SOT-23 package. Identical pin out to SOT-23 with 30% higher power handling capability.



SuperSOT™-3



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Maximum Drain Current – Continuous	(Note 1a)	2.7	A
	– Pulsed		15	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
359B	FDN359BN	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C		21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		T_J = -55°C			10	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C		–4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 2.7 A V_{GS} = 4.5 V, I_D = 2.4 A V_{GS} = 10 V, I_D = 2.7 A, T_J = 125°C		0.026 0.032 0.033	0.046 0.060 0.075	Ω
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 2.7 A		11		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		485	650	pF
C_{oss}	Output Capacitance			105	140	pF
C_{rss}	Reverse Transfer Capacitance			65	100	pF
R_G	Gate Resistance	f = 1.0 MHz		1.8		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		7	14	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			20	35	ns
t_f	Turn–Off Fall Time			2	4	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 2.7 A, V_{GS} = 5 V		5	7	nC
Q_{gs}	Gate–Source Charge			1.3		nC
Q_{gd}	Gate–Drain Charge			1.8		nC

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				0.42	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note 2)		0.7	1.2	V
trr	Diode Reverse Recovery Time	IF = 2.7A, diF/dt = 100 A/µs		12	20	ns
Qrr	Diode Reverse Recovery Charge			3	5	nC

otes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.

b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%