

N-Channel Logic Level Enhancement Mode Power MOSFET

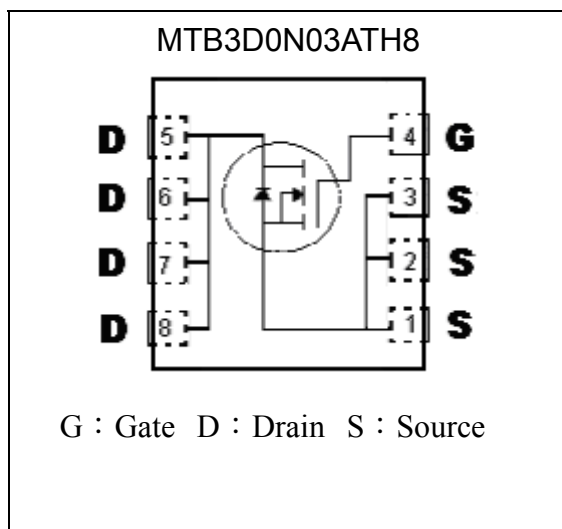
MTB3D0N03ATH8

BV_{DSS}	30V
I_D	75A
R_{DS(ON)}@ V_{GS}=10V, I_D=30A	2.9 mΩ (typ)
R_{DS(ON)}@ V_{GS}=4.5V, I_D=24A	4.0 mΩ (typ)

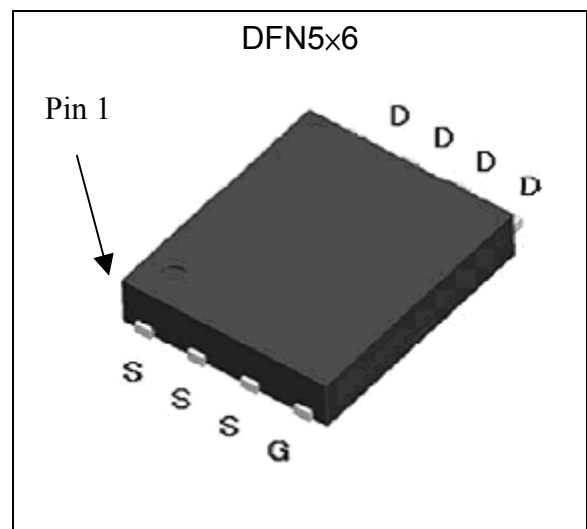
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Dynamic dv/dt rating
- Repetitive Avalanche Rated
- Pb-free lead plating and Halogen-free package

Symbol

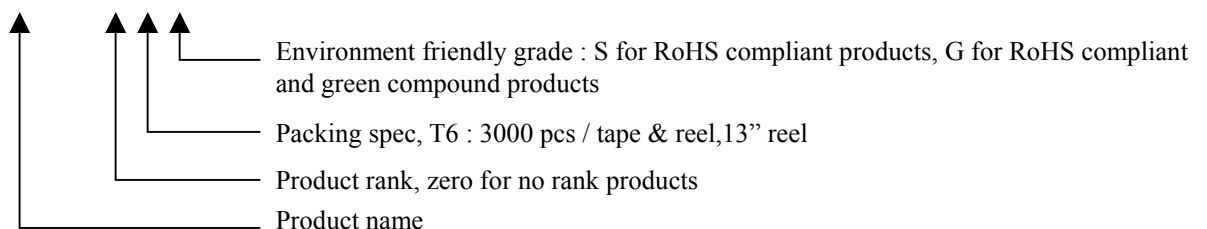


Outline



Ordering Information

Device	Package	Shipping
MTB3D0N03ATH8-0-T6-G	DFN 5 × 6 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @ T _C =25°C, V _{GS} =10V	I _D	75	A	
Continuous Drain Current @ T _C =100°C, V _{GS} =10V		47		
Pulsed Drain Current	I _{DM}	160 *1		
Avalanche Current	I _{AS}	53		
Avalanche Energy @ L=0.1mH, I _D =53A, R _G =25Ω	E _{AS}	140	mJ	
Repetitive Avalanche Energy @ L=0.05mH	E _{AR}	40 *2		
Total Power Dissipation	P _D	T _C =25°C	50	W
		T _C =100°C	20	
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+150	°C	

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=40A, Rated V_{DS}=30V N-CH

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	50 *3	°C/W

- Note : 1. Pulse width limited by maximum junction temperature
 2. Duty cycle ≤ 1%
 3. Surface mounted on 1 in² copper pad of FR-4 board, t ≤ 10s; 125°C/W when mounted on minimum copper pad.

Characteristics (T_C=25°C, unless otherwise specified)

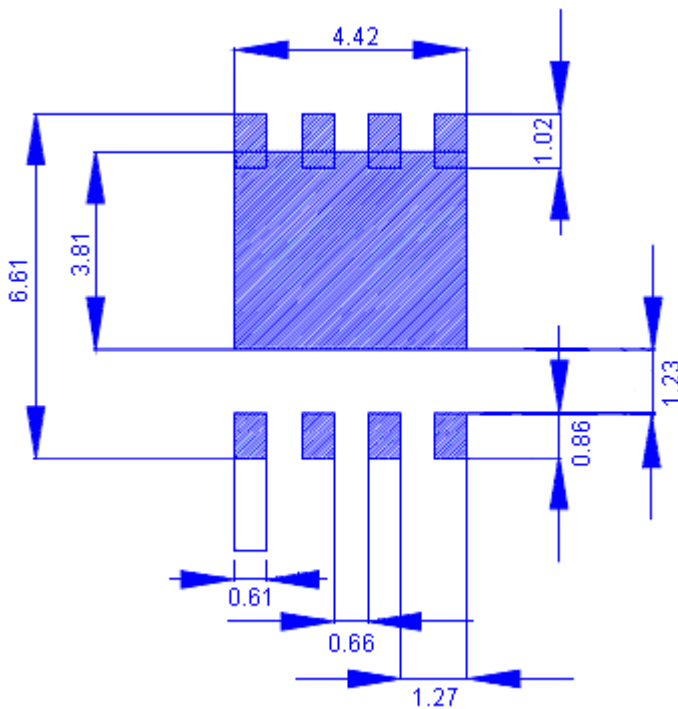
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250μA
V _{GS(th)}	1.0	1.7	2.5	V	V _{DS} = V _{GS} , I _D =250μA
G _{FS} *1	-	40	-	S	V _{DS} = 5V, I _D =24A
I _{GSS}	-	-	±100	nA	V _{GS} =±20
I _{DSS}	-	-	1	μA	V _{DS} = 24V, V _{GS} = 0
	-	-	25		V _{DS} = 20V, V _{GS} = 0, T _j =125°C
R _{DS(ON)} *1	-	2.9	4.0	mΩ	V _{GS} = 10V, I _D =30A
	-	4.0	6.0	mΩ	V _{GS} = 4.5V, I _D =24A
Dynamic					
C _{iss}	-	2747	-	pF	V _{GS} =0V, V _{DS} =15V, f=1MHz
C _{oss}	-	436	-		
C _{rss}	-	341	-		

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Qg (VGS=10V) *1, 2	-	38	-	nC	VDS=15V, VGS=10V, ID=30A
Qg (VGS=4.5V) *1, 2	-	16.9	-		
Qgs *1, 2	-	5.1	-		
Qgd *1, 2	-	10	-		
td(ON) *1, 2	-	13	-	ns	VDS=15V, ID=24A, VGS=10V, RGS=2.7Ω
tr *1, 2	-	8	-		
td(OFF) *1, 2	-	27	-		
tf *1, 2	-	12	-		
Rg	-	2.2	-	Ω	VGS=15mV, VDS=0V, f=1MHz
Source-Drain Diode					
IS *1	-	-	75	A	
ISM *3	-	-	150		
VSD *1	-	-	1.3	V	IF=30A, VGS=0V
trr	-	30	-	ns	IF=IS, dIF/dt=100A/μs
Qrr	-	10	-	nC	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

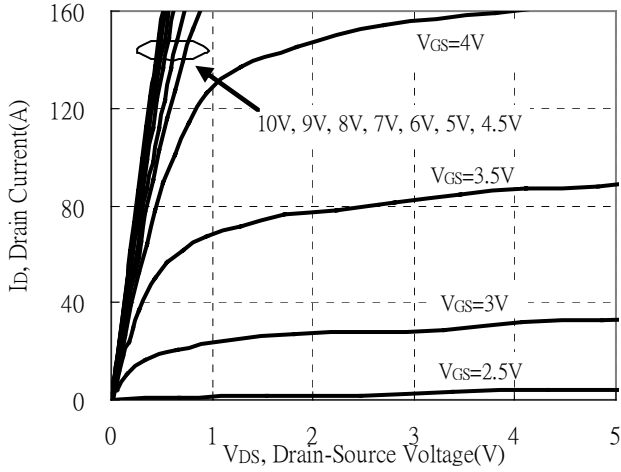
Recommended Soldering Footprint



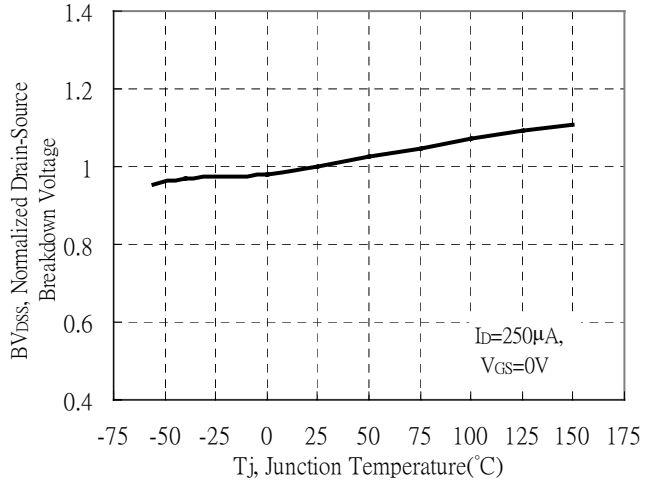
unit : mm

Typical Characteristics

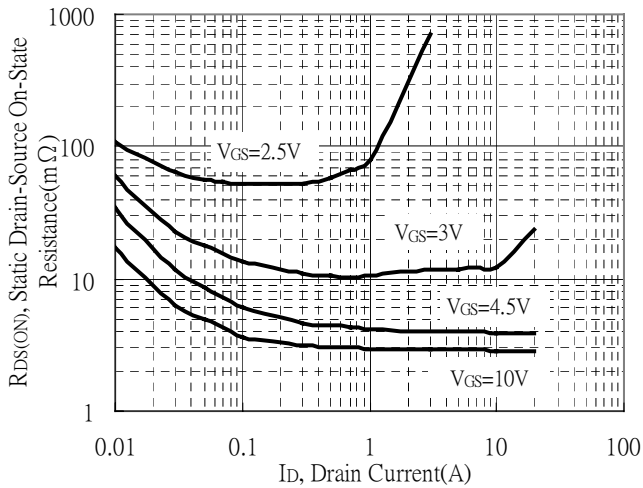
Typical Output Characteristics



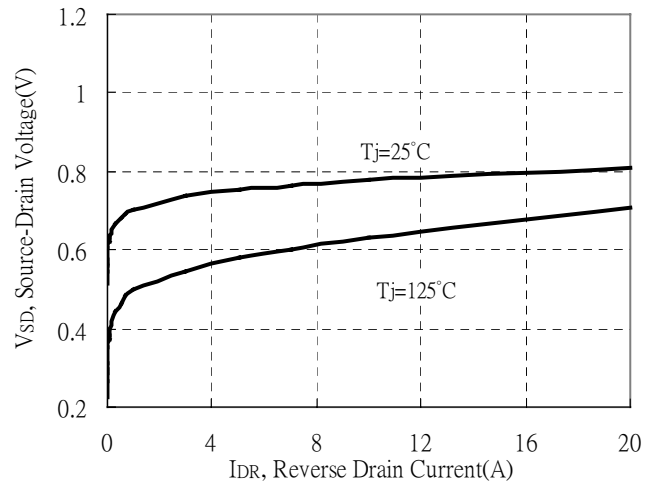
Brekdown Voltage vs Ambient Temperature



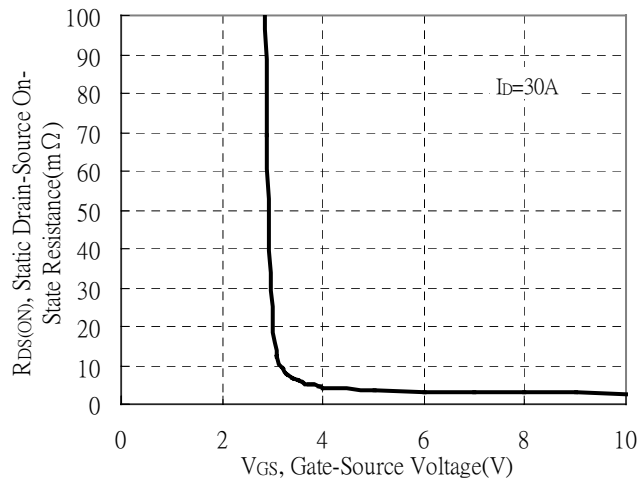
Static Drain-Source On-State resistance vs Drain Current



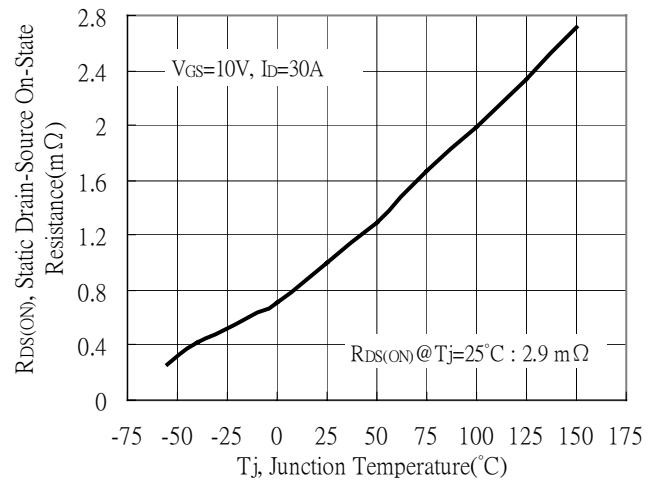
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



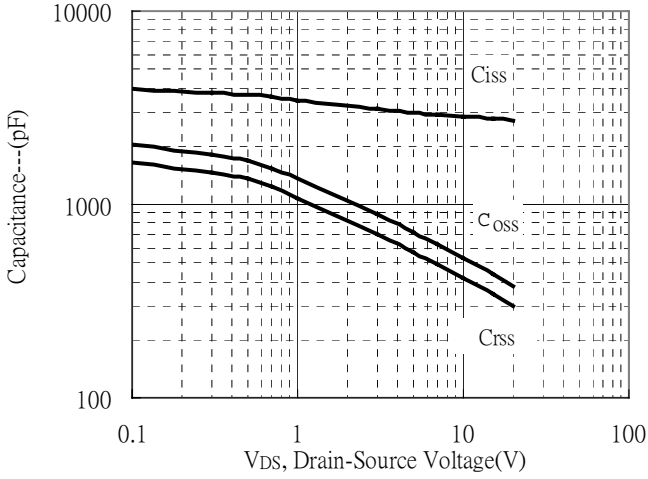
Drain-Source On-State Resistance vs Junction Temperature



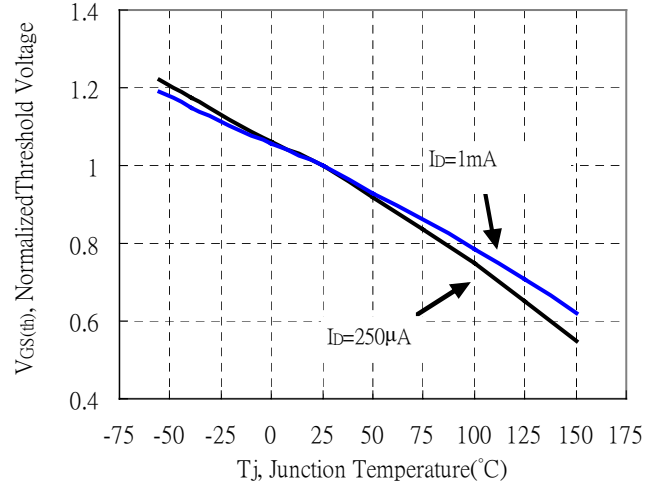


Typical Characteristics(Cont.)

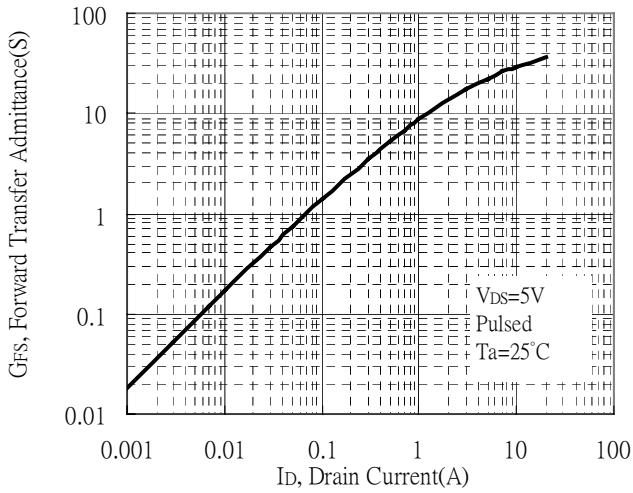
Capacitance vs Drain-to-Source Voltage



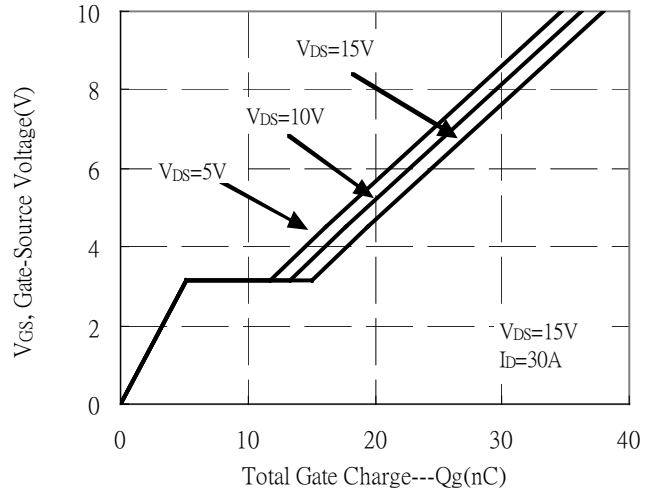
Threshold Voltage vs Junction Temperature



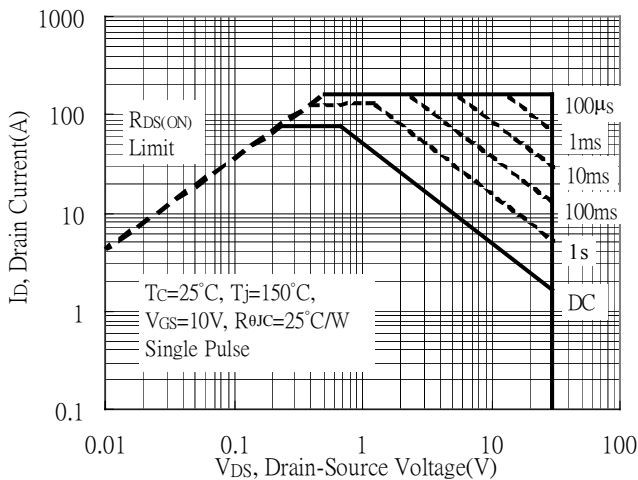
Forward Transfer Admittance vs Drain Current



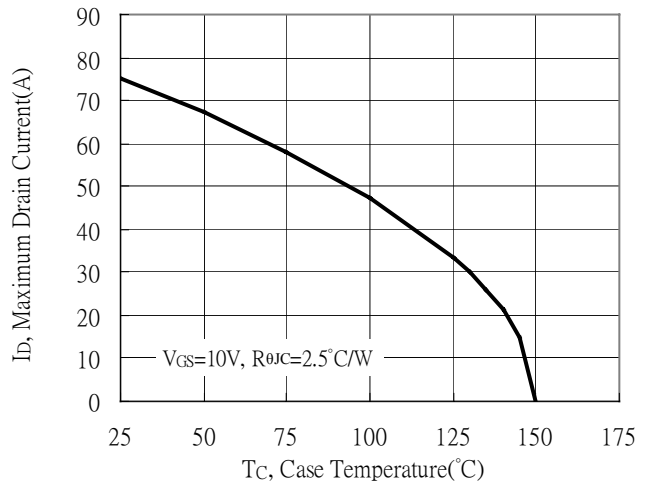
Gate Charge Characteristics



Maximum Safe Operating Area



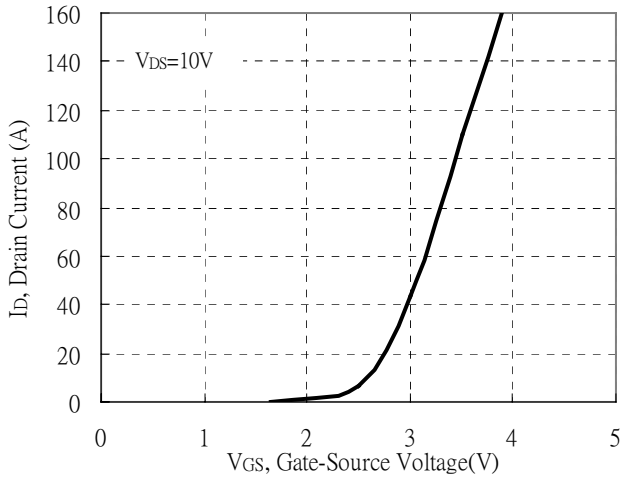
Maximum Drain Current vs Case Temperature



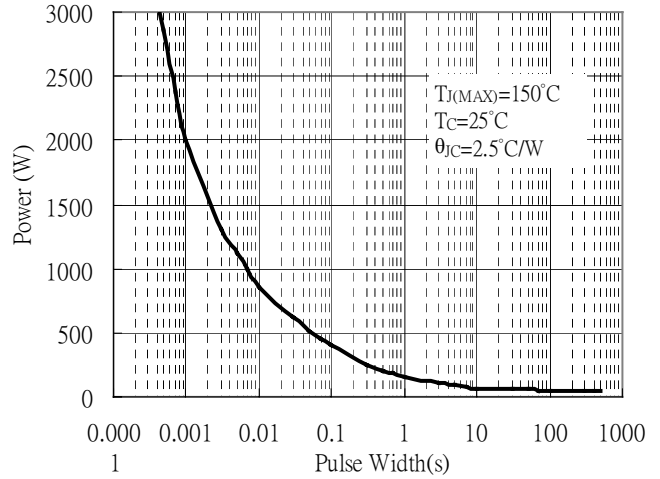


Typical Characteristics(Cont.)

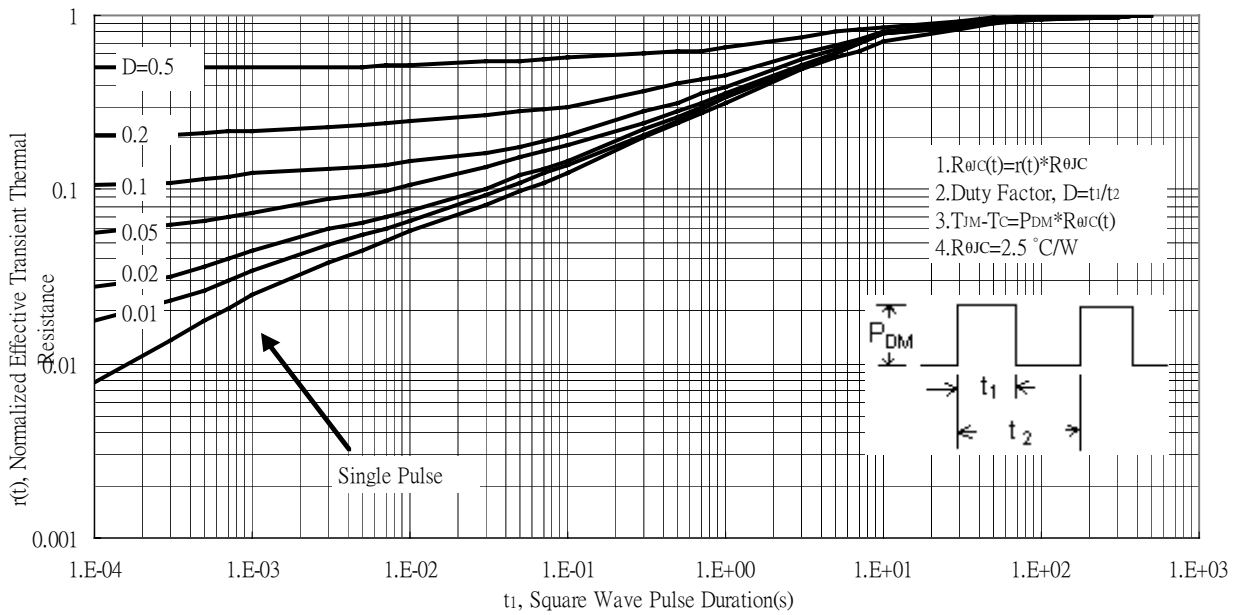
Typical Transfer Characteristics



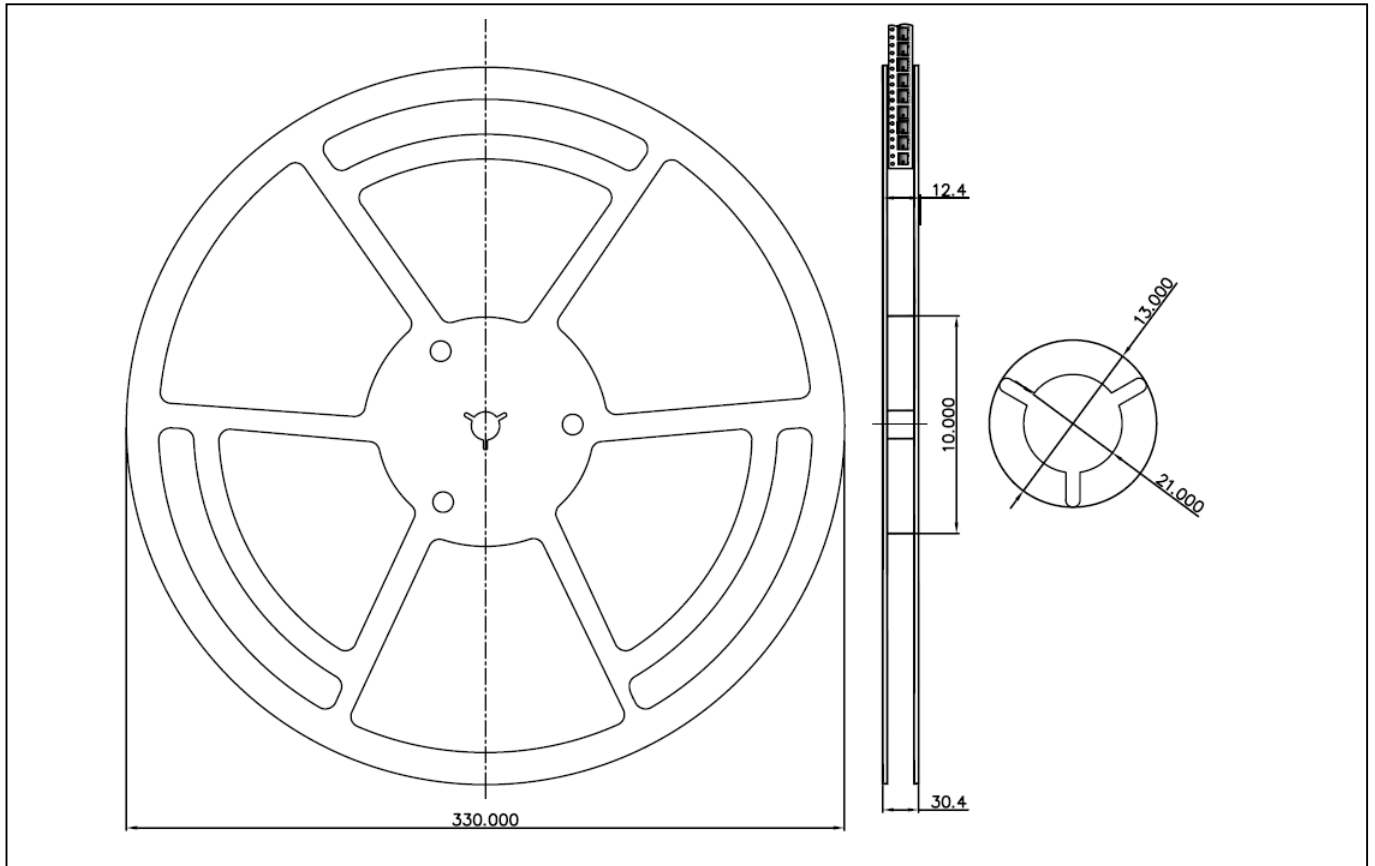
Single Pulse Maximum Power Dissipation



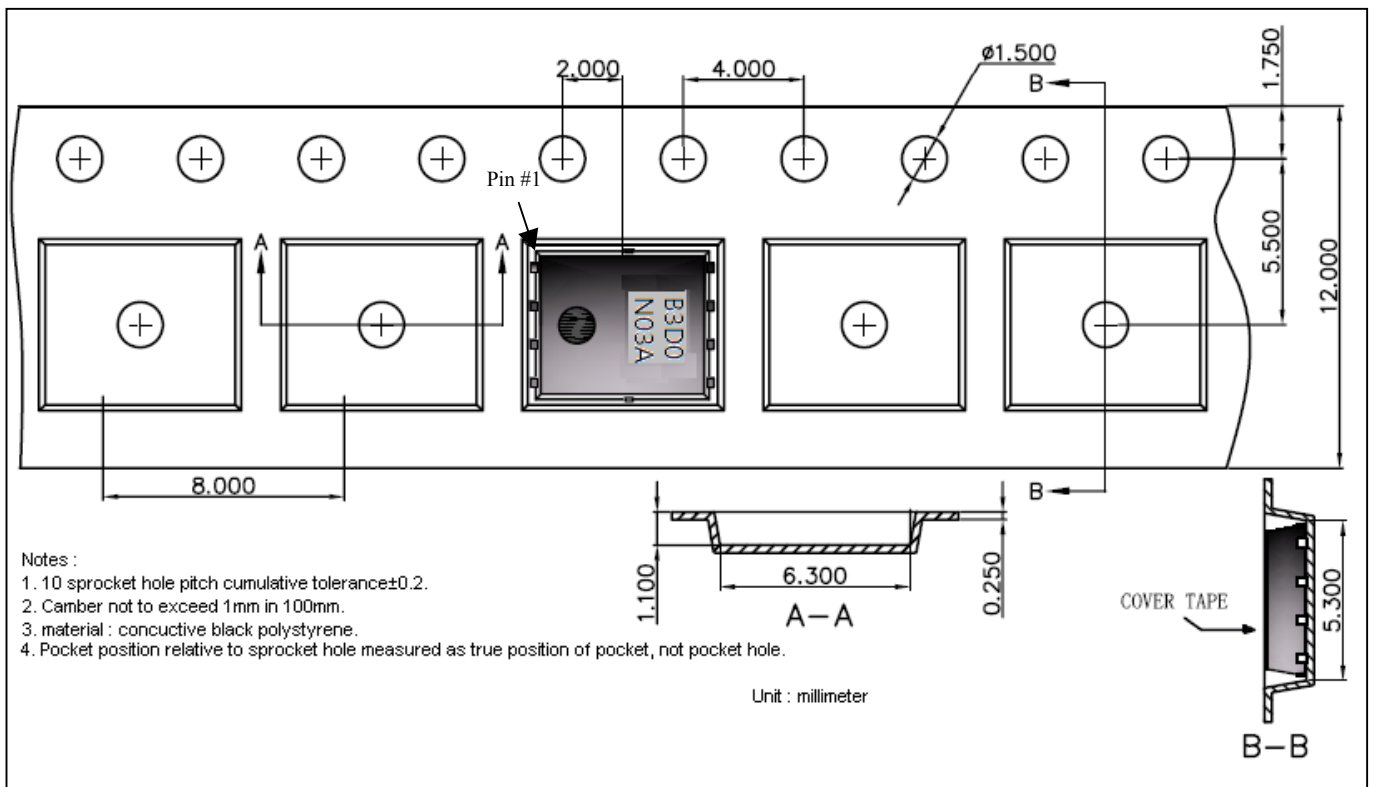
Transient Thermal Response Curves



Reel Dimension



Carrier Tape Dimension



Notes :

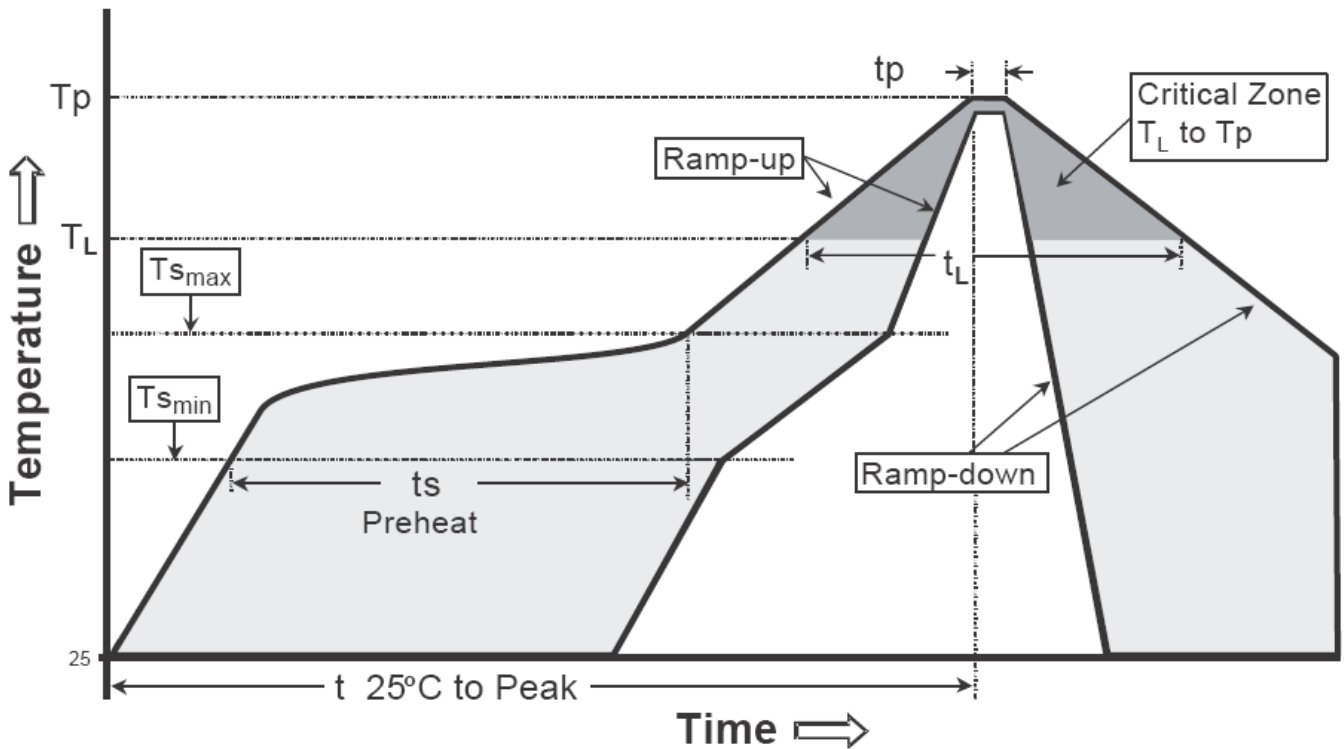
1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. material : conductive black polystyrene.
4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

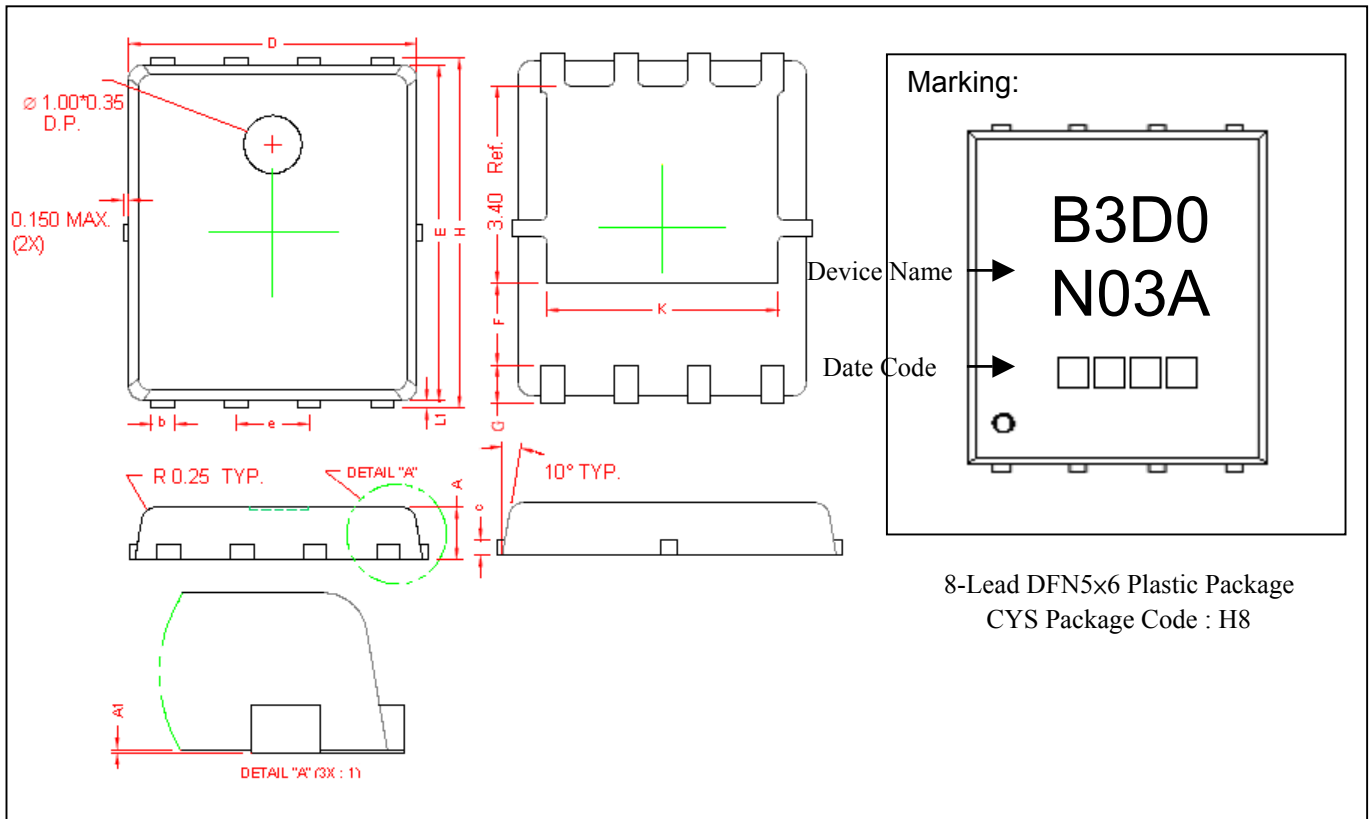
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

DFN5x6 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039	E	5.70	5.90	0.224	0.232
A1	0.00	0.05	0.000	0.002	e	1.27 BSC		0.050 BSC	
b	0.35	0.49	0.014	0.019	H	5.95	6.20	0.234	0.244
c	0.254 REF		0.010 REF		L1	0.10	0.18	0.004	0.007
D	4.90	5.10	0.193	0.201	G	0.60 REF		0.024 REF	
F	1.40 REF		0.055 REF		K	4.00 REF		0.157 REF	

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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