DuSLIC

Dual Channel Subscriber Line Interface Concept

PEB 3264/-2 Version 1.3
PEB 4264/-2 Version 1.1
PEB 3265 Version 1.3
PEB 4265/-2 Version 1.1
PEB 4266 Version 1.1

Wired Communications

Infineon
technologies

N e v e r   s t o p   t h i n k i n g .

DuSLIC

Dual Channel Subscriber Line

Interface Concept

PEB 3264/-2 Version 1.3
PEB 4264/-2 Version 1.1
PEB 3265 Version 1.3
PEB 4265/-2 Version 1.1
PEB 4266 Version 1.1

Wired Communications

Infineon technologies

N e v e r   s t o p   t h i n k i n g .

Revision History:	**2000-11-09**	**DS2**
Previous Version:	Product Overview DS1	

Page	Subjects (major changes since last revision)
all	PEB 3265 version changed from 1.2 to 1.3
all	New codecs SLICOFI-2S/-2S2 (PEB 3264/-2) and new SLIC´s SLIC-S/-S2 (PEB 4264/-2) and SLIC-E2 (PEB4265-2) added.
all	Major changes throughout the whole document

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

Table of Contents   **Page**

Table of Contents **Page**

List of Figures **Page**

List of Figures   **Page**

Preliminary

Preface

This document describes the DuSLIC chip set comprising a programmable dual channel *SLICOFI-2x* codec and two single channel high-voltage SLIC chips. For more DuSLIC related documents please see our webpage at http://www.infineon.com/duslic.

Synonyms

To simplify matters, the following synonyms are used:

SLICOFI-2x: Synonym used for all codec versions SLICOFI-2/-2S/-2S2

SLIC: Synonym used for all SLIC versions SLIC-S/-S2, SLIC-E/-E2 and SLIC-P

Organization of this Document

This Product Overview is divided into six chapters. It is organized as follows:

- Chapter 1, Overview
  A general description of the product, list of its key features and some typical applications.

- Chapter 2, Functional Description
  The main functions are presented following a functional block diagram.

- Chapter 3, Operational Description
  A brief description of the three operating modes: power down, active and ringing (plus signal monitoring techniques).

- Chapter 4, Interfaces
  Connection information including standard IOM$^{®}$-2 and PCM interface timing frames and pins.

- Chapter 5, Application Circuits
  Illustrations of balanced ringing, unbalanced ringing and protection circuits.

- Chapter 6, Index

1 Overview

DuSLIC is a chip set, comprising one dual channel *SLICOFI-2x* codec and two single-channel SLIC chips. It is a highly flexible codec/SLIC solution for an analog line circuit and is widely programmable. Users can now access different markets with a single hardware design that meets all different standards worldwide.

The interconnections between the single channel high-voltage SLIC (170 V process) and the dual channel *SLICOFI-2x* codec (advanced CMOS process) are a seamless fit. This guarantees maximum transmission performance with a minimum of necessary components.

DuSLIC family chip sets:

Table 1   DuSLIC Chip Sets

Chip Set	DuSLIC-S	DuSLIC-S2	DuSLIC-E	DuSLIC-E2	DuSLIC-P
Marketing Name	SLICOFI-2S/ SLIC-S	SLICOFI-2S2/ SLIC-S2	SLICOFI-2/ SLIC-E	SLICOFI-2/ SLIC-E2	SLICOFI-2/ SLIC-P
Product ID	PEB 3264/ PEB 4264	PEB 3264-2/ PEB 4264-2[1]	PEB 3265/ PEB 4265	PEB 3265/ PEB 4265-2[2]	PEB 3265/ PEB 4266
Longitudinal Balance	53 dB	60 dB	53 dB	60 dB	53 dB
Maximum DC feeding	32 mA	50 mA	32 mA	50 mA	32 mA
Neg. Battery Voltages	2	2	2	2	2/3
Add. positive Voltages	1	1	1	1	0
Internal Ringing	45 Vrms balanced	no	85 Vrms balanced	85 Vrms balanced	85 Vrms bal., 50 Vrms unbal.
ITDF[3]	no	no	yes	yes	yes
TTX	1.2 Vrms	no	2.5 Vrms	2.5 Vrms	2.5 Vrms
Add-Ons[4]	no	no	yes	yes	yes

[1] Nevertheless marked on the chip as PEB 4264

[2] Nevertheless marked on the chip as PEB 4265

[3] Integrated Test and Diagnosis Functions (board or line testing)

[4] The add-on functions are DTMF detection, Caller ID generation, Message Waiting lamp support, Three-party Conferencing, Universal Tone Detection (UTD), Line Echo Cancellation (LEC) and Sleep Mode.

The DuSLIC family comprises five different chip sets (see **Table 1**):

– Three basic DuSLIC chip sets optimized for different applications:
  DuSLIC-S (Standard),
  DuSLIC-E (Enhanced),
  DuSLIC-P (Power Management).

– Two different performance versions of the basic DuSLIC-E and DuSLIC-S chip sets (mainly regarding longitudinal balance and maximum DC feeding):
DuSLIC-E2 (using SLIC-E2 PEB 4265-2 compared to DuSLIC-E)
DuSLIC-S2 (using SLIC-S2 PEB 4264-2 and codec PEB 3264-2)

The codec devices SLICOFI-2, SLICOFI-2S and SLICOFI-2S2 are manufactured in an advanced 0.35 µm 3.3 V CMOS process.

The SLIC-E, SLIC-E2 and SLIC-P devices are manufactured in Infineon Technologies robust and well proven 170 V Smart Power technology.

The SLIC-S and SLIC-S2 devices are manufactured in Infineon Technologies 90 V Smart Power technology.

All line circuit functions are implemented on the DuSLIC chip set:

- BORSCHT functions
- Internal balanced/unbalanced ringing capability up to 85 Vrms
- Metering by Polarity Reversal and by 12/16 kHz sinusoidal bursts
- Dual-Tone Multifrequency (DTMF) detection and generation
- Caller ID generation
- Three-party Conferencing
- Universal Tone Detection (UTD) unit for fax-/modemtone detection
- Line Echo Cancellation unit (LEC)

Integrated battery switches guarantee minimum power consumption during the off-hook, on-hook and ringing modes. Test and diagnosis functions have been integrated to simplify testing (ITDF). No external test equipment is needed for either subscriber line testing in the field or board testing during production or in the field.

Usage of Codecs and SLICs:

DuSLIC-E, DuSLIC-E2 and DuSLIC-P comprise the same SLICOFI-2 codec with full EDSP (Enhanced Digital Signal Processor) features like DTMF detection, Caller ID generation, Universal Tone Detection (UTD) and Line Echo Cancellation.

DuSLIC-S comprises the SLICOFI-2S codec without EDSP features.

DuSLIC-S2 comprises the SLICOFI-2S2 codec based on the SLICOFI-2S but without Teletax metering (TTX) and internal ringing capability.

The respective SLIC variant for each chip set featured in **Table 1** has been selected according to performance and application requirements:

SLIC-S/-S2 (PEB 4264 / PEB 4264-2) and SLIC-E/-E2 (PEB 4265 / PEB 4265-2) are optimized for access network requirements, while the power management SLIC-P (PEB 4266) is an enhanced version for extremely power-sensitive applications or for applications where internal unbalanced ringing is required.

DuSLIC Architecture

Unlike traditional designs, DuSLIC splits the SLIC function into high-voltage SLIC functions and low-voltage SLIC functions.

The low-voltage functions are handled in the *SLICOFI-2x* device. The partitioning of the functions is shown in **Figure 1**.

HV SLIC Functions

Voltage feeding
Transversal current
  sensing
Longitudinal current
  sensing
Overload protection
Battery switching
Ring amplification
On-hook transmission
Polarity reversal

LV SLIC Functions

Programmable DC feeding
Ring generation
Supervision
Teletax generation
Teletax notch filter
Ring trip detection
Ground key detection
Hook switch detection

Codec Filter Functions

Filtering
PCM compression/expansion
Programmable gain
Programmable frequency
Impedance matching
Hybrid balance
DTMF generation
DTMF detection
FSK generation (Caller ID)
Linear mode support
  (16-bit uncompressed voice data)
IOM-2 and PCM/µC interface
Integrated Test and Diagnosis Functions (IDTF)
Line Echo Cancelling (LEC)
Universal Tone Detection (UTD)
Three-party conferencing
Message waiting lamp support

ezm14034.wmf

Figure 1   DuSLIC Chip Set

Dual Channel Subscriber Line Interface Concept DuSLIC

<div align="right">

PEB 3264/-2
PEB 3265
PEB 4264/-2
PEB 4265/-2
PEB 4266

</div>

Version 1.3

1.1   Features

- Internal balanced/unbalanced ringing capability up to 85 Vrms
- Programmable Teletax (TTX) generation
- Programmable battery feeding with capability for driving longer loops
- Fully programmable dual-channel codec
- Ground/loop start signaling
- Polarity reversal
- Integrated Test and Diagnosis Functions (IDTF)
- On-hook transmission
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID (FSK) generator
- Integrated fax/modem detection (Universal Tone Detection (UTD))
- Integrated Line Echo Cancellation unit (LEC)
- Optimized filter structure for modem transmission
- Three-party conferencing (in PCM/μC mode)
- Message waiting lamp support (PBX)
- Power optimized architecture
- Power management capability (integrated battery switches)
- 8 and 16 kHz PCM Transmission
- IOM-2 or PCM/μC-interface selectable
- Specification in accordance with ITU-T Recommendation G.712, ITU-T Recommendation Q.552 for interface Z and applicable LSSGR
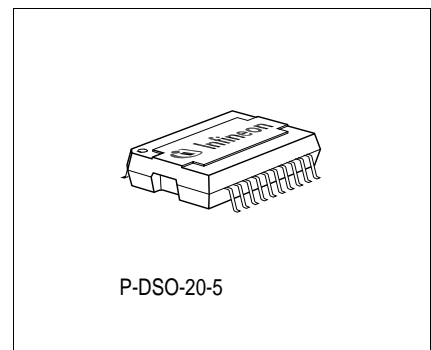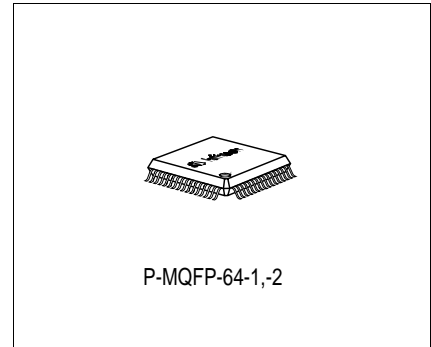
P-MQFP-64-1,-2

P-DSO-20-5

Type	Package
PEB 3264/-2	P-MQFP-64-1
PEB 4264/-2	P-DSO-20-5
PEB 3265	P-MQFP-64-1
PEB 4265/-2	P-DSO-20-5
PEB 4266	P-DSO-20-5

1.2 Typical Applications

The Infineon Technologies DuSLIC family is particularily designed for all access network applications and customer premises equipment but adresses all major telephone applications including:

- Digital Loop Carrier (DLC)
- Wireless Local Loop
- Fiber in the Loop
- Private Branch Exchange
- Intelligent NT (Network Termination) for ISDN
- ISDN Terminal Adapter
- Central Office
- Cable Modem
- XDSL NT
- Router
- Integrated Access Device (IAD)
- Voice over Packet Network Application
- PCM-x systems

1.3 Logic Symbols
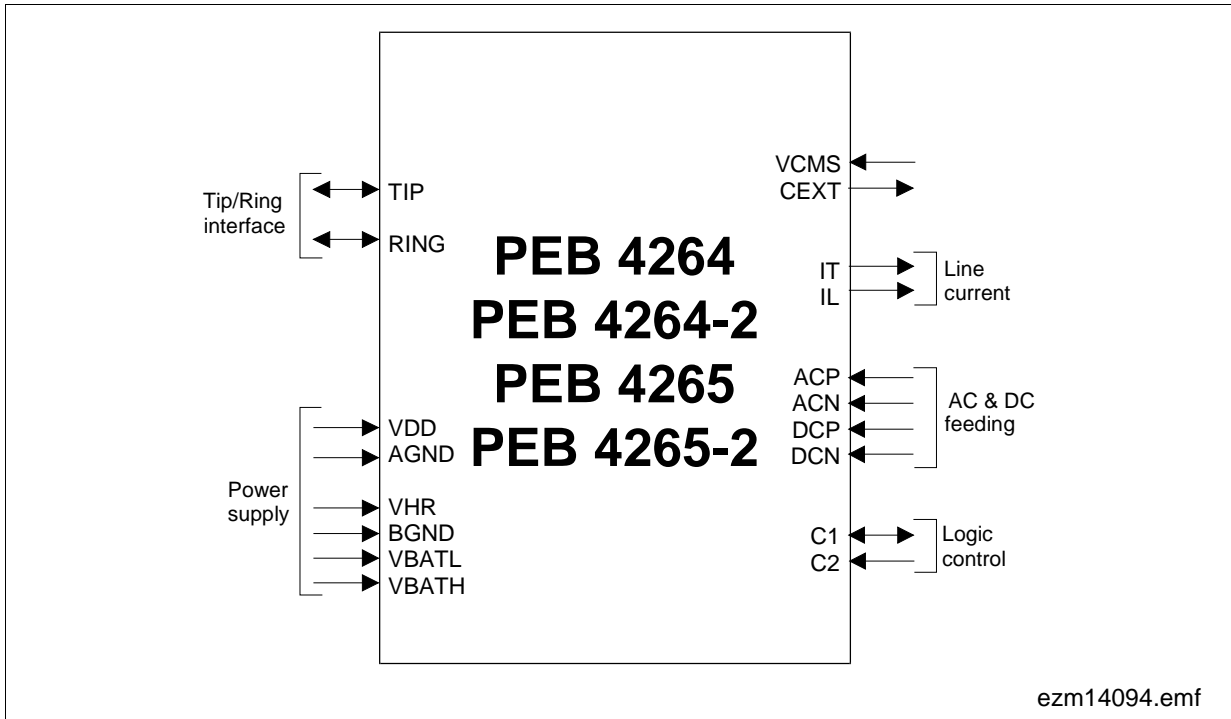
Figure 2   Logic Symbol SLIC-S / SLIC-S2 / SLIC-E / SLIC-E2
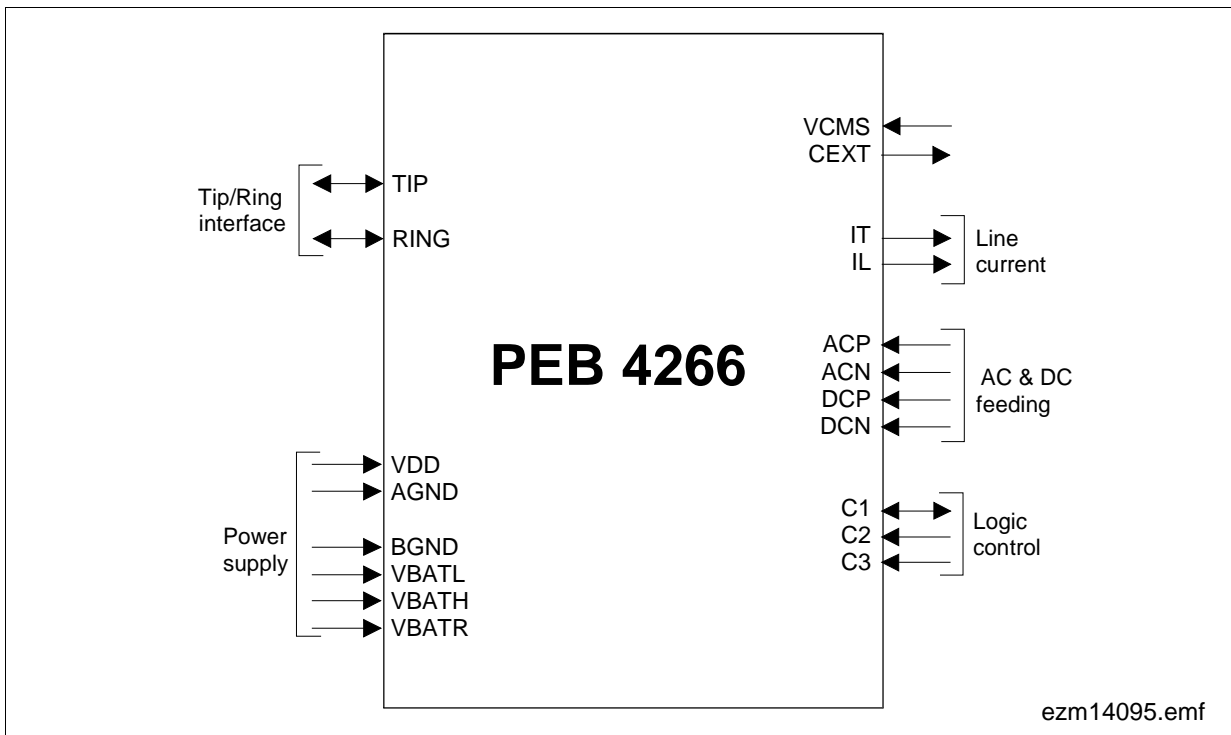
Figure 3   Logic Symbol SLIC-P
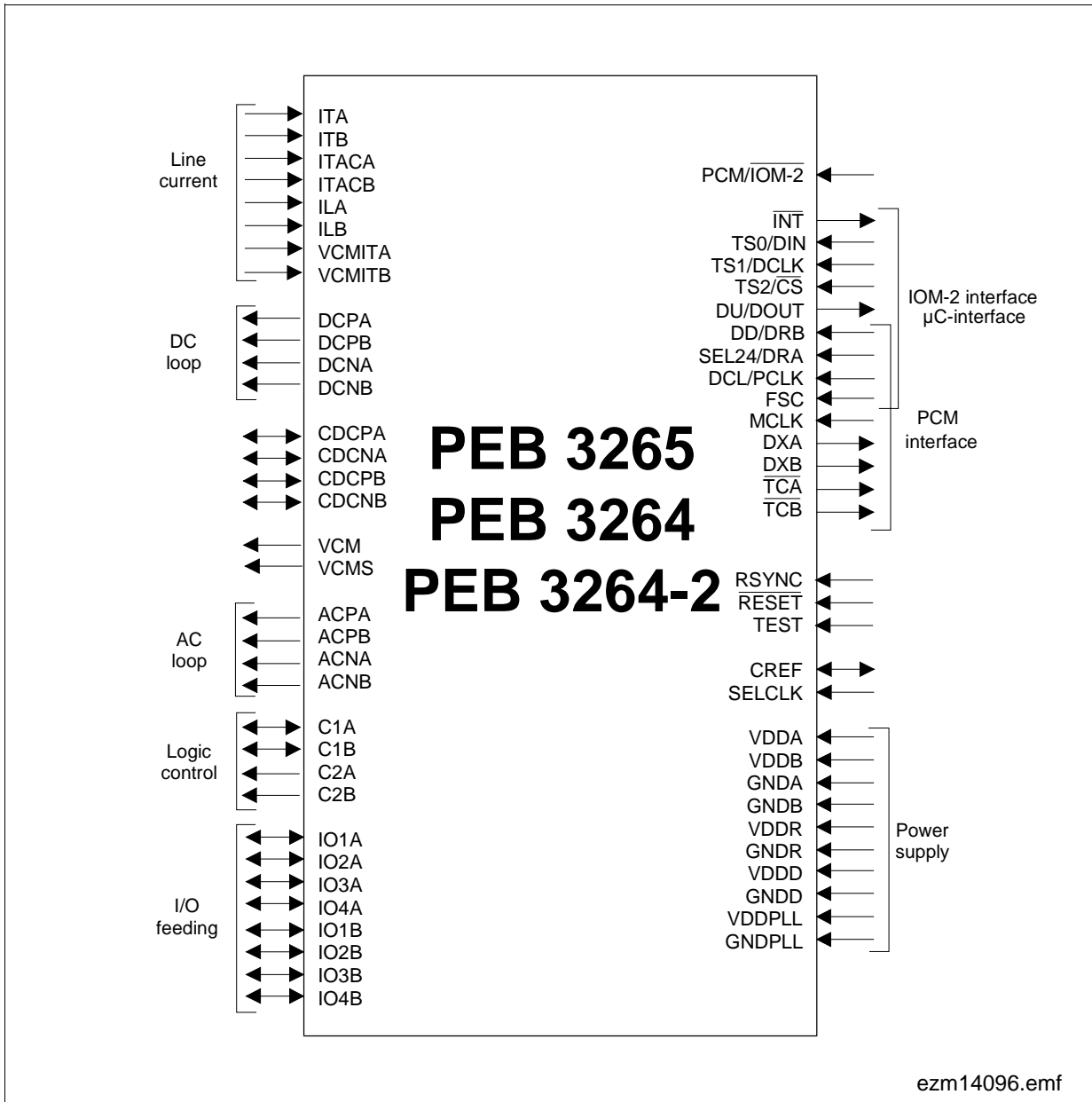
Figure 4   Logic Symbol SLICOFI-2/-2S/-2S2

2 Functional Description

2.1 Functional Overview

2.1.1 Basic Functions available for all DuSLIC Chip Sets

The DuSLIC chip set is a cost-effective, high-performance solution that provides the BORSCHT functions of an analog line circuit. DuSLIC has the advantage of offering all the functions integrated in a single channel high-voltage SLIC and in a dual channel DSP-based codec.

The functions described in this chapter are integrated in all DuSLIC chip sets (see **Figure 5** for DuSLIC-S/-S2 and **Figure 6** for DuSLIC-E/-E2/-P).

BORSCHT Functions

All BORSCHT functions are integrated:

- Battery feed
- Overvoltage protection
  (realized by the robust high-voltage SLIC technology and additional circuitry)
- Ringing[1]
- Signaling (supervision)
- Coding
- Hybrid for 2/4-wire conversion
- Testing

The following paragraphs explain the advantages of using DuSLIC to implement the BORSCHT functions.

- Battery Feed

An analog line circuit provides the voltage and current for subscriber equipment. In conventional line circuits, extra hardware is needed to adapt the battery feed characteristics to the requirements for different applications and countries. With the DuSLIC chip set, the battery feed (DC) characteristics can be programmed in the *SLICOFI-2x* (low-voltage SLIC function, see **Figure 1**) and applied to the line via the SLIC.

- Overvoltage Protection

Overvoltage protection is indispensable to prevent damage to the line circuit if the system is exposed to high voltages that can result from power lines crossing or lightning strikes.

---

[1] For DuSLIC-S2 chip set only external ringing is supported

The robust 170 V SLIC technology together with the external low cost protection circuit, consisting of varistors, resistors and thyristor diodes, form a reliable overvoltage protection solution. If an overvoltage occurs, the protection circuit separates the DuSLIC from the Tip and Ring lines.

• Ringing

The ringing signal is a low-frequency, high-voltage signal to the subscriber equipment. In conventional line circuits, the ringing voltage (e.g. 40 V_{RMS} to 85 V_{RMS}) is generated in an external ringing generator and applied to the Tip and Ring lines by a relay. With the DuSLIC chip set, the ringing generator is integrated and this relay is not needed. This saves space and costs in the line circuit design. The ringing signal is generated in the low-voltage *SLICOFI-2x* and amplified in the high-voltage SLIC. DuSLIC supports balanced and unbalanced ringing. With balanced ringing, the ringing voltage is applied differentially to the Tip and Ring lines. With unbalanced ringing, the ringing voltage is applied single-ended to either the Tip or Ring line against a potential which is near ground (for details see **"Ringing Modes" on Page 69**). Balanced ringing is generated by SLIC-E/-E2 and SLIC-S, while SLIC-P can generate both balanced and unbalanced ringing.

• Signaling (Supervision)

DuSLIC must detect when a subscriber changes from on-hook mode to off-hook mode in both non-ringing (hook switch detection) and ringing modes (ring trip detection). With this chip set, the thresholds for ring trip detection can be programmed in *SLICOFI-2x* to suit applications without using external components.

• Coding

SLICOFI-2x encodes an analog input signal to a digital PCM signal and decodes a PCM signal to an analog signal. Both A-law and μ-law coding is supported and can be selected via software.

• Hybrid for 2/4-wire Conversion

The subscriber equipment is connected to a 2-wire interface (Tip and Ring) where information is transmitted bidirectionally. For digital transmission through the switching network, the information must be split into separate transmit and receive paths (4 wires). To avoid generating echoes, the hybrid function requires a balanced network matched to the line impedance. Hybrid balancing can be programmed in the DuSLIC device without using any external components.

• Testing

Access to the analog loop is necessary to perform the regular measurements involved in monitoring the local loop. Line circuit functions must also be tested. In conventional line circuit solutions, test units have to be switched to perform loop and line circuit tests. A remote testing unit and relays are normally necessary to perform a full range of tests. DuSLIC already offers a number of internal test features to check both the local loop and the line circuit.

Programmability

An important feature of the DuSLIC design is the fact that all the SLIC and codec functions are programmable via the dual-channel codec device. Conventional designs need a number of external components to adapt the circuit for use in different countries and applications. In contrast, the configuration software DuSLICOS can be used to program the following functions of the DuSLIC chip set:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude[1]
- Hook thresholds
- TTX modes[1]

One of the main challenges of linecard development is to adapt the above-mentioned functions to country-specific requirements. These adaptations used to be handled by hardware, an approach that required a different linecard board for every modification to a specification.

Because signal processing within the *SLICOFI-2x* is completely digital, it is possible to adapt to the requirements listed above by simply updating the coefficients that control DSP processing of all data. This means, for example, that changing impedance matching or hybrid balance requires no hardware modifications. A single hardware is now capable of meeting the requirements for different markets. The digital nature of the filters and gain stages also assures high reliability, no drifts (over temperature or time) and minimal variations between different lines.

The characteristics for the two voice channels within *SLICOFI-2x* can be programmed independently of each other. The DuSLICOS software is provided to automate calculation of coefficients to match different requirements. DuSLICOS also verifies the calculated coefficients.

---

[1] Not available with DuSLIC-S2 chip set

2.1.2   Additional Functions available for DuSLIC-E/-E2/-P Chip Sets

The following line circuit functions are integrated only in the DuSLIC-E/-E2/-P chip sets (see **Figure 6**):

• Teletax metering

In many countries, Teletax metering signals (TTX signals) are sent to the subscriber for billing purposes. A 12/16 kHz sinusoidal metering burst has to be transmitted. As soon as metering pulses are applied to the subscriber line, they also divert to the transmit signal path which means that a notch filter has to block the 12/16 kHz signal to prevent overloading the transmit A/D converter. In contrast to conventional line circuits, the DuSLIC chip set generates the metering signal internally. The fact that the notch filter is integrated is one of the big advantages of DuSLIC.

• DTMF

A DTMF signal is used for touchtone signaling from a subscriber to the central office. Each digit is represented by a pair of tones. DuSLIC has an integrated DTMF decoder. The decoder is able to monitor the transmit and receive path for valid tone pairs and outputs the corresponding digital code for each DTMF tone pair. DuSLIC also has an integrated DTMF generator comprising two tone generators.

• Caller ID Frequency Shift Keying (FSK) Modulator

Caller ID is used to provide caller information to the subscriber during on-hook transmission. DuSLIC has an integrated FSK modulator capable of sending Caller ID information. The Caller ID modulator complies with all requirements of ITU-T recommendation V.23 and Bell 202.

• LEC (Line Echo Cancellation)

DuSLIC contains an adaptive line echo cancellation unit for the cancellation of near end echos (up to 8 ms cancelable echo delay time).

• UTD (Universal Tone Detection)

DuSLIC has an integrated Universal Tone Detection unit to detect special tones in the receive or transmit path (e.g. fax or modem tones). This is e.g. useful for activating the optimized filter coefficient set for modem transmission.
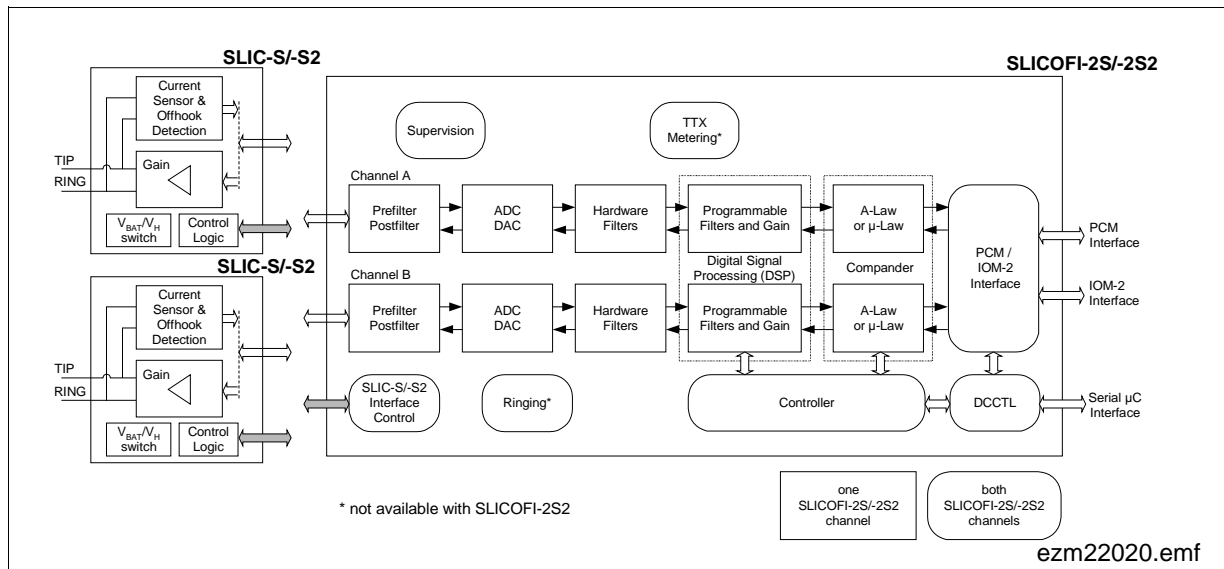
Figure 5   Line Circuit Functions included in the DuSLIC-S/-S2
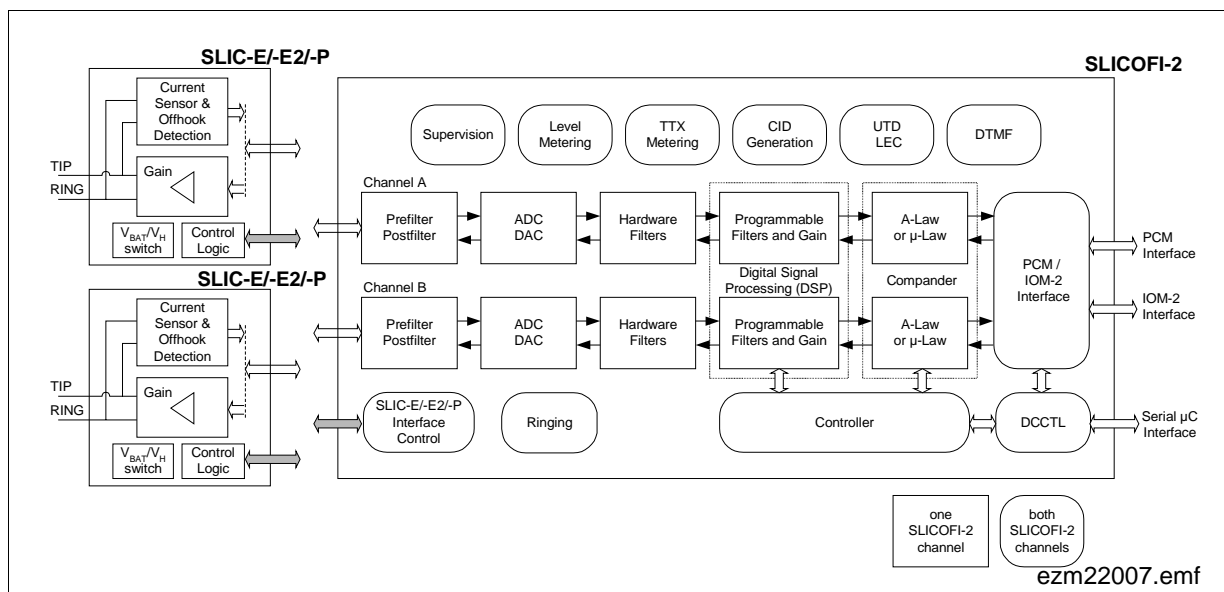
Figure 6   Line Circuit Functions included in the DuSLIC-E/-E2/-P

2.2 DC Feeding

Analog telephones need a DC current in the off-hook state. AC speech signals in the receive and transmit directions are superimposed on this DC current.

Once the off-hook state has been detected, the SLIC must supply a DC current to the subscriber line. The current is typically in the range of 14 to 40 mA (for DUSLIC programming capabilities see **Table 2**), depending on local country specifications. Conventional linecard solutions require additional hardware to adjust the DC feed current to meet different country specifications.

By contrast, DC feeding with the *SLICOFI-2x* is fully programmable by using the software coefficients depicted in**Table 2**. Special digital filter technology offers an extremely cost-effective solution that is far more flexible than analog DC feeding circuits. The DC feeding characteristic in SLICOFI-2 is programmed using software coefficients. **Figure 7** shows the signal paths for DC feeding between the SLICs and *SLICOFI-2x*:
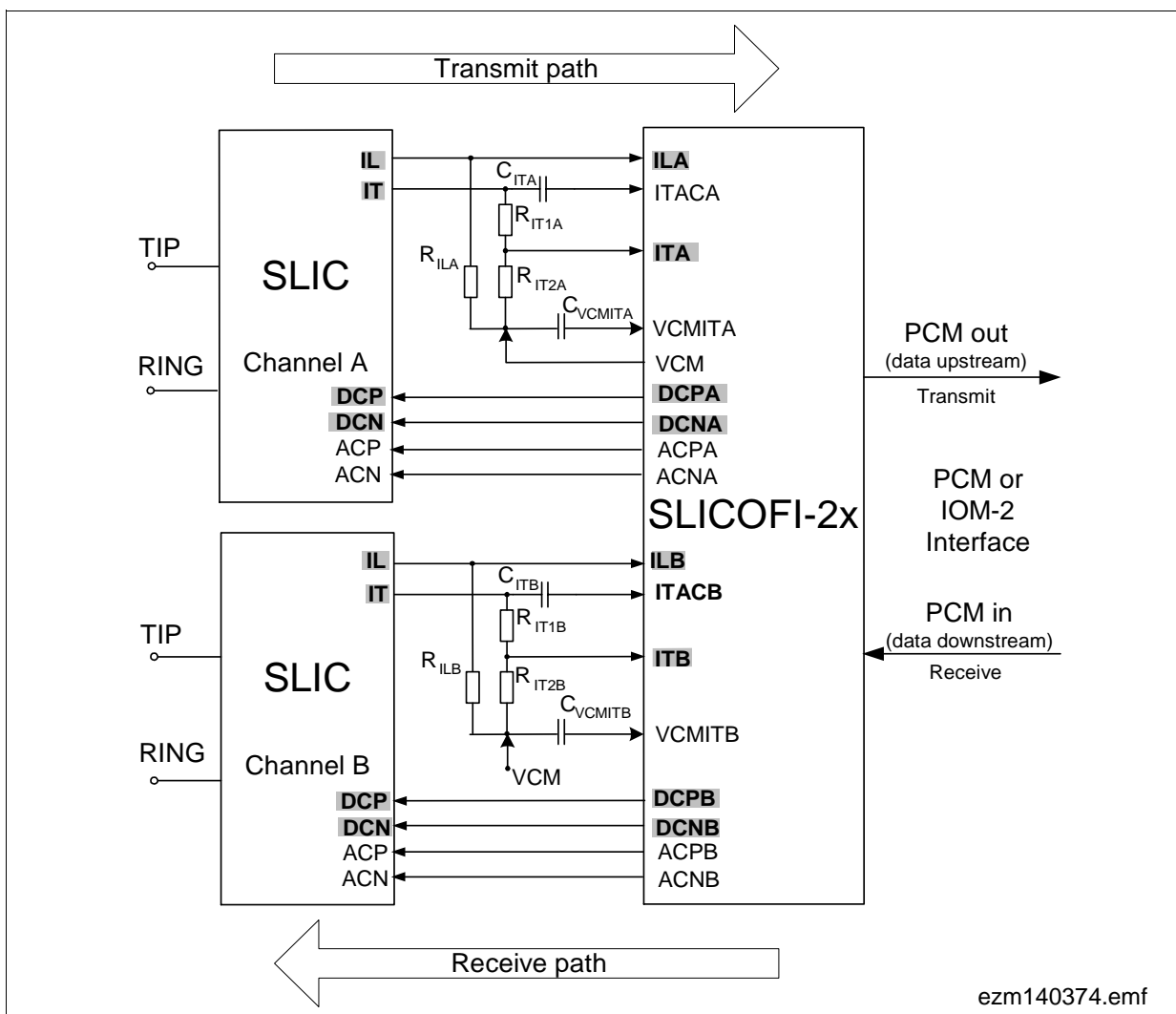
Figure 7   Signal Paths - DC Feeding

2.2.1   DC Characteristic Feeding Zones

The DuSLIC DC feeding characteristic has three different zones: the constant current zone, the resistive zone and the constant voltage zone. A voltage reserve V_{RES} (see **Chapter 2.2.7**) can be selected to avoid clipping the high level AC signals (e.g. TTX) and to take into account the voltage drop of the SLIC. The DC feeding characteristic is shown in **Figure 8**.
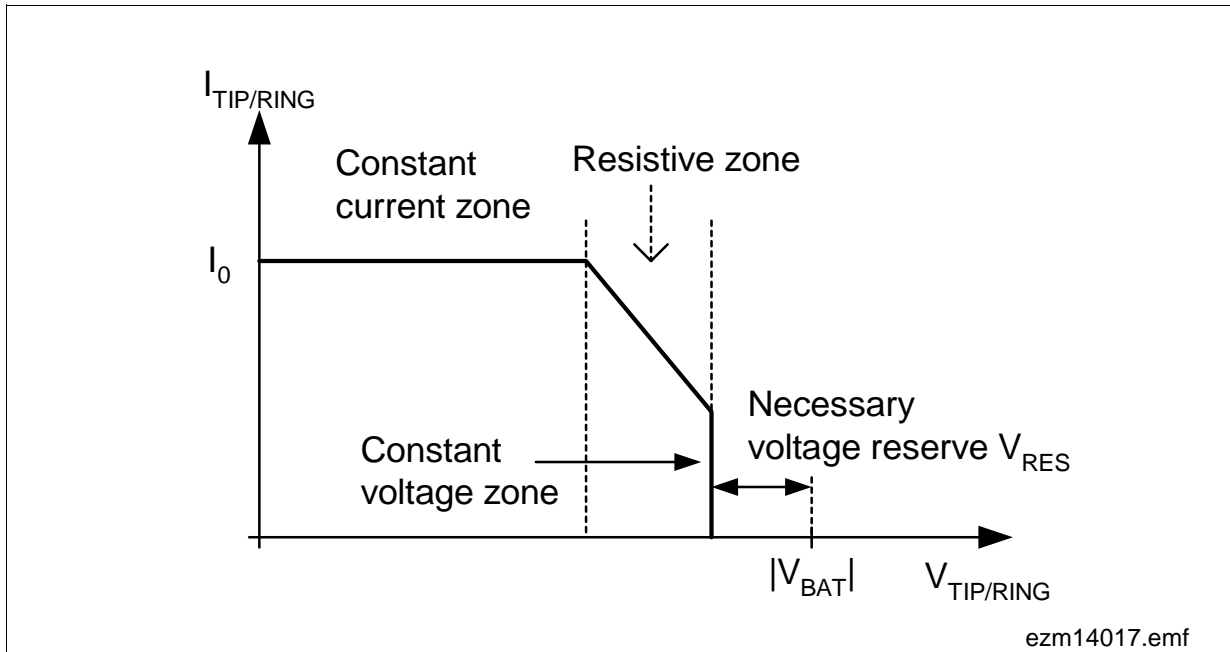
Figure 8   DC Feeding Characteristic

The simplified diagram shows the constant current zone as an ideal current source with an infinite internal resistance, while the constant voltage zone is shown as an ideal voltage source with an internal resistance of 0 Ω. For the specification of the internal resistances see **Chapter 2.2.5**

2.2.2 Constant Current Zone

In the off-hook state, the feed current must usually be kept at a constant value independent of load (see **Figure 9**). The SLIC senses the DC current and supplies this information to *SLICOFI-2x* via the IT pin (input pin for DC control). *SLICOFI-2x* compares the actual current with the programmed value and adjusts the SLIC drivers as necessary. $I_{\text{TIP/RING}}$ in the constant current zone is programmable from 0 to 32 mA or 0 to 50 mA depending on the used SLIC version.
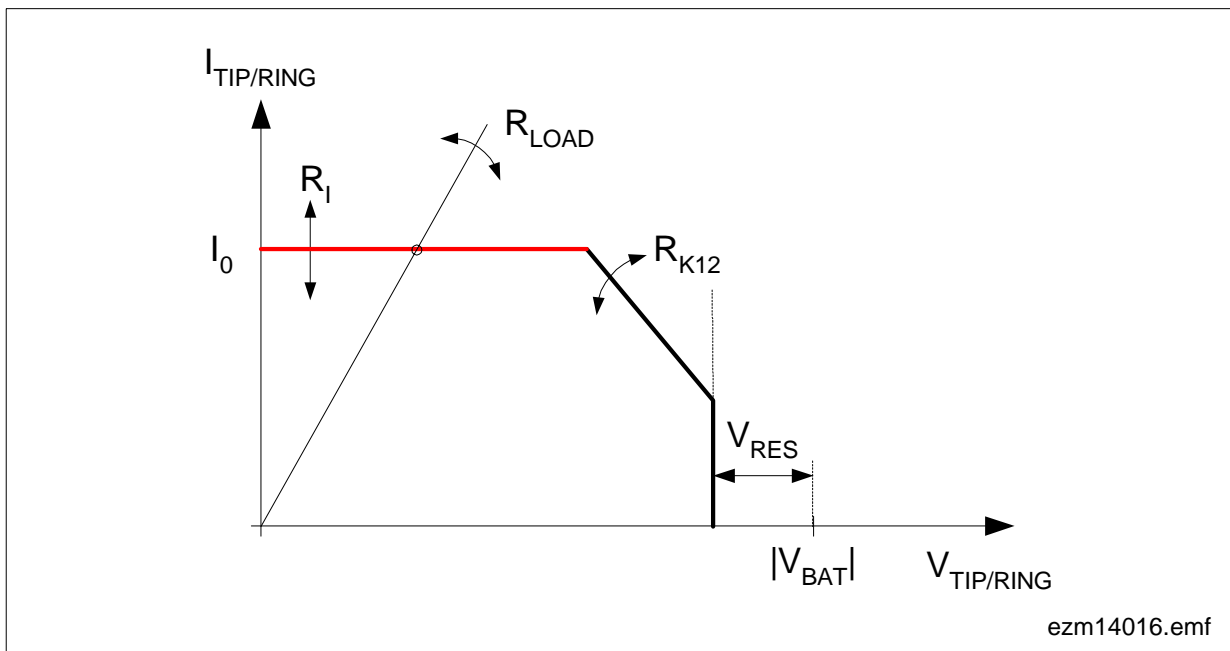
Figure 9   Constant Current Zone

Depending on the load, the operating point is determined by $V_{\text{TIP/RING}}$ between the Tip and Ring pins.

The operating point is calculated from:

$V_{\text{TIP/RING}} = R_{\text{LOAD}} \times I_{\text{TIP/RING}}$
where

$R_{\text{LOAD}} = R_{\text{PRE}} + R_{\text{LINE}} + R_{\text{PHONE,OFF-HOOK}}$
$R_{\text{PRE}} = R_{\text{PROT}} + R_{\text{STAB}}$ (see **Figure 52**, **Page 98**).

The lower the load resistance R_{LOAD}, the lower the voltage between the Tip and Ring pins. A typical value for the programmable feeding resistance in the constant current zone is about $R_{\text{I}} = 10$ kΩ (see **Table 2**).

2.2.3   Resistive Zone

The programmable resistive zone R_{K12} of DuSLIC provides extra flexibility over a wide range of applications. The resistive zone is used for very long lines where the battery is incapable of feeding a constant current into the line.

The operating point in this case crosses from the constant current zone for low and medium impedance loops to the resistive zone for high impedance loops (see **Figure 10**). The resistance of the zone R_{K12} is programmable from R_V to 1000 Ω.
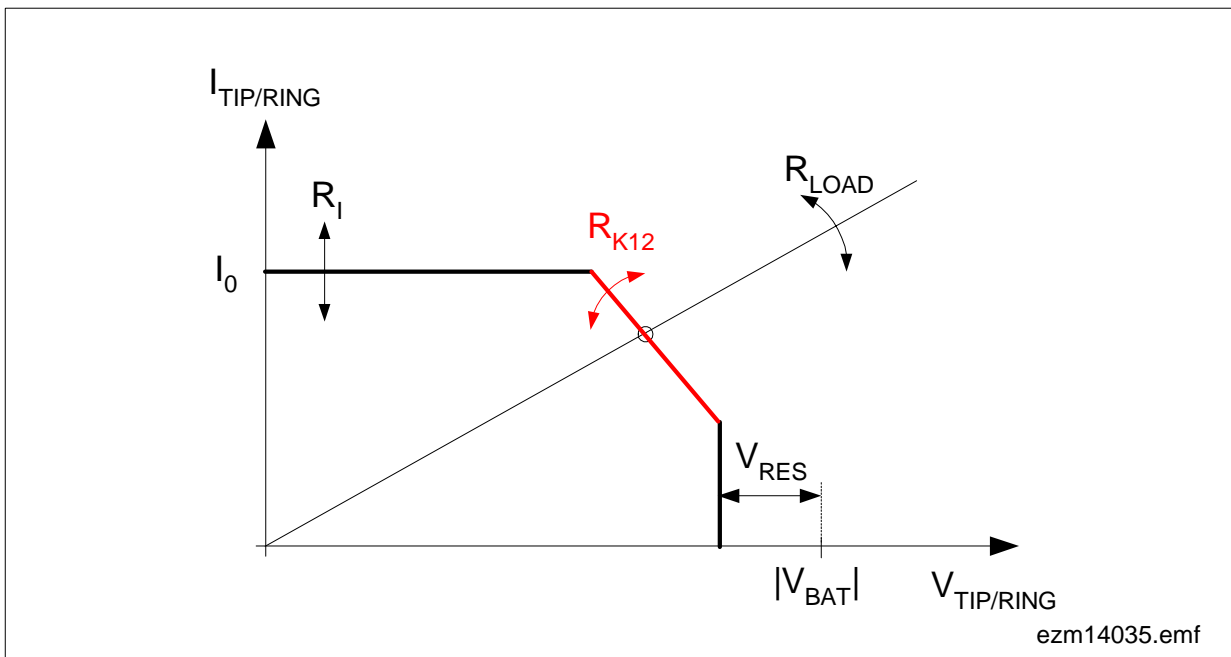
Figure 10   Resistive Zone

2.2.4 Constant Voltage Zone

The constant voltage zone (see **Figure 11**) is used in some applications to supply a constant voltage to the line. In this case $V_{TIP/RING} = V_{LIM}$ is constant and the current depends on the load between the Tip and Ring pin. V_{LIM} is set by the DuSLICOS software.

In the constant voltage zone the external resistors $R_{PRE} = R_{PROT} + R_{STAB}$ necessary for stability and protection define the resistance R_V seen at the RING and TIP wires of the application.
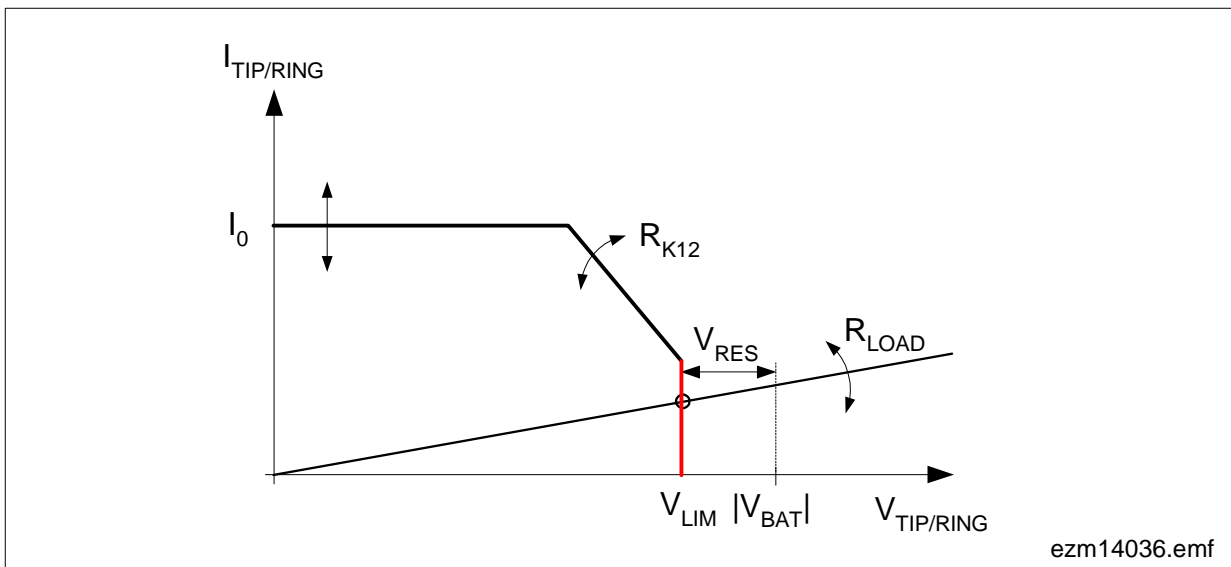
Figure 11   Constant Voltage Zone

2.2.5 Programmable Voltage and Current Range of DC Characteristic

In the above chapters the idealized DC characteristics were shown. A detailed description is given in **Figure 12**.
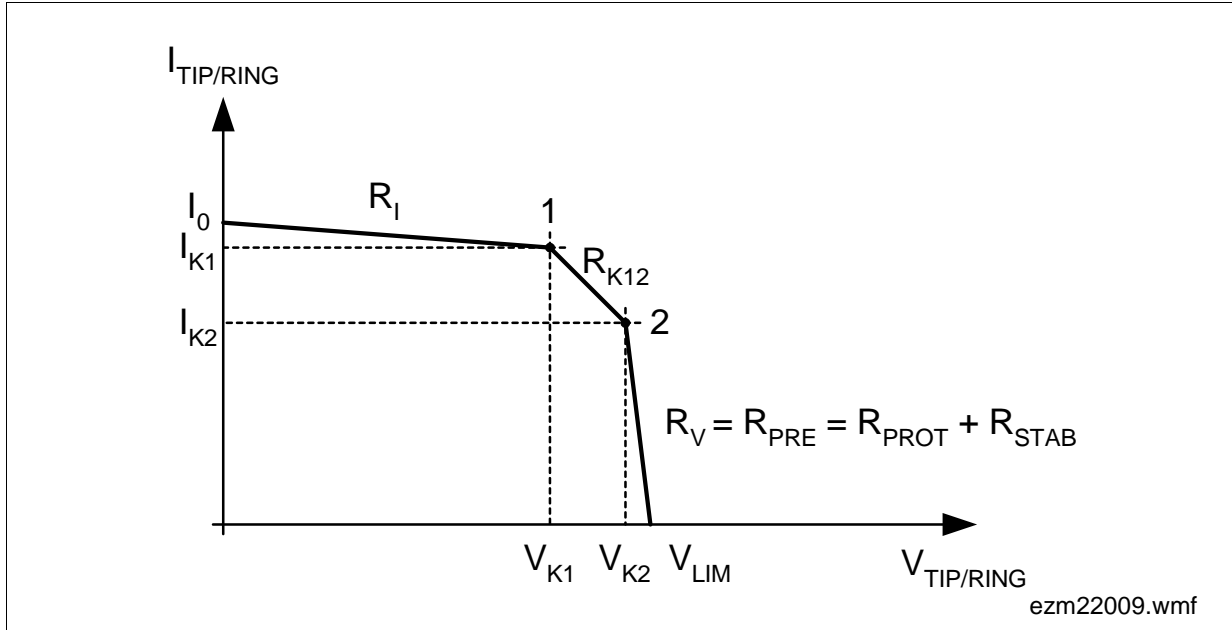
Figure 12   DC Characteristic (Detailed Description)

The programmable range of the parameters R_I, I_0, I_{K1}, V_{K1}, R_{K12} and V_{LIM} is given in **Table 2**:

Table 2   DC Characteristic

Symbol	Programmable Range	Condition
R_I	1.8 kΩ … 40 kΩ	–
I_0	0 … 32 mA	only for DuSLIC-S, DuSLIC-E, DuSLIC-P
	0 … 50 mA	only for DuSLIC-S2, DuSLIC-E2
I_{K1}	0 … 32 mA	only for DuSLIC-S, DuSLIC-E, DuSLIC-P
	0 … 50 mA	only for DuSLIC-S2, DuSLIC-E2
V_{K1}	0 … 50 V	–
	$V_{K1} < V_{LIM} - I_{K1} \times R_{K12}$	only (V_{K1}, I_{K1})
	$V_{K1} < V_{LIM} - I_{K1} \times R_V$ $V_{K1} > V_{LIM} - I_{K1} \times R_{K12}$	(V_{K1}, I_{K1}) and (V_{K2}, I_{K2})
R_{K12}	R_V … 1000 Ω	–
V_{LIM}	0 … 50 V	–
	$V_{LIM} > V_{K1} + I_{K1} \times R_{K12}$	only (V_{K1}, I_{K1})

2.2.6 SLIC Power Dissipation

The power dissipation in the SLIC can be estimated by the power dissipation in the output stages (see **Chapter 3.5.3**). The power dissipation can be calculated from:

$$P_{SLIC} \approx (V_{BAT} - V_{TIP/RING}) \times I_{TIP/RING}$$

Figure 13   Power Dissipation

![Infineon technologies logo]
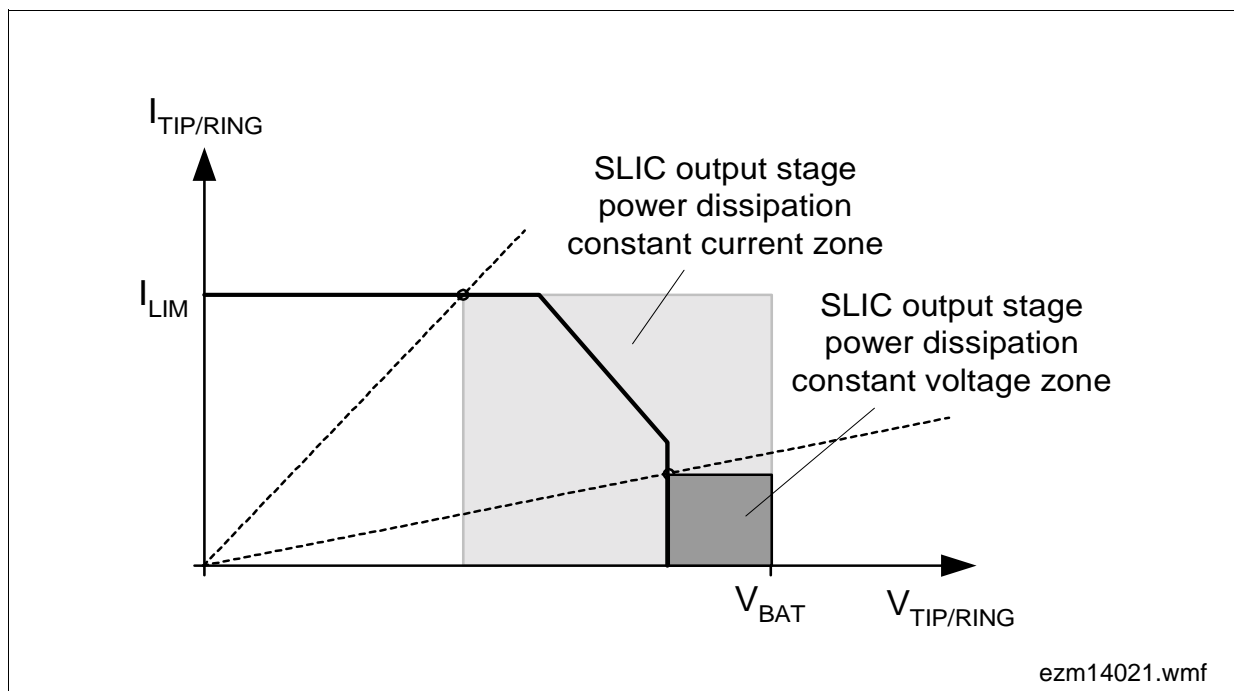
2.2.7 Necessary Voltage Reserve

To avoid clipping AC speech signals as well as AC metering pulses, a voltage reserve V_{RES} (see **Figure 8**) has to be provided.

$V_{RES} = |V_{BAT}| - V_{LIM}$ (see **Page 18**)

V_{BAT} is the selected battery voltage, which can be depending on the mode either V_{BATH}, V_{BATL}, $(V_{HR} - V_{BATH})$ for SLIC-S/-S2/-E/-E2 or V_{BATH}, V_{BATL}, $-V_{BATR}$ for SLIC-P.

V_{RES} consists of:

- Voltage reserve of the SLIC output buffers: this voltage drop depends on the output current through the Tip and Ring pins. For a standard output current of 25 mA, this voltage reserve is a few volts (see **Table 14**).
- Voltage reserve for AC speech signals: max. signal amplitude (example 2 V)
- Voltage reserve for AC metering pulses: The TTX signal amplitude V_{TTX} depends on local specifications and varies from 0.1 Vrms to several Vrms at a load of 200 Ω. To obtain V_{TTX} = 2 Vrms at a load of 200 Ω and R_{PRE} = 50 Ω ($R_{PRE} = R_{PROT} + R_{STAB}$, see **Figure 51**, **Page 97**), 3 Vrms = 4.24 Vpeak are needed at the SLIC output.

Therefore a V_{RES} value of 10.24 V must be selected (= 4 V (SLIC drop for peak current of DC and speech and TTX) + 2 V (AC speech signals) + 4.24 V (TTX-signal)).

ezm14032.wmf
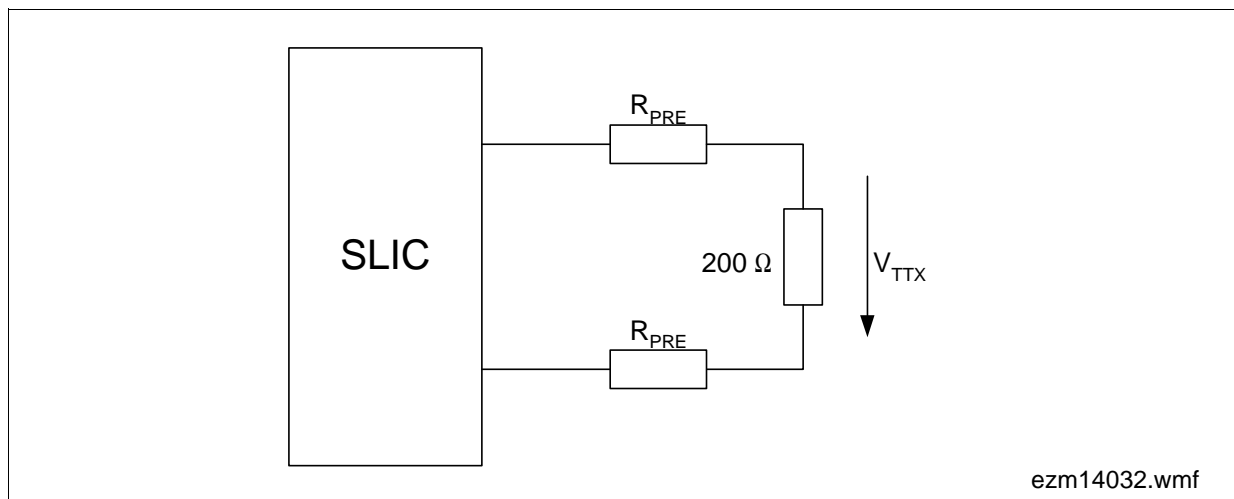
Figure 14   **TTX Voltage Reserve Schematic**

DuSLIC

2.2.8 Extended Battery Feeding

If the battery voltage is not sufficient to supply the minimum required current through the line even in the resistive zone, the auxiliary positive battery voltage can be used to expand the voltage swing between Tip and Ring. With this extended supply voltage V_{HR} (DuSLIC-S/-S2/E/-E2) respectively V_{BATR} (DuSLIC-P), it is possible to supply the constant current for long lines. **Figure 15** shows the DC feeding impedances $R_{MAX,ACTH}$ in ACTH mode and $R_{MAX,ACTR}$ in ACTR mode (for ACTH and ACTR modes see **Chapter 3.1**).
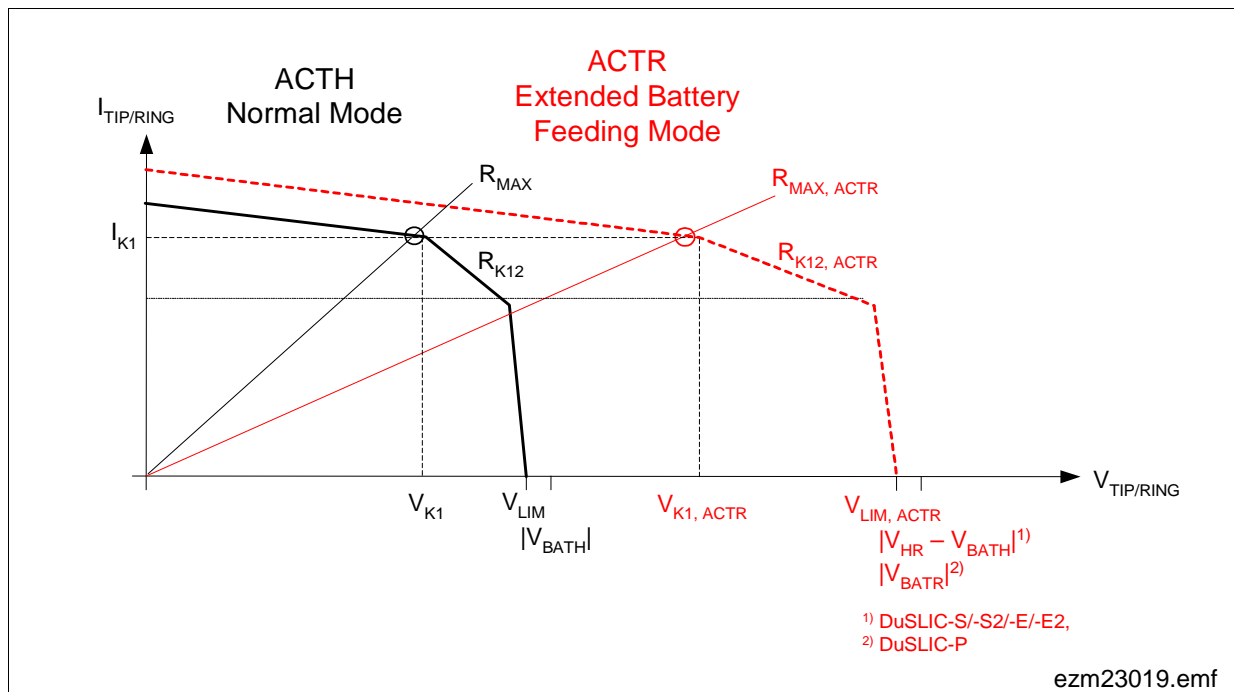
Figure 15   DC Feeding Characteristics (ACTH, ACTR)

2.3   AC Transmission Characteristics

SLICOFI-2x uses either an IOM-2 or a PCM digital interface. In receive direction, *SLICOFI-2x* converts PCM data from the network and outputs a differential analog signal (ACP and ACN) to the SLIC, that amplifies the signal and applies it to the subscriber line. In transmit direction, the transversal (IT) and longitudinal (IL) currents on the line are sensed by the SLIC and fed to the *SLICOFI-2x*. A capacitor separates the transversal line current into DC (IT) and AC (ITAC) components. As ITAC is the sensed transversal (also called metallic) current on the line, it includes both the receive and transmit components. *SLICOFI-2x* separates the receive and transmit components digitally, via a transhybrid circuit. **Figure 16** shows the signal paths for AC transmission between the SLICs and *SLICOFI-2x*:
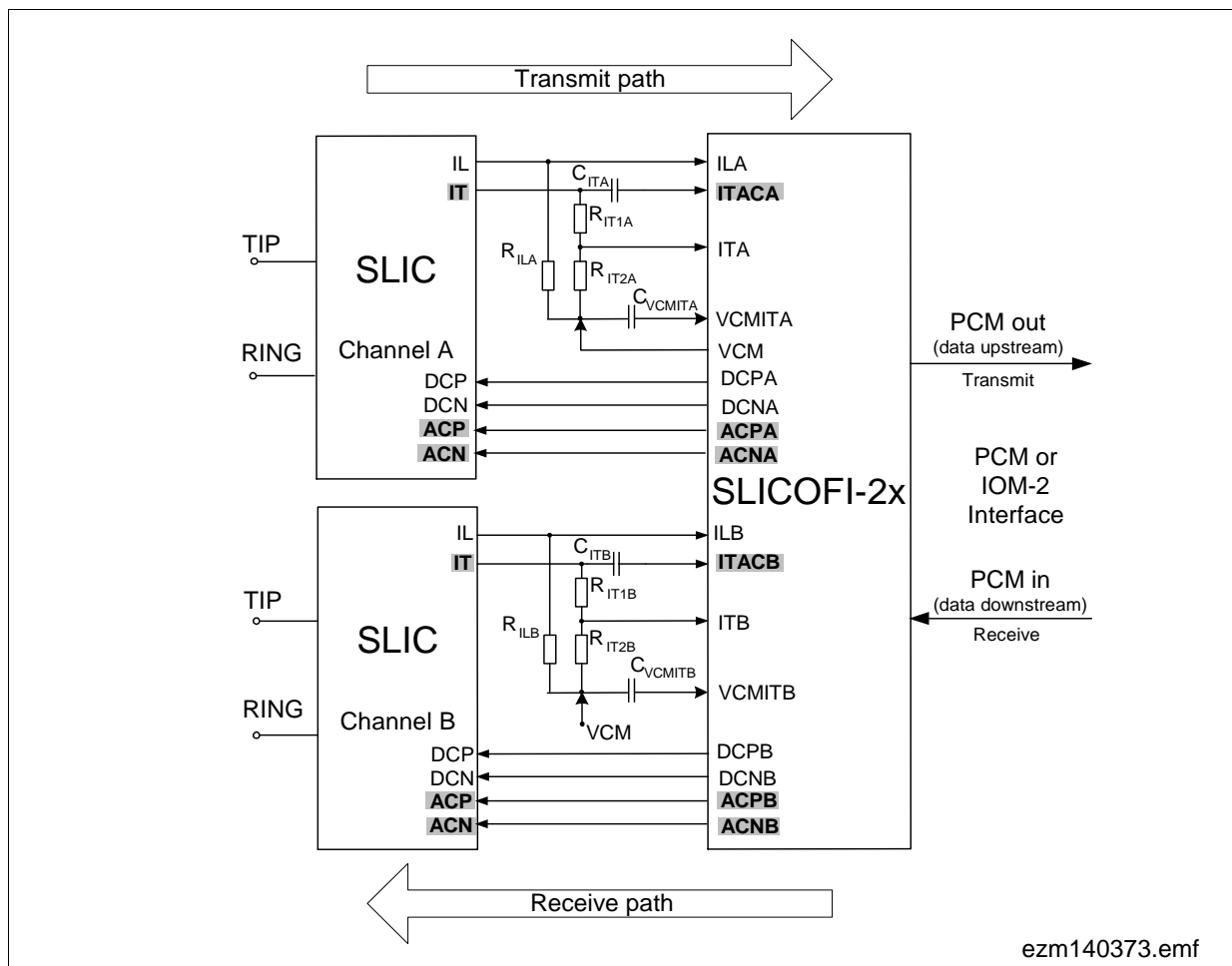
Figure 16   Signal Paths - AC Transmission

The signal flow within the *SLICOFI-2x* for one voice channel is shown in **Figure 17** by the following schematic circuitry. With the exception of a few analog filter functions, signal processing is performed digitally in the *SLICOFI-2x*.
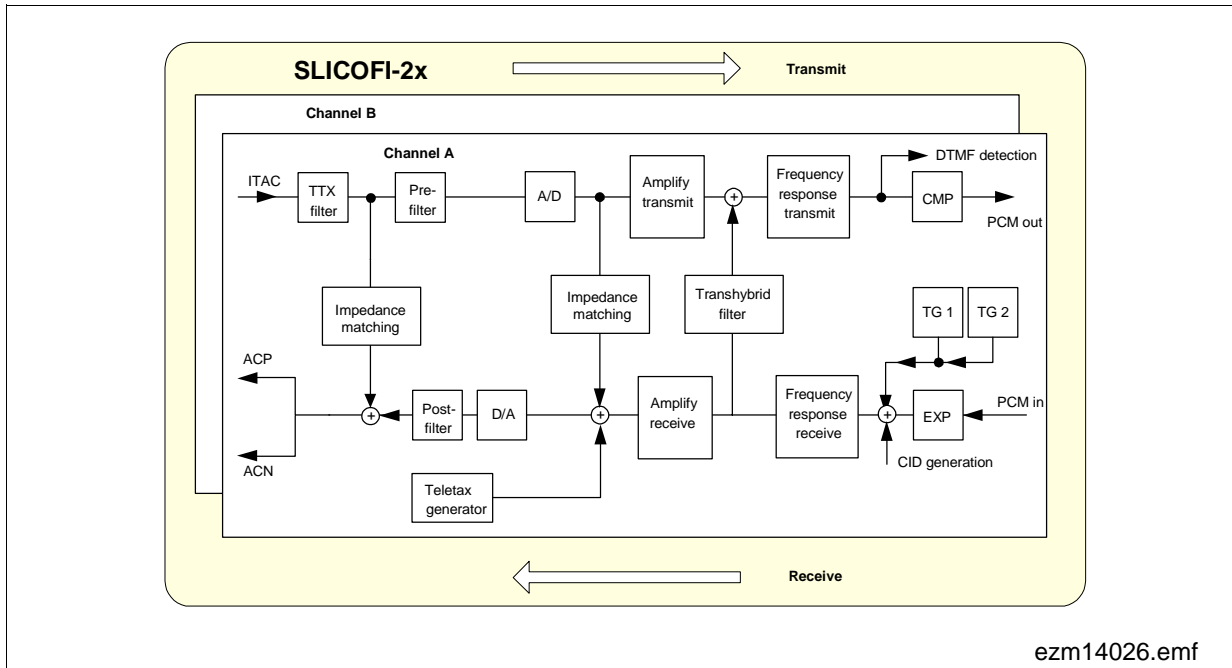
Figure 17   Signal Flow in Voice Channel (A)

2.3.1   Transmit Path

The current sense signal (ITAC) is converted to a voltage by an external resistor. This voltage is first filtered by an anti-aliasing filter (pre-filter), that stops producing noise in the voiceband from signals near the A/D sampling frequency. A/D conversion is done by a 1-bit sigma-delta converter. The digital signal is down-sampled further and routed through programmable gain and filter stages. The coefficients for the filter and gain stages can be programmed to meet specific requirements. The processed digital signal goes through a compander (CMP) that converts the voice data into A-law or μ-law codes. A time slot assignment unit outputs the voice data to the programmed time slot. *SLICOFI-2x* can also operate in 16-bit linear mode for processing uncompressed voice data. In this case, two time slots are used for one voice channel.

2.3.2   Receive Path

The digital input signal is received via the IOM-2 or PCM interface. Expansion (EXP), PCM low-pass filtering, frequency response correction and gain correction are performed by the DSP. The digital data stream is up-sampled and converted to a corresponding analog signal. After smoothing by post-filters in the *SLICOFI-2x*, the AC signal is fed to the SLIC, where it is superimposed on the DC signal. The DC signal has been processed in a separate DC path. A TTX signal, generated digitally within *SLICOFI-2x*, can also be added.

2.3.3   Impedance Matching

The SLIC outputs the voice signal to the line (receive direction) and also senses the voice signal coming from the subscriber. The AC impedance of the SLIC and the load impedance need to be matched in order to maximize power transfer and minimize two-wire return loss. The two-wire return loss is a measure of the impedance matching between a transmission line and the AC termination of DuSLIC.

The actual line impedance however can vary considerably, depending on loop length, loaded/unloaded lines, cable type, etc. Reference networks have therefore been defined to represent the average characteristics of a country's local loop. These reference networks differ from country to country and need to be reflected by the linecard being used in that country.

Impedance matching is done digitally within *SLICOFI-2x* by providing three impedance matching feedback loops. The loops feed the transmit signal back to the receive signal simulating the programmed impedance through the SLIC. When calculating the feedback filter coefficients, the external resistors between the protection circuit and SLIC ($R_{PRE} = R_{PROT} + R_{STAB}$, see **Figure 51**, **Page 97**) have to be taken into account. The impedance can be programmed to any appropriate real and complex values shown in the Nyquist diagram **Figure 18**. This means that the device can be adapted to requirements anywhere in the world without requiring the hardware changes that are necessary with conventional line card designs.
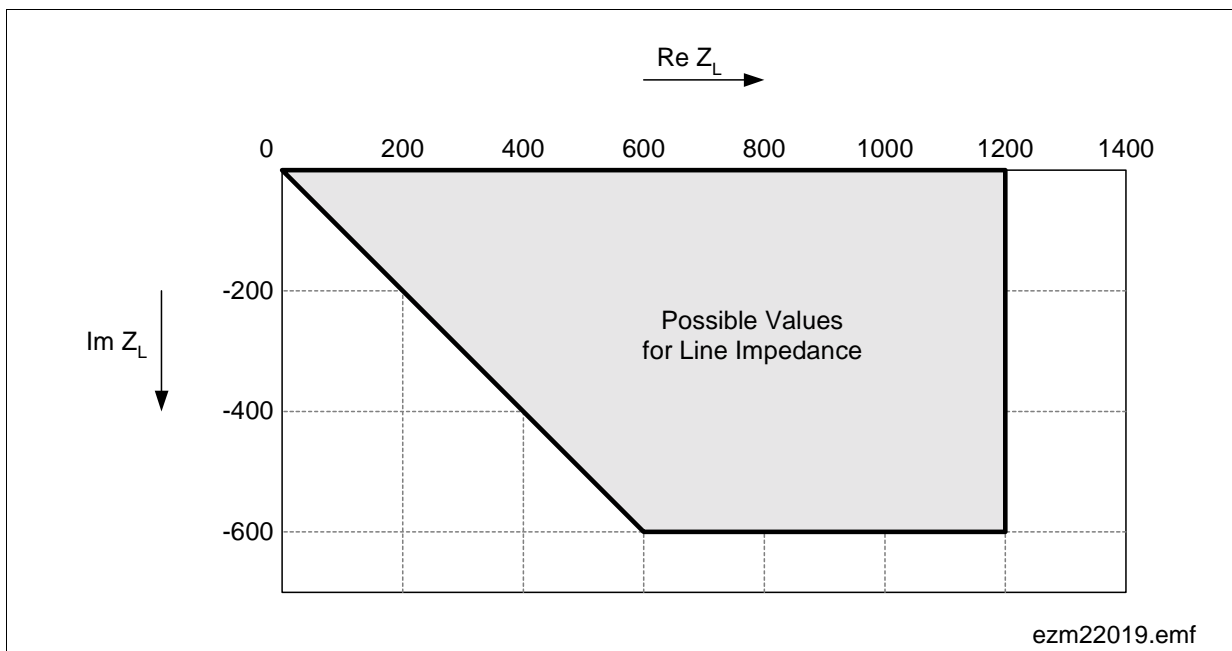
Figure 18   Nyquist Diagram

2.3.4 Transhybrid Balance

Digital switching systems can handle voice data only if receive and transmit data are separated on distinctive channels. The analog voice signal on the local loop is 2-wire full duplex, so it needs to be converted from 2-wire to 4-wire (2 wires each for receive and transmit). The circuitry, that performs this task, is commonly referred to as a hybrid circuit (see **Figure 19**)
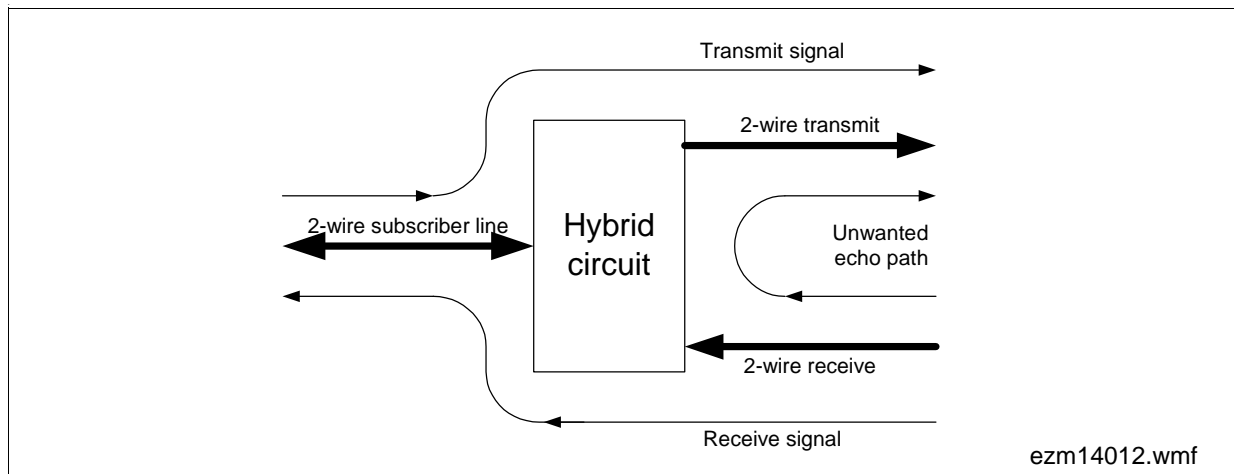
Figure 19   2/4-wire Conversion in the Hybrid Circuit

To prevent the receive voice signal being looped back (echoed) directly into the transmit voice path, the hybrid circuit has to separate the receive path signal from the transmit path signal.

In contrast with conventional line card designs, echo cancellation is implemented digitally within *SLICOFI-2x*. **Figure 19** shows the transhybrid loop that subtracts the receive signal from the transmit signal. The hybrid function is also dependent on loop condition. It has to be adapted to country-specific requirements. In conventional line card designs, this is done by external hardware adaptation. With *SLICOFI-2x*, adaptation is simply a matter of updating coefficients. No hardware changes are necessary.

2.4 Ringing

With the 170 V technology used for the SLIC, a ringing voltage of up to 85 Vrms can be generated on-chip without the need for an external ringing generator. The *SLICOFI-2x* generates a sinusoidal ringing signal that causes less noise and cross-talk in neighboring lines than a trapezoidal ringing signal. The ringing frequency is programmable from 3 to 300 Hz.

The advantage over traditional applications with a central ringing generator and decoupling resistors (approx. R = 400 Ω) is the very low source impedance of DuSLIC (approx. 60 Ω without R_{PROT}). Thus it is possible to supply the subscriber line with a lower ringing voltage from the SLIC. SLIC-E/-E2, SLIC-S/-S2 and SLIC-P support different ringing methods (see **Chapter 2.4.3**).

2.4.1 Ringer Load

A typical ringer load can be thought of as a resistor in series with a capacitor. Ringer loads are usually described as a REN (Ringer Equivalence Number) value. REN is used to describe the on-hook impedance of the terminal equipment, and is actually a dimensionless ratio that reflects a certain load. REN definitions vary from country to country. A commonly used REN is described in FCC part 68 that defines a single REN as either 5 kΩ, 7 kΩ or 8 kΩ of AC impedance at 20 Hz. The impedance of an n-multiple REN is equivalent to parallel connection of n single RENs. In this manual, all references to REN assume the 7 kΩ model.

For example, a 1 REN and 5 REN load would be:
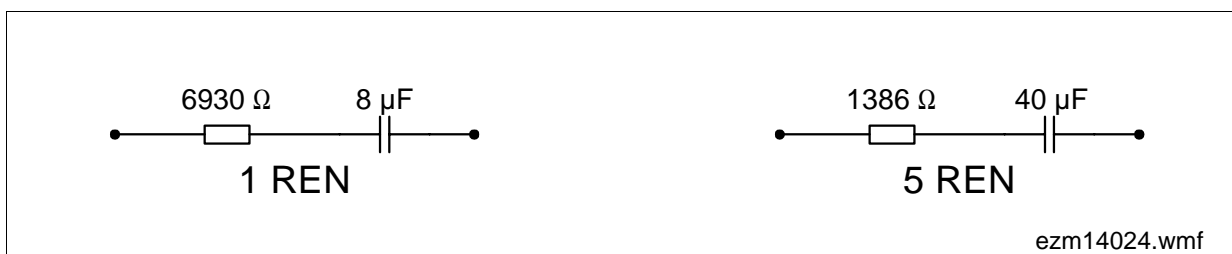
Figure 20   Typical Ringer Loads of 1 and 5 REN used in US

2.4.2 Ring Trip

Once the subscriber has gone off-hook, the ringing signal must be removed within a specified time, and power must start feeding to the subscriber's phone. There are two ring trip methods:

DC Ring Trip Detection

Most applications with DuSLIC are using DC ring trip detection. By applying a DC offset together with the ringing signal, a transversal DC loop current starts to flow when the subscriber goes off-hook. This DC current is sensed by the SLIC and in this way used as an off-hook criterion. The SLIC supplies this information to the *SLICOFI-2x* at the IT pin. The *SLICOFI-2x* continuously integrates the sensed line current I_{TRANS} over one ringer period. This causes the integration result to represent the DC component of the ring current. If the DC current exceeds the programmed ring trip threshold, *SLICOFI-2x* generates an interrupt. Ring trip is reliably detected and reported within two ring signal periods. The ringing signal is switched off automatically at zero crossing by the *SLICOFI-2x*. The threshold for the ring trip DC current is set internally in *SLICOFI-2x*, programmed via the digital interface. The DC offset for ring trip detection can be generated by the DuSLIC chip set and the internal ring trip function can be used, even if an external ringing generator is used.

AC ring trip detection:

For short lines (< 1 kΩ loop length) and for low-power applications, the DC offset can be avoided to reduce the battery voltage for a given ring amplitude. Ring trip detection is done by rectifying the ring current I_{TRANS}, integrating it over one ringer period and comparing it to a programmable AC ring trip threshold.
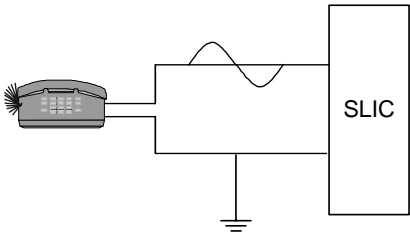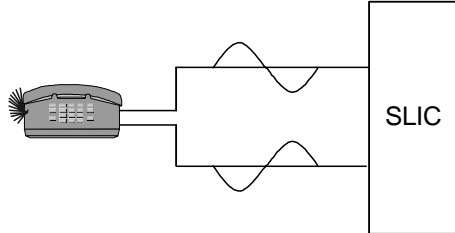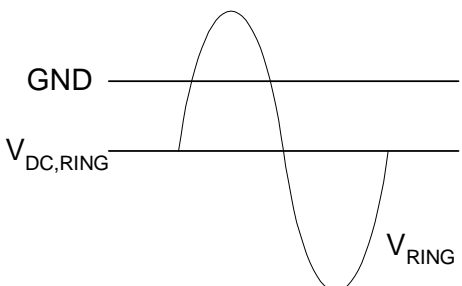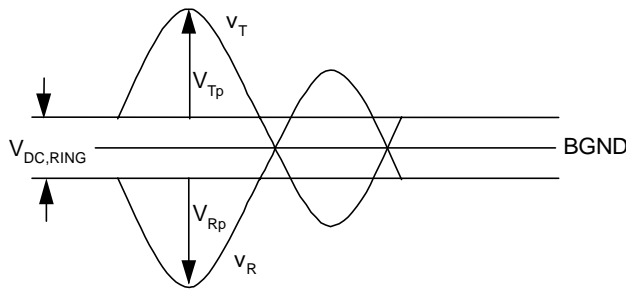
Most applications with DuSLIC are using DC ring trip detection, which is more reliable than AC ring trip detection.

2.4.3 Ringing Methods

There are two methods of ringing:

- Balanced ringing (bridged ringing)
- Unbalanced ringing (divided ringing)

Table 3   Unbalanced versus Balanced Ringing

Unbalanced Ringing:	Balanced Ringing:
The ringing signal is applied to only either the Tip or Ring line, whereas GND is applied to the other line.	An opposite-phase ringing signal is applied to both Tip and Ring lines. The resulting ringing signal is the differential signal between Tip and Ring line. $V_{RING} = V_T - V_R$ $V_T = V_{AC(t)} + V_{DC,RING}/2$ $V_R = -V_{AC(t)} - V_{DC,RING}/2$ If $V_T = -V_R$ then $V_{RING} = 2*V_{AC(t)} + V_{DC,RING}$
ezm140311.wmf	ezm140312.wmf
ezm140313.wmf	ezm140317.wmf

The resulting ringing amplitude in balanced mode is twice the amplitude of V_T or V_R. This is an advantage over the unbalanced mode because the ringing generator circuit in balanced mode has to handle voltages of only half the amplitude to generate the same amplitude of ringing signal. The SLIC process technology used is capable of generating balanced ringing signals with amplitudes of up to 85 V_{RMS}.

Internal balanced ringing generally offers more benefits compared to unbalanced ringing:

- Balanced ringing produces much less longitudinal voltage, which results in a lower amount of noise coupled into adjacent cable pairs
- By using a differential ringing signal, lower supply voltages become possible

The phone itself cannot distinguish between balanced and unbalanced ringing. Where unbalanced ringing is still used, it is often simply a historical leftover. For a comparison between balanced and unbalanced ringing see also ANSI document T1.401-1993.

Additionally, integrated ringing with the DuSLIC offers the following advantages:

- Internal ringing (no need for external ringing generator and relays)
- Reduction of board space because of much higher integration and fewer external components
- Programmable ringing amplitude, frequency and ringing DC offset without hardware changes
- Programmable ring trip thresholds
- Switching off the ringing signal at zero-crossing

2.4.4 DuSLIC Ringing Options

Application requirements differ with regard to ringing amplitudes, power requirements, loop length and loads. The DuSLIC options include three different SLICs to select the most appropriate ringing methods (see **Table 4**):

Table 4   Ringing Options with SLIC-S, SLIC-E/-E2 and SLIC-P

SLIC Version/ Ringing Facility, Battery Voltages	SLIC-S PEB 4264	SLIC-E/-E2 PEB 4265 PEB 4265-2	SLIC-P PEB 4266
Internal balanced ringing max. voltage in Vrms (sinusoidal) with 20 V_{DC} used for ring trip detection	45 Vrms	85 Vrms	85 Vrms
DC voltage for balanced ringing[1]	programmable typ. 0 … 50 V	programmable typ. 0 … 50 V	programmable typ. 0 … 50 V
Internal unbalanced ringing max. voltage in Vrms (sinusoidal)	NO	NO	50 Vrms
DC voltage for unbalanced ringing	NO	NO	$V_{BATR}/2$
Required SLIC supply voltages for maximum ringing amplitude (typically)	$V_{DD} = 5$ V, $V_{BATH} = -54$ V, $V_{HR} = 36$ V	$V_{DD} = 5$ V, $V_{BATH} = -70$ V, $V_{HR} = 80$ V	$V_{DD} = 5$ V or 3.3 V, $V_{BATH} = -70$ V, $V_{BATR} = -150$ V
Number of battery voltages for power saving	2 (V_{BATL} & V_{BATH})	2 (V_{BATL} & V_{BATH})	2 (when internal ringing is used) 3 (when external ringing is used)

[1] In most applications 20 V_{DC} are sufficient for reliable ring trip detection. A higher DC voltage will reduce the achievable maximum ringing voltage. For short loops 10 V_{DC} may be sufficient.

SLIC-S allows balanced ringing up to 45 Vrms and is dedicated for short loop or PBX applications.

For SLIC-S2 only external ringing is provided.

SLIC-E/-E2 allows balanced ringing up to 85 Vrms and can therefore be used in systems with higher loop impedance.

The low-power SLIC-P is optimized for power-critical applications (e.g. intelligent ISDN network termination). Internal ringing can be used up to 85 Vrms balanced or 50 Vrms unbalanced.

For lowest power applications where external ringing is preferred, three different battery voltages (V_{BATR}, V_{BATH}, V_{BATL}) can be used for optimizing the power consumption of the application.[1]

SLIC-E/-E2 and SLIC-P differ in supply voltage configuration and the ring voltages at Tip and Ring V_T and V_R. External ringing is supported by both SLIC's.

External Ringing Support by DuSLIC

External ringing requires an external ring signal generator and a TTL compatible zero crossing signal which has to be applied to the RSYNC pin of the *SLICOFI-2x*.

The ring relay is controlled by the IO1 pin. Due to the high current drive capability of the IO1 ouput, no additional relay driver is necessary.

The relay can be switched:

• **Synchronous:** The ring relay is switched at the zero crossing of the external ringing frequency.
• **Asynchronous**: The ring relay is switched immediately with the ring command.

---

[1] In this case V_{BATR} is typically used for the on-hook state, while V_{BATH} and V_{BATL} are used for optimized feeding of different loop length in the off-hook state.

2.4.5 Internal Balanced Ringing via SLICs

SLIC-E/-E2 and SLIC-P support internal balanced ringing up to $V_{RING,RMS}$ = 85 Vrms, SLIC-S support balanced ringing up to $V_{RING,RMS}$ = 45 Vrms.

The ringing signal is generated digitally within *SLICOFI-2x*[1].
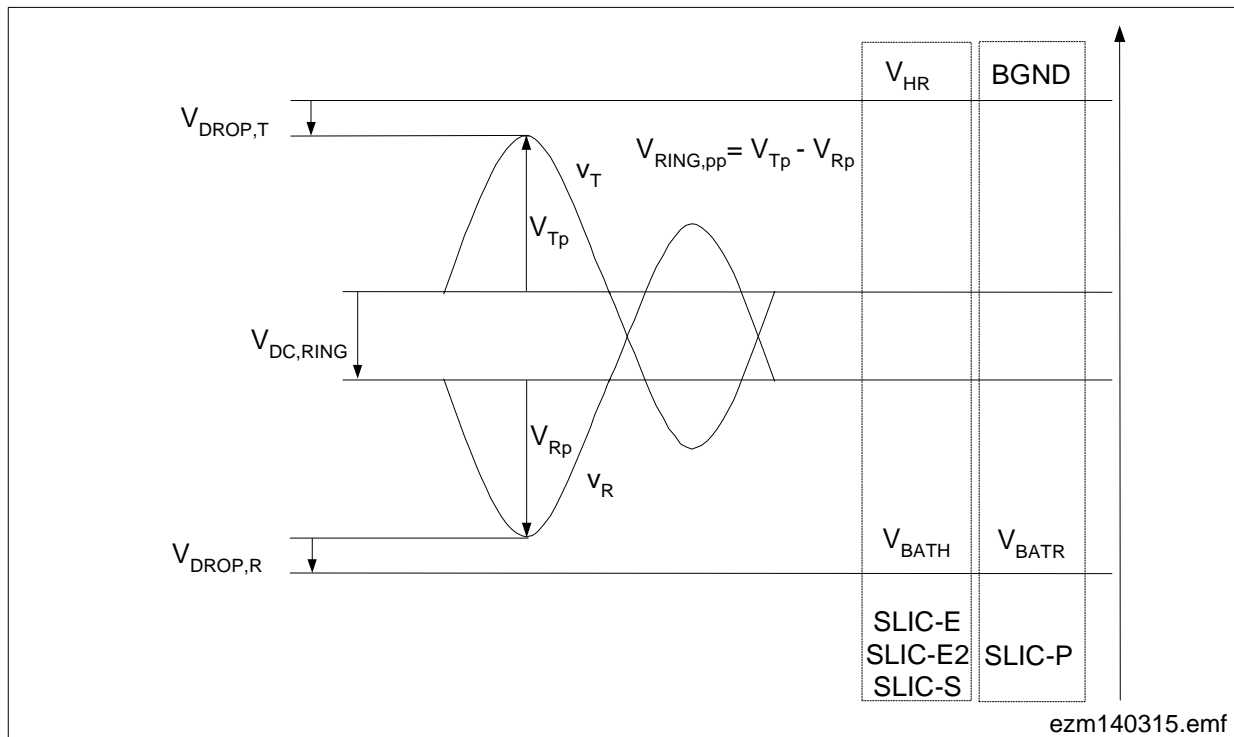
Figure 21   Balanced Ringing via SLIC-E/-E2, SLIC-S and SLIC-P

In ringing mode, the DC feeding regulation loop is not active. A programmable ring offset voltage is applied to the line instead. During ring bursts, the ringing DC offset and the ringing signal are summed digitally within *SLICOFI-2x* in accordance with the programmed values. This signal is then converted to an analog signal and applied to the SLIC. The SLIC amplifies the signal and supplies the line with ringing voltages up to 85 Vrms. In balanced ringing mode, the SLIC uses an additional supply voltage V_{HR} for SLIC-E/-E2/-S and V_{BATR} for SLIC-P. The total supply span is now $V_{HR} - V_{BATH}$ for SLIC-E/-E2/-S and V_{BATR} for SLIC-P.

The maximum ringing voltage that can be achieved is:

for SLIC-E/-E2/-S: $V_{RING,RMS} = (V_{HR} - V_{BATH} - V_{DROP, RT} - V_{DC,RING})/1.41$

for SLIC-P: $V_{RING,RMS} = (- V_{BATR} - V_{DROP,RT} - V_{DC,RING})/1.41$

where: $V_{DROP,RT} = V_{DROP,T} + V_{DROP,R}$

---

[1] SLICOFI-2S2 supports only external ringing

With the DuSLIC ringing voltages up to 85 Vrms sinusoidal can be applied, but also trapezoidal ringing can be programmed.

The SLIC senses the transversal current on the line and supplies this information to the *SLICOFI-2x* at the IT pin. The IT current is monitored by *SLICOFI-2x*. If the DC current exceeds the programmed ring trip threshold, *SLICOFI-2x* generates an interrupt. Ring trip is reliably detected and reported within two ring signal periods. The ringing signal is switched off during zero crossing by the *SLICOFI-2x*. For a detailed application diagram of internal balanced ringing refer to the chapter on "Application Circuits" (see **Figure 50**, **Page 96**).

2.4.6 Internal Unbalanced Ringing with SLIC-P

The internal unbalanced ringing together with SLIC-P can be used for ringing voltages up to 50 Vrms. The SLICOFI-2 integrated ringing generator is used and the ringing signal is applied to either the Tip or Ring line. Ringing signal generation is the same as described above for balanced ringing. Since only one line is used for ringing, technology limits the ringing amplitude to about half the value of balanced ringing, to maximum 50 Vrms.
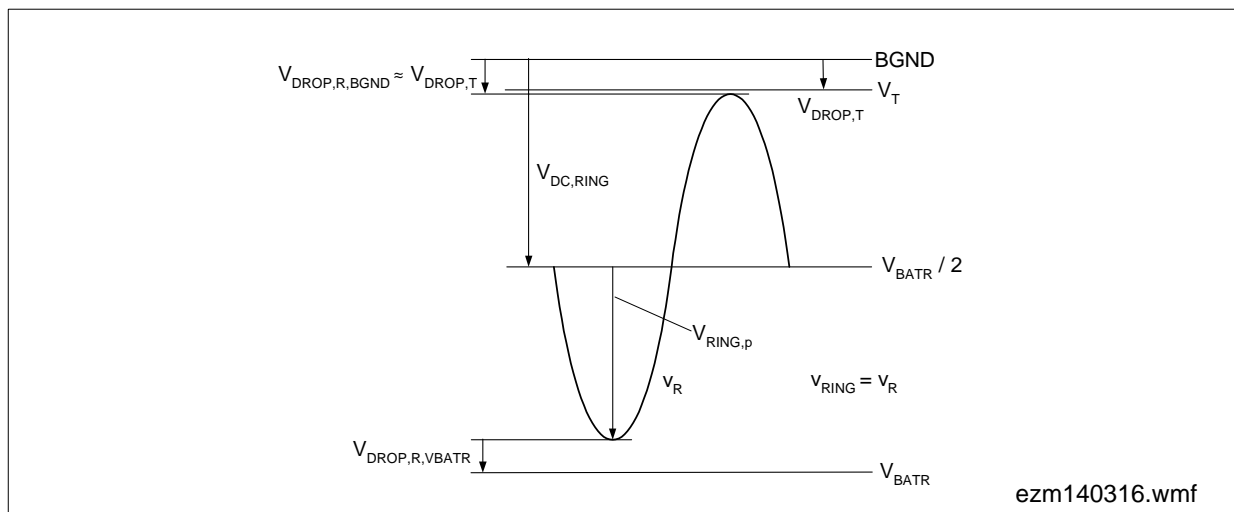
Figure 22   Unbalanced Ringing Signal

The above diagram shows an example with the ring line used for ringing and the Tip line fixed at $-V_{DROP,T}$ which is the drop in the output buffer of the Tip line of SLIC-P (typ. < 1 V). The ring line has a fixed DC voltage of $V_{BATR}/2$ used for ring trip detection.

The maximum ringing voltage is:

$$V_{RING,RMS} = (-V_{BATR} - V_{DROP,R,VBATR} - V_{DROP,T})/2.82$$

When the called subscriber goes off-hook, a DC path is established from the Ring to the Tip line. The DC current is recognized by the SLICOFI-2 because it monitors the IT pin. An interrupt indicates ring trip if the line current exceeds the programmed threshold.

The same hardware can be used for integrated balanced or unbalanced ringing. The balanced or unbalanced modes are configured by software. The maximum achievable amplitudes depend on the values selected for V_{BATR}.

In both balanced and unbalanced ringing modes, SLICOFI-2 automatically applies and removes the ringing signal during zero-crossing. This reduces noise and cross-talk to adjacent lines.

2.4.7   External Unbalanced Ringing

SLICOFI-2x supports external ringing for higher ringing voltage requirements with all SLICs. In this case DuSLICs integrated ring trip functionality is used. For a detailed application diagram of unbalanced ringing see **Figure 53** (**Page 100**) and **Figure 54** (**Page 101**).

Since high voltages are involved, an external relay should be used to switch the RING line off and to switch the external ringing signal together with a DC voltage to the line. The DC voltage has to be applied for the internal ring trip detection mechanism which operates for external ringing in the same way as for internal ringing.

The *SLICOFI-2x* has to be set to the external ringing mode. A synchronization signal of the external ringer is applied to the *SLICOFI-2x* via the RSYNC pin. The external relay is switched on or off synchronously to this signal via the IO1 pin of the *SLICOFI-2x* according to the actual mode of the DuSLIC. An interrupt is generated if the DC current exceeds the programmed ring trip threshold.

2.5   Signaling (Supervision)

Signaling in the subscriber loop is monitored internally by the DuSLIC chip set.

Supervision is performed by sensing the longitudinal and transversal line currents on the Ring and Tip wires. The scaled values of these currents are generated in the SLIC and fed to the *SLICOFI-2x* via the IT and IL pins.

Transversal line current: $I_{\text{TRANS}} = (I_R + I_T)/2$

Longitudinal line current: $I_{\text{LONG}} = (I_R - I_T)/2$

where I_R, I_T are the loop currents on the Ring and Tip wires.

Off-hook Detection

Loop start signaling is the most common type of signaling. The subscriber loop is closed by the hook switch inside the subscriber equipment.

• In Active mode, the resulting transversal loop current is sensed by the internal current sensor in the SLIC. The IT pin of the SLIC indicates the subscriber loop current to the *SLICOFI-2x*. External resistors (R_{IT1}, R_{IT2}, see **Figure 50**) convert the current information to a voltage on the ITA (or ITB) pin.
  The analog information is first converted to a digital value. It is then filtered and processed further which effectively suppresses line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.
• In Sleep/Power Down mode (PDRx) a similar mechanism is used. In this mode, the internal current sensor of the SLIC is switched off to minimize power consumption. The loop current is therefore fed and sensed through 5 kΩ resistors integrated in the SLIC. The information is made available on the IT pin and interpreted by the *SLICOFI-2x*.
– In Sleep mode, the analog information is fed to an analog comparator integrated in the *SLICOFI-2x* who directly indicates off-hook.
– In Power Down mode, the *SLICOFI-2x* converts the analog information to a digital value. It is then filtered and processed further which effectively suppresses line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.

In applications using ground start signaling, DuSLIC can be set in the ground start mode. In this mode, the Tip wire is switched to high impedance mode. Ring ground detection is performed by the internal current sensor in the SLIC and transferred to the *SLICOFI-2x* via the IT pin.

Ground Key Detection

The scaled longitudinal current information is transferred from the SLIC via the IL pin and the external resistor R_{IL} to *SLICOFI-2x*. This voltage is compared with a fixed threshold value. For the specified R_{IL} (1.6 kΩ, see application circuit **Figure 50**) this threshold corresponds to 17 mA (positive and negative). After further post-processing, this information generates an interrupt and ground key detection is indicated.

The post-processing is performed to guarantee ground key detection, even if longitudinal AC currents with frequencies of $16^2/_3$, 50 or 60 Hz are superimposed. The time delay between triggering the ground key function and registering the ground key interrupt will in most cases (f = 50 Hz, 60 Hz) be less than 40 ms.

In Power Down mode, the SLIC's internal current sensors are switched off and ground key detection is disabled.

2.6 Metering

There are two different metering methods:

- Metering by sinusoidal bursts with either 12 or 16 kHz or
- Polarity reversal of Tip and Ring.

2.6.1 Metering by 12/16 kHz Sinusoidal Bursts

The required amplitude of the sinusoidal 12 or 16 kHz metering signals varies from a few hundred millivolts to several V$_{RMS}$, depending on the country specifications and the application (long loop or short loop application). These signals are superimposed onto the speech signal. As soon as metering pulses are applied to the subscriber line, they also divert to the transmit signal path which means that a notch filter has to block the 12/16 kHz signal, to prevent overloading the transmit A/D converter. In contrast to conventional line circuits, the DuSLIC chip set generates the metering signal internally. The fact that the adaptive notch filter is integrated is one of the big advantages of DuSLIC.

Teletax Metering and Filtering

To satisfy worldwide application requirements, SLICOFI-2/-2S[1] offers integrated metering injection of either 12 or 16 kHz signals with programmable amplitudes. SLICOFI-2/-2S also has an integrated adaptive TTX notch filter and can switch the TTX signal to the line in a smooth way. When switching the signal to the line, the switching noise is less than 1 mV. **Figure 23** shows TTX bursts at certain points of the signal flow within SLICOFI-2/-2S.

---

[1] Metering is not available with SLICOFI-2S2
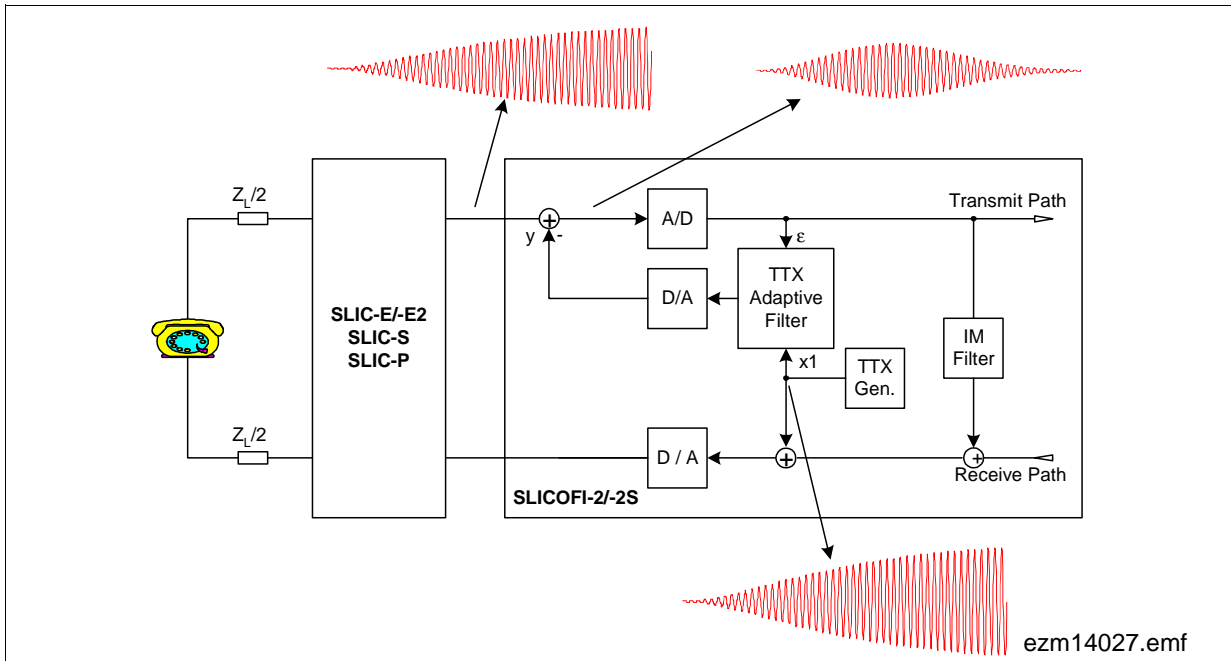
Figure 23   Teletax Injection and Metering

The integrated, adaptive TTX notch filter guarantees an attenuation of > 40 dB.
No external components for filtering TTX bursts are required.

2.6.2 Metering by Polarity Reversal

SLICOFI-2/-2S also supports metering by changing the actual polarity of the voltages on the TIP/RING lines. Metering with polarity reversal is usually used for pay phones (coin lines). Every time the polarity changes, a magnet in the pay phone releases a coin.

2.6.2.1 Soft reversal

Some applications require a smooth polarity reversal (soft reversal), as shown in **Figure 24**. Soft reversal helps to prevent negative effects like non-required ringing. Soft reversal is deactivated by the SOFT-DIS bit in register BCR2.

SOFT-DIS = 1   Immediate reversal is performed (hard reversal)

SOFT-DIS = 0   Soft reversal is performed. Transition time (time from START to SR-END1, see **Figure 24**) is programmable by CRAM-coefficients, default value 80 ms.
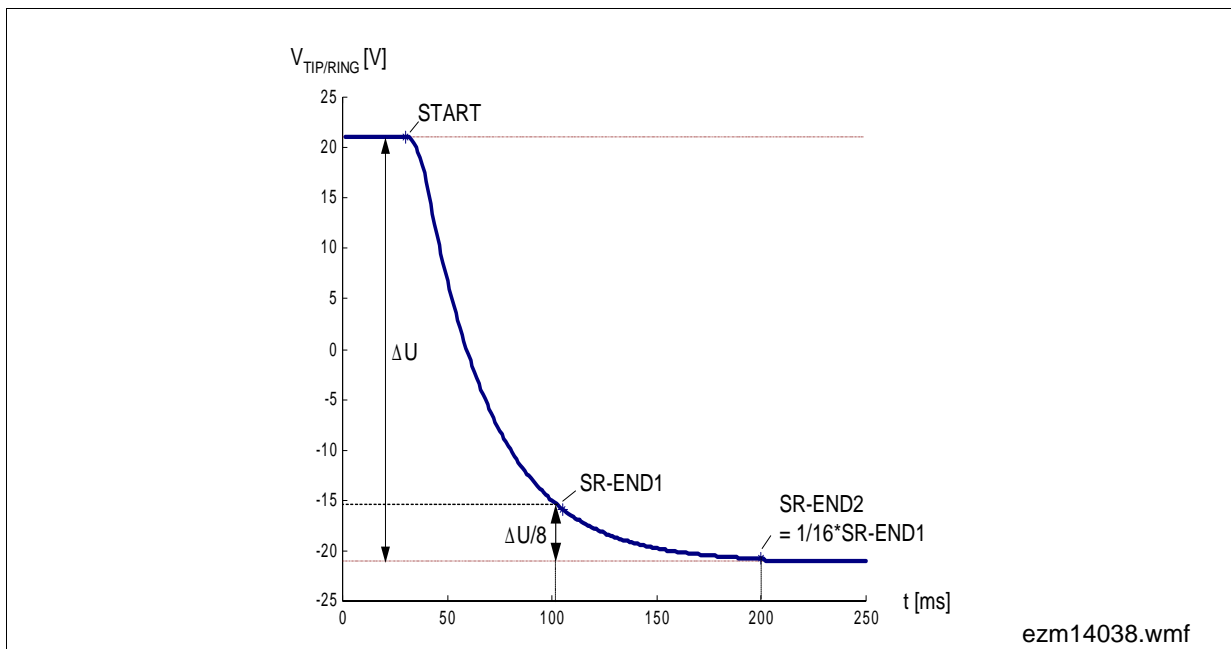
Figure 24   Soft Reversal (Example for Open Loop)

START: The soft ramp starts by setting the REVPOL bit in register BCR1 to 1.
The DC characteristic is switched off.
SR-END1: At the soft reversal end one point, the DC characteristic is switched on again. Programmable by the DuSLICOS software, e.g. $\Delta U/8$.
SR-END2: At the soft reversal end two point, the soft ramp is switched off. Programmable by the DuSLICOS software, e.g. 1/16*SR-END1.

2.7 DuSLIC Enhanced Signal Processing Capabilities

The signal processing capabilities described in this chapter are realized by an Enhanced Digital Signal Processor (EDSP) except for DTMF generation. Each function can be individually enabled or disabled for each DuSLIC channel. Therefore power consumption can be reduced according to the needs of the application.

Figure 25 shows the AC signal path for DuSLIC with the ADCs and DACs, impedance matching loop, thranshybrid filter, gain stages and the connection to the EDSP.
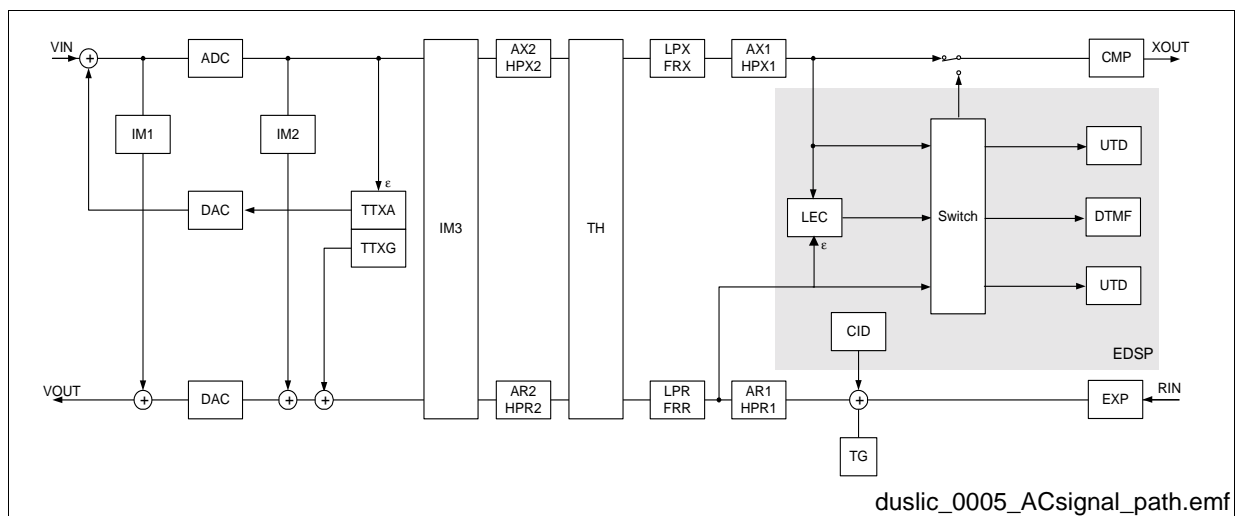
Figure 25   DuSLIC AC Signal Path

2.7.1 DTMF Generation and Detection[1]

Dual Tone Multi-Frequency (DTMF) is a signaling scheme using voice frequency tones to signal dialing information. A DTMF signal is the sum of two tones, one from a low group (697 - 941 Hz) and one from a high group (1209 - 1633 Hz), with each group containing four individual tones. This scheme allows 16 unique combinations. Ten of these codes represent the numbers from zero through nine on the telephone keypad, the remaining six codes (*, #, A, B, C, D) are reserved for special signaling. The buttons are arranged in a matrix, with the rows determining the low group tones, and the columns determining the high group tone for each button.

In all *SLICOFI-2x* codec versions the 16 standard DTMF tone pairs can be generated independently in each channel via two integrated tone generators. Alternatively the frequency and the amplitude of the tone generators can be programmed individually via the digital interface. Each tone generator can be switched on and off. The generated DTMF tone signals meet the frequency variation tolerances specified in the ITU-T Q.23 recommendation.

---

[1] DTMF Detection only available for DuSLIC-E/-E2/-P

Both channels (A and B) of SLICOFI-2[1] have a powerful built-in DTMF decoder that will meet most national requirements. The receiver algorithm performance meets the quality criteria for central office/exchange applications. It complies among others with the requirements of ITU-T Q.24, Bellcore GR-30-CORE (TR-NWT-000506) and Deutsche Telekom network (BAPT 223 ZV 5, Approval Specification of the Federal Office for Post and Telecommunications, Germany).

The performance of the algorithm can be adapted according to the needs of the application via the digital interface (detection level, twist, bandwidth and center frequency of the notch filter).

Table 5 shows the performance characteristics of the DTMF decoder algorithm:

Table 5   Performance Characteristics of the DTMF Decoder Algorithm

	Characteristic	Value	Notes
1	Valid input signal detection level	– 48 to 0 dBm0	Programmable
2	Input signal rejection level	– 5 dB of valid signal detection level	–
3	Positive twist accept	< 8 dB	Programmable
4	Negative twist accept	< 8 dB	Programmable
5	Frequency deviation accept	< ± (1.5% + 4 Hz) and < ± 1.8%	Related to center frequency
6	Frequency deviation reject	> ± 3%	Related to center frequency
7	DTMF noise tolerance (could be the same as 14)	– 12 dB	dB referenced to lowest amplitude tone
8	Minimum tone accept duration	40 ms	–
9	Maximum tone reject duration	25 ms	–
10	Signaling velocity	≥ 93 ms/digit	–
11	Minimum inter-digit pause duration	40 ms	–
12	Maximum tone drop-out duration	20 ms	–
13	Interference rejection 30 Hz to 480 Hz for valid DTMF recognition	Level in frequency range 30 Hz … 480 Hz ≤ level of DTMF frequency + 22 dB	dB referenced to lowest amplitude tone

---

[1] DTMF Detection only available for DuSLIC-E/-E2/-P

Table 5 **Performance Characteristics of the DTMF Decoder Algorithm** (cont'd)

	Characteristic	Value	Notes
14	Gaussian noise influence Signal level – 22 dBm0, SNR = 23 dB	Error rate better than 1 in 10000	–
15	Pulse noise influence Impulse noise tape 201 according to Bellcore TR-TSY-000762	Error rate better than 14 in 10000	measured with DTMF level – 22 dBm0 Impulse Noise – 10 dBm0 and – 12 dBm0

In the event of pauses < 20 ms:

• If the pause is followed by a tone pair with the same frequencies as before, this is interpreted as drop-out.
• If the pause is followed by a tone pair with different frequencies and if all other conditions are valid, this is interpreted as two different numbers.

DTMF decoders can be switched on or off individually to reduce power consumption. In normal operation, the decoder monitors the Tip and Ring wires via the ITAC pins (transmit path). Alternatively the decoder can be switched also in the receive path. On detecting a valid DTMF tone pair, SLICOFI-2 generates an interrupt via the appropriate INT pin and indicates a change of status. The DTMF code information is provided by a register which is read via the digital interface.

The DTMF decoder also has excellent speech-rejection capabilities and complies with Bellcore TR-TSY-000763. The algorithm has been fully tested with the speech sample sequences in the Series-1 Digit Simulation Test Tapes for DTMF decoders from Bellcore.

2.7.2   Caller ID Generation (only DuSLIC-E/-E2/-P)

A generator to send calling line identification (Caller ID, CID) is integrated in the DuSLIC chip set. Caller ID is a generic name for the service provided by telephone utilities that supply information like the telephone number or the name of the calling party to the called subscriber at the start of a call. In call waiting, the Caller ID service supplies information about a second incoming caller to a subscriber already busy with a phone call.

In typical Caller ID (CID) systems, the coded calling number information is sent from the central exchange to the called phone. This information can be shown on a display on the subscriber telephone set. In this case, the Caller ID information is usually displayed before the subscriber decides to answer the incoming call. If the line is connected to a computer, caller information can be used to search in databases and additional services can be offered.

There are two methods used for sending CID information depending on the application and country-specific requirements:

- Caller ID generation using DTMF signaling (see **Chapter 2.7.1**)
- Caller ID generation using FSK

DuSLIC contains DTMF generation units and FSK generation units which can be used for both channels simultaneously.

DuSLIC FSK Generation

Different countries use different standards to send Caller ID information. The DuSLIC chip set is compatible with the widely used standards Bellcore GR-30-CORE, British Telecom (BT) SIN227, SIN242 or the UK Cable Communications Association (CCA) specification TW/P&E/312. Continuous phase binary frequency shift keying (FSK) modulation is used for coding which is compatible with BELL 202 (see **Table 6**) and ITU-T V.23, the most common standards. SLICOFI-2 can be easily adapted to these requirements by programming via the microcontroller interface. Coefficient sets are provided for the most common standards.

Table 6   FSK Modulation Characteristics

Characteristic	ITU-T V.23	Bell 202
Mark (Logic 1)	1300 ± 3 Hz	1200 ± 3 Hz
Space (Logic 0)	2100 ± 3 Hz	2200 ± 3 Hz
Modulation	FSK	
Transmission rate	1200 ± 6 baud	
Data format	Serial binary asynchronous	

The Caller ID data of the calling party can be transferred via the microcontroller interface into a SLICOFI-2 buffer register. The SLICOFI-2 will start sending the FSK signal when the CIS-EN bit is set and the CID-data buffer is filled up to CIS-BRS plus 1 byte. The data transfer into the buffer register is handled by a SLICOFI-2 interrupt signal. Caller data is transferred from the buffer via the interface pins to the SLIC-E/-E2/-P and fed to the Tip and Ring wires. The Caller ID data bytes from CID-data buffer are sent LSB first.

DuSLIC offers two different levels of framing:

• A basic low-level framing mode

All the data necessary to implement the FSK data stream – including channel seizure, mark sequence and framing for the data packet or checksum – has to be configured by firmware. SLICOFI-2 transmits the data stream in the same order in which the data is written to the buffer register.

• A high level framing mode

The number of channel seizure and mark bits can be programmed and are automatically sent by the DuSLIC. Only the data packet information has to be written into the CID buffer. Start and stop bits are automatically inserted by the SLICOFI-2.

The example below shows signaling of CID on-hook data transmission in accordance with Bellcore specifications. The Caller ID information applied on Tip and Ring is sent during the period between the first and second ring burst.

Bellcore On-hook Caller ID Physical Layer Transmission

1 Message length equals the number of bytes to follow in the message body, excluding the checksum.
A: 0.2-3 second ring burst.
B: 0.5-1.5 seconds between first ring burst and start of data transmission.
C: 300 alternating mark and space bits.
D: 180 mark bits.
C + D + E = 2.9 to 3.7 seconds.
F: ≥ 200ms
G: 1.8-3 second ring burst

ezm14014.wmf
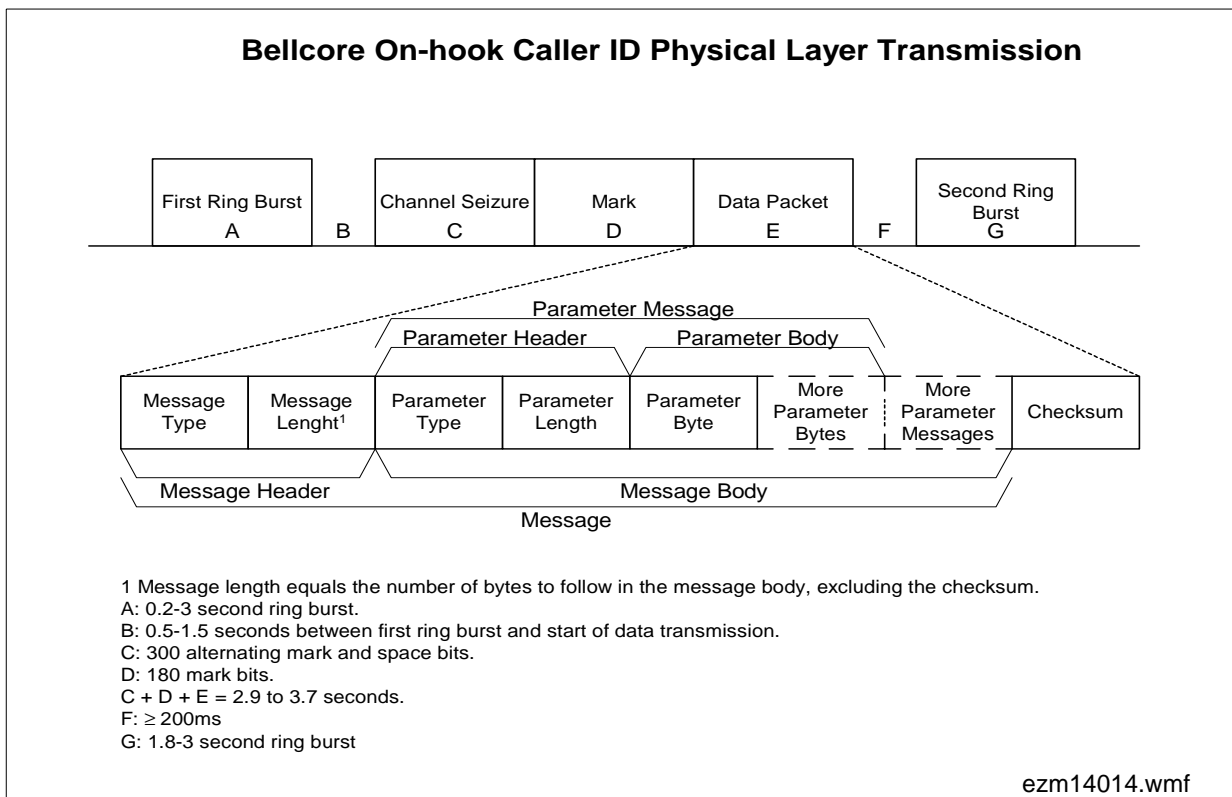
Figure 26   Bellcore On-hook Caller ID Physical Layer Transmission

2.7.3 Line Echo Cancelling (LEC) (only DuSLIC-E/-E2/-P)

The DuSLIC contains an adaptive line echo cancellation unit for the cancellation of near end echoes. With the adaptive balancing of the LEC unit the transhybrid loss can be improved up to a value of about 50 dB. The maximum echo cancellation time selectable is 8 ms. The line echo cancellation unit is especially useful in combination with the DTMF detection unit. In critical situations the performance of the DTMF detection can be improved.

The DuSLIC line echo canceller is compatible with applicable standards ITU-T G.165 and G.168. An echo cancellation delay time of up to 8 ms can be programmed.

The LEC unit consists basically of an FIR filter, a shadow FIR filter, and a coefficient adaption mechanism between these two filters as shown in **Figure 27**.
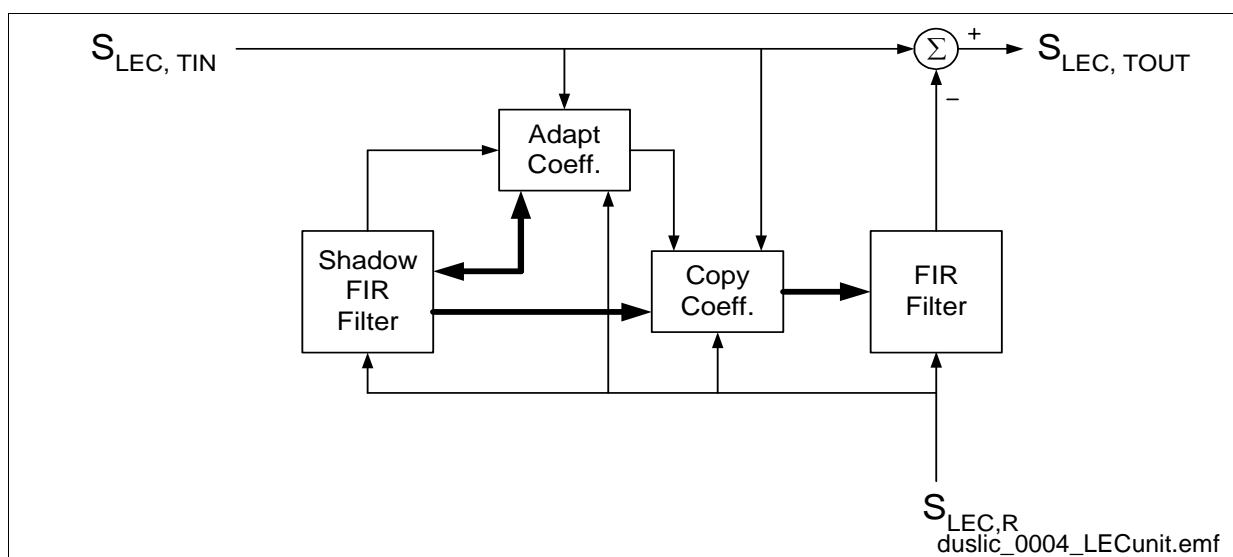
Figure 27   Line Echo Cancellation Unit - Block Diagram

The adaption process is controlled by the three parameters Pow_{LECR} (Power Detection Level Receive), $DeltaP_{LEC}$ (Delta Power) and DeltaQ (Delta Quality). Adaptation takes place only if both of the following conditions hold:

1. $S_{LEC,R} > Pow_{LECR}$
2. $S_{LEC,R} - S_{LEC,TIN} > DeltaP_{LEC}$

With the first condition, adaptation to small signals can be avoided. The second condition avoids adaptation during double talk. The parameter $DeltaP_{LEC}$ represents the echo loss provided by external circuitry.

If the adaptation of the shadow filter is performed better than the adaption of the actual filter by a value of more than DeltaQ then the shadow filter coefficients will be copied to the actual filter.

At the start of an adaption process the coefficients of the LEC unit can be reset to default initial values or set to the old coefficient values. The coefficients may also be frozen.

2.7.4   Universal Tone Detection (UTD) (only DuSLIC-E/-E2/-P)

Each channel of the DuSLIC has two Universal Tone Detection units which can be used to detect special tones in the receive and transmit paths, especially fax or modem tones (e.g., see the modem startup sequence described in recommendation ITU-T V.8).

This allows the use of modem-optimized filter for V.34 and V.90 connections. If the DuSLIC UTD detects that a modem connection is about to be established, the optimized filter coefficients for the modem connection can be downloaded before the modem connection is set up. With this mechanism implemented in the DuSLIC chip set, the optimum modem transmission rate can always be achieved.

Figure 28 shows the functional block diagram of the UTD unit:
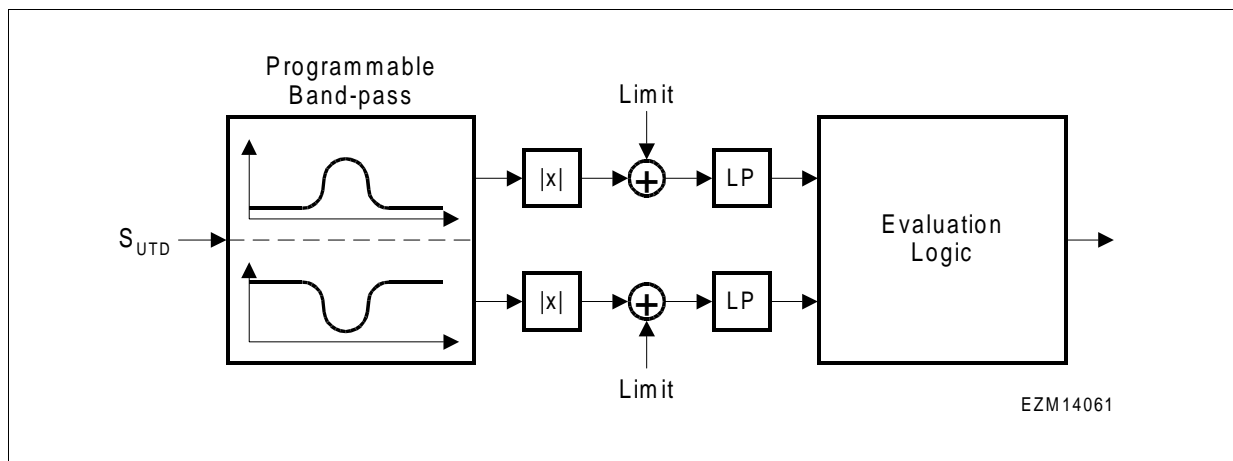
Figure 28   UTD Functional Block Diagram

Initially, the input signal is filtered by a programmable band-pass (center frequency f_C and bandwidth f_{BW}). Both the in-band signal (upper path) and the out-of-band signal (lower path) are determined, and the absolute value is calculated. Both signals are furthermore filtered by a limiter and a low-pass. All signal samples (absolute values) below a programmable limit Lev_N (Noise Level) are set to zero and all other signal samples are diminished by Lev_N. The purpose of this limiter is to increase noise robustness. After the limiter stages both signals are filtered by a fixed low-pass.

The evaluation logic block determines whether a tone interval or silence interval is detected and an interrupt is generated for the receive or transmit path.

If the bandwidth parameter is programmed to a negative value, the UTD unit can be used for the detection of silence intervals in the whole frequency range.

The DuSLIC UTD unit is compatible with ITU-T G.164.

The UTD is resistant to a modulation with 15 Hz sinusoidal signals and a phase reversal but is not able to detect the 15 Hz modulation and the phase reversal.

2.8 Message Waiting Indication (only DuSLIC-E/-E2/-P)

Message Waiting is a function that can be required by PBX applications. A Message Waiting Indication (MWI) lamp is activated indicating to the subscriber that a message has arrived.

The DuSLIC Message Waiting function uses a glow lamp at the subscriber phone. Current does not flow through a glow lamp until the voltage reaches a threshold value of approximately 80 V. At this threshold, the neon gas in the lamp will start to glow. When the voltage is reduced, the current falls under a certain threshold and the lamp is extinguished. DuSLIC has high-voltage SLIC technology (170 V) which is able to activate the glow lamp without any external components.

The hardware circuitry is shown in **Figure 29** below. The figure shows a typical telephone circuit with the hook switch in the on-hook mode, together with the impedances for the on-hook (Z_R) and off-hook (Z_L) modes.

Z_L	AC Impedance
Z_R	Ringer Impedance
R_{MW}	Pre Resistor Message Waiting

ezm14066.wmf
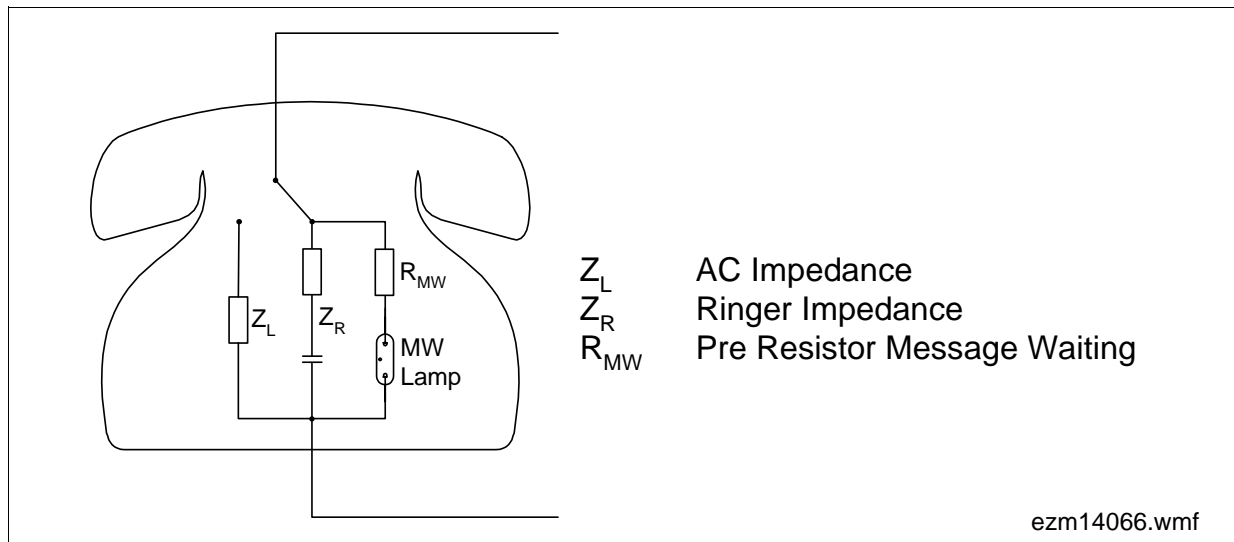
Figure 29   MWI Circuitry with Glow Lamp

The glow lamp circuit also requires a resistor (R_{MW}) and a lamp (MW Lamp) built into the phone. When activated, the lamp must be able to either blink or remain on constantly .

In non-DuSLIC solutions the telephone ringer may respond briefly if the signal slope is too steep, which is not desirable. DuSLIC's integrated ramp generator can be programmed to increase the voltage slowly, to ensure activating the lamp and not the ringer.

2.9 Three-party Conferencing

Each DuSLIC channel has a three-party conferencing facility consisting of four PCM registers, adders and gain stages in the microprogram and the corresponding control registers (see **Figure 30**). Cascading DuSLIC channels allows even Multi-party Conferencing. Three-party conferencing is available in PCM/µC-mode only.
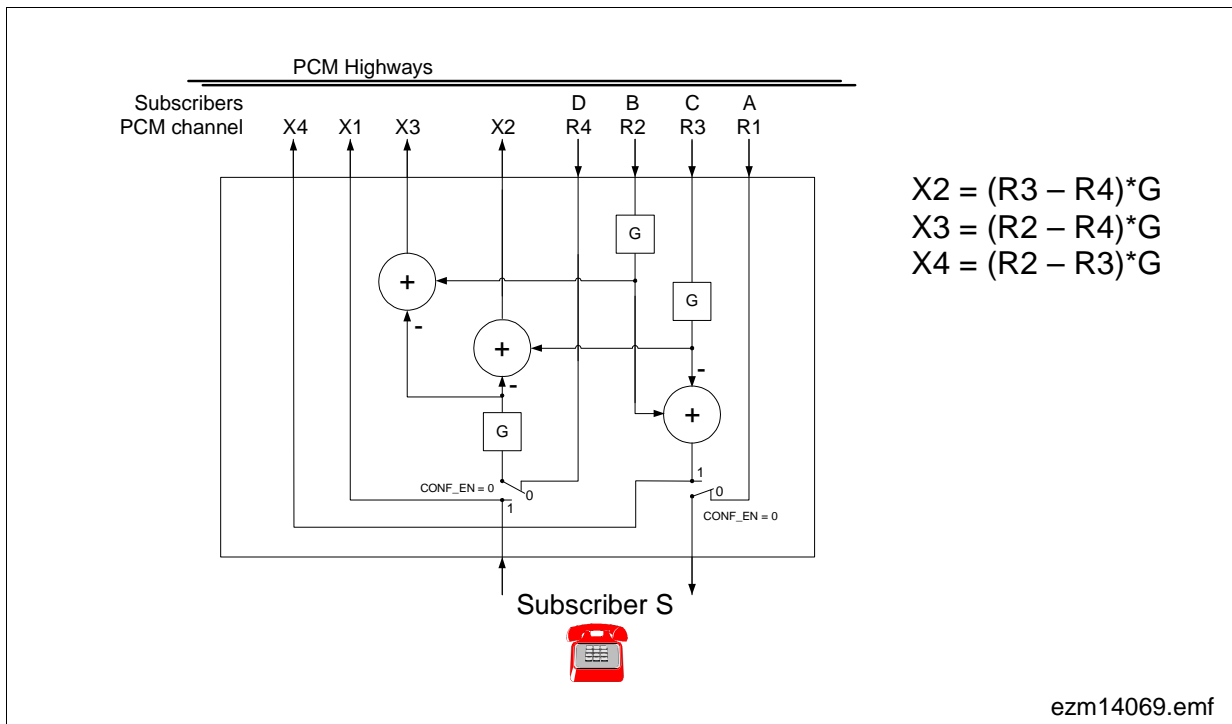
Figure 30 **Conference Block for one DuSLIC Channel**

Note: G...Gain Stage (Gain Factor),
X1-X4...PCM transmit channels, R1-R4...PCM receive channels,
A, B, C, D, S...examples for voice data on PCM channels X1-X4, R1-R4

Table 7 shows all possible three-party conferencing modes and the corresponding selection of the PCM transmit and receive channels X1 to X4 and R1 to R4 (see also **Figure 30**). The timeslot assignment, the PCM-highway selection, the PCM line drivers and the behaviour of the conferencing facility itself are controled by various registers[1]. A programmable gain stage G is able to adjust the gain of the conferencing voice data (B, C, D, S) in a range of – 6 dB to + 3 dB to prevent overload of the sum signals.

---

[1] not to be explained in this document.

2.9.1 Conferencing Modes

Table 7 Conference Modes

Mode	Receive PCM Channels				Transmit PCM Channels				Subscriber S
	R1	R2	R3	R4	X1	X2	X3	X4	
PCM Off					off	off	off	off	off
PCM Active	A				S	off	off	off	A
External Conference		B	C	D	off	G·(B+D)	G·(C+D)	G·(B+C)	off
External Conference + PCM Active	A	B	C	D	S	G·(B+D)	G·(C+D)	G·(B+C)	A
Internal conference		B	C		off	G·(B+S)	G·(C+S)	off	G·(B+C)

- **PCM Off**
  After a reset, or in power down there is no communication via the PCM highways. Also when selecting new timeslots it is recommended to switch off the PCM line drivers by setting the control bits to zero.
- **PCM Active**
  This is the normal operating mode without conferencing. Only the channels R1 and X1 are in use, and voice data are transferred from subscriber A to analog subscriber S and vice versa.
- **External Conference**
  In this mode the SLICOFI-2 acts as a server for a three-party conference of subscribers B, C and D which may be controlled by any device connected to the PCM highways. The SLICOFI-2 channel itself can remain in power down mode to lower power consumption.
- **External Conference + PCM Active**
  Like in External Conference mode any external three-party conference is supported. At the same time an internal phone call is active using the channels R1 and X1.
- **Internal Conference**
  If the analog subscriber S is one of the conference partners, the internal conference mode will be selected. The partners (B, C) do not need any conference facility, since the SLICOFI-2 performs all required functions for them as well.

2.10   16 kHz Modes on PCM Highway

In addition to the standard 8-kHz transmission PCM-interface modes, there are also two 16-kHz modes for high data transmission performance.

Table 8 shows the configuration of the PCM channels for the different PCM interface modes.

Table 8   Possible Modes in PCM/μC Interface Mode

Config. Bits		Receive PCM Channels					Transmit PCM Channels				
PCM16K	LIN	R1	R1L[1]	R2	R3	R4	X1	X1L[2]	X2	X3	X4
PCM Mode											
0	0	A	[3]	B	C	D	S	–	depends on conference mode		
LIN Mode											
0	1	A-HB	A-LB	B	C	D	S-HB	S-LB	depends on conference mode		
PCM16 Mode											
1	0	DS1	–	–	DS2	–	DS1	–	–	DS2	–
LIN16 Mode											
1	1	DS1-HB	–	DS1-LB	DS2-HB	DS2-LB	DS1-HB	–	DS1-LB	DS2-HB	DS2-LB

[1] Time slot R1 + 1

[2] Time slot X1 + 1

[3] Empty cells in the table mark unused data in the PCM receive channels and switched-off line drivers in the PCM transmit channels

The configuration bits PCM16K and LIN (in the BCR3 register) are used to select the following PCM interface modes:

• **PCM Mode**

Normal mode used for voice transmission via channels R1 and X1 (receive and transmit). The PCM input channels R2, R3 and R4 are always available for use in different conference configurations. The status of the PCM output channels depends on the conference mode configuration.

- **LIN Mode**

Similar to the PCM mode, but for 16 bit linear data at 8 kHz sample rate via the PCM channels R1, R1L (receive) and X1, X1L (transmit).

- **PCM16 Mode**

Mode for higher data transmission rate of PCM encoded data using a 16 kHz sample rate (only in PCM/µC interface mode with specific register setting). In this mode the channels R1, R3 (X1, X3) are used to receive (transmit) two samples of data (DS1, DS2) in each 8 kHz frame.

- **LIN16 Mode**

Like the PCM16 mode for 16 kHz sample rate but for linear data. Channels R1 to R4 (X1 to X4) are used for receiving (transmitting) the high and low bytes of the two linear data samples DS1 and DS2.

- **LIN16 Mode:**

Like the PCM16 mode for the 16-kHz sample rate but for linear data. The channels R1 to R4 (X1 to X4) are used for receiving (transmitting) the high and low bytes of the two linear data samples DS1 and DS2.

3   Operational Description

3.1   Operating Modes for the DuSLIC Chip Set

Sleep (SL)

The SLICOFI-2 is able to go into a sleep mode with minimal power dissipation. In this mode off-hook detection is performed without any checks on spikes or glitches. Off-hook is detected by an analog comparator in SLICOFI-2 and transferred via the INT or the DU-pin. The sleep mode can be used for either channel, but for the most effective power saving, both channels should be set to this mode.

Power Down Resistive (PDRH for SLIC-E/-E2/-S/-S2 and PDRR for SLIC-P)

The Power Down Resistive mode is the standard mode for none-active lines. Off-hook is detected by a current value fed to the DSP, compared with a programmable threshold, and filtered by a data upstream persistence checker. The power management SLIC-P can be switched to a Power Down Resistive High (PDRH) or a Power Down Resistive Ring (PDRR) mode.

HIRT

The line drivers in the SLIC-E/-E2/-P are shut down and no resistors are switched to the line. Off-hook detection is not possible. In HIRT mode the SLICOFI-2 is able to measure the input offset of the current sensors.

Power Down High Impedance (PDH)

In Power Down High Impedance mode, the SLIC is totally powered down. No off-hook sensing can be performed. This mode can be used for emergency shutdown of a line.

Active High (ACTH)

A regular call can be performed, voice and metering pulses can be transferred via the telephone line and the DC loop is operational in the Active High mode.

Active Low (ACTL)

The Active Low mode is similar to the Active High mode. The only difference is that the SLIC uses a lower battery voltage, V_{BATL} (bit ACTL = 1).

Active Ring (ACTR)

The Active Ring mode is different for the SLIC-E/-E2 and the SLIC-P. The SLIC-E/-E2 uses the additional positive voltage V_{HR} for extended feeding and the SLIC-P will switch to the negative battery voltage V_{BATR}.

Ringing

If the *SLICOFI-2x* is switched to Ringing mode, the SLIC is switched to ACTR mode.

With the SLIC-P connected to the SLICOFI-2, the Ring on Ring (ROR) mode allows unbalanced internal ringing on the Ring wire. The Tip wire is set to battery ground. The ring signal will be superimposed by $V_{BATR}/2$.

The Ring on Tip (ROT) mode is the equivalent to the ROR mode.

Active with HIT

This is a testing mode where the Tip wire is set to a high impedance mode. It is used for special line testing. It is only available in an active mode of the *SLICOFI-2x* to enable all necessary test features.

Active with HIR

HIR is similar to HIT but with the Ring wire set to high impedance.

Active with Metering

Any available active mode can be used for metering either with Reverse Polarity or with TTX Signals.

Ground Start

The Tip wire is set to high impedance in Ground Start mode. Any current drawn on the Ring wire leads to a signal on IT, indicating off-hook.

Ring Pause

The ring burst is switched off in Ring Pause, but the SLIC remains in the specified mode and the off-hook recognition behaves like in ringing mode (Ring Trip).

3.2 Operating Modes for the DuSLIC-S/-S2 Chip Set

Table 9   **DuSLIC-S/-S2 Operating Modes**

SLICOFI-2S / SLICOFI-2S2 Mode	SLIC-S / SLIC-S2 Mode	SLIC-S/-S2 Internal Supply Voltages (+/−) $[V_{HI}/V_{BI}]$	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	Open/V_{BATH}	None	None	High Impedance
Power Down Resistive	PDRH	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL [1]	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BGND}/V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATL} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATL} − V_{AC} − V_{DC})/2$
Active High (ACTH)	ACTH	V_{BGND}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATH} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATH} − V_{AC} − V_{DC})/2$
Active Ring (ACTR)	ACTR	V_{HR}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX-generator (optional)	Tip: $(+ V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2$ Ring: $(+ V_{BATH} + V_{HR} − V_{AC} − V_{DC})/2$
Ringing (Ring)	ACTR	V_{HR}/V_{BATH}	Balanced ring signal feed (incl. DC offset)	Buffer, Sensor, DC loop, Ring generator	Tip: $(V_{BATH} + V_{HR} + V_{DC})/2$ Ring: $(V_{BATH} + V_{HR} − V_{DC})/2$

Table 9   DuSLIC-S/-S2 Operating Modes (cont'd)

SLICOFI-2S / SLICOFI-2S2 Mode	SLIC-S / SLIC-S2 Mode	SLIC-S/-S2 Internal Supply Voltages (+/−) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
Ring Pause	ACTR	V_{HR}/V_{BATH}	DC offset feed	Buffer, Sensor, DC loop, Ramp generator	Tip: (V_{BATH} + V_{HR} + V_{DC})/2 Ring: (V_{BATH} + V_{HR} − V_{DC})/2
Active with HIR	HIR	V_{HR}/V_{BATH}	E.g. line test (Tip)	Tip Buffer, Sensor, DC + AC loop	Tip: (V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2 Ring: High impedance
Active with HIT	HIT	V_{HR}/V_{BATH}	E.g. line test (Ring)	Ring Buffer, Sensor, DC + AC loop	Ring: (V_{BATH} + V_{HR} − V_{AC} − V_{DC})/2 Tip: High impedance

[1]   load ext. C for switching from PDRH to ACTH in on-hook mode

V_{AC} … Tip/Ring AC Voltage

V_{DC} … Tip/Ring DC Voltage

3.3 Operating Modes for the DuSLIC-E/-E2 Chip Set

Table 10   DuSLIC-E/-E2 Operating Modes

SLICOFI-2 Mode	SLIC-E / SLIC-E2 Mode	SLIC-E/-E2 Internal Supply Voltages (+/−) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	Open/V_{BATH}	None	None	High Impedance
Sleep	PDRH	Open/V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATH} (via 5 kΩ)
Power Down Resistive	PDRH	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL[1]	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BGND}/V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATL} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATL} - V_{AC} - V_{DC})/2$
Active High (ACTH)	ACTH	V_{BGND}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATH} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATH} - V_{AC} - V_{DC})/2$
Active Ring (ACTR)	ACTR	V_{HR}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(+ V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2$ Ring: $(+ V_{BATH} + V_{HR} - V_{AC} - V_{DC})/2$

Table 10   DuSLIC-E/-E2 Operating Modes (cont'd)

SLICOFI-2 Mode	SLIC-E / SLIC-E2 Mode	SLIC-E/-E2 Internal Supply Voltages (+/−) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
Ringing (Ring)	ACTR	V_{HR}/V_{BATH}	Balanced Ring signal feed (incl. DC offset)	Buffer, Sensor, DC loop, Ring generator	Tip: (V_{BATH} + V_{HR} + V_{DC})/2 Ring: (V_{BATH} + V_{HR} − V_{DC})/2
Ring Pause	ACTR	V_{HR}/V_{BATH}	DC offset feed	Buffer, Sensor, DC loop, ramp generator	Tip: (V_{BATH} + V_{HR} + V_{DC})/2 Ring: (V_{BATH} + V_{HR} − V_{DC})/2
HIRT	HIRT	V_{HR}/V_{BATH}	E.g. sensor offset calibration	Sensor, DC transmit path	High Impedance
Active with HIR	HIR	V_{HR}/V_{BATH}	E.g. line test (Tip)	Tip-Buffer, Sensor, DC + AC loop	Tip: (V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2 Ring: High impedance
Active with HIT	HIT	V_{HR}/V_{BATH}	E.g. line test (Ring)	Ring-Buffer, Sensor, DC + AC loop	Ring: (V_{BATH} + V_{HR} − V_{AC} − V_{DC})/2 Tip: High impedance

[1]   load ext. C for switching from PDRH to ACTH in on-hook mode

V_{AC} … Tip/Ring AC Voltage

V_{DC} … Tip/Ring DC Voltage

3.4 Operating Modes for the DuSLIC-P Chip Set

Table 11   DuSLIC P Operating Modes

SLICOFI-2 Mode	SLIC-P Mode	SLIC-P Internal Supply Voltages [V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	V_{BATR}	None	None	High impedance
Sleep	PDRH	V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATH} (via 5 kΩ)
Sleep	PDRR	V_{BATR}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATR} (via 5 kΩ)
Power Down Resistive	PDRH	V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL[1]	V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRR	V_{BATR}	Off-hook detect as in active mode (DSP)	Off-hook, Analog comparator	V_{BGND}/V_{BATR} (via 5 kΩ)
–	PDRRL[2]	V_{BATR}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATR} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATL} + V_{AC} + V_{DC})/2 Ring: (V_{BATL} − V_{AC} − V_{DC})/2
Active High (ACTH)	ACTH	V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATH} + V_{AC} + V_{DC})/2 Ring: (V_{BATH} − V_{AC} − V_{DC})/2

Table 11   **DuSLIC P Operating Modes** (cont'd)

SLICOFI-2 Mode	SLIC-P Mode	SLIC-P Internal Supply Voltages [V_{Bl}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
Active Ring (ACTR)	ACTR	V_{BATR}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATR} + V_{AC} + V_{DC})/2 Ring: (V_{BATR} − V_{AC} − V_{DC})/2
Ringing (Ring)	ACTR	V_{BATR}	Balanced ring signal feed (incl. DC offset)	Buffer, Sensor, DC loop, ring generator	Tip: (V_{BATR} + V_{DC})/2 Ring: (V_{BATR} − V_{DC})/2
Ringing (Ring)	ROR	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC loop, ring generator	Ring: (V_{BATR} − V_{DC})/2 Tip: 0 V
Ringing (Ring)	ROT	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC loop, ring generator	Tip: (V_{BATR} + V_{DC})/2 Ring: 0 V
Ring Pause	ACTR, ROR, ROT	V_{BATR}	DC offset feed	Buffer, Sensor, DC loop, ramp generator	Tip: (V_{BATR} + V_{DC})/2 Ring: (V_{BATR} − V_{DC})/2
HIRT	HIRT	V_{BATR}	E.g. sensor offset calibration	Sensor, DC transmit path	High impedance
Active with HIR	HIR	V_{BATR}	E.g. line test (Tip)	Tip-Buffer, Sensor, DC + AC loop	Tip: (V_{BATR} + V_{AC} + V_{DC})/2 Ring: High impedance
Active with HIT	HIT	V_{BATR}	E.g. line test (Ring)	Ring-Buffer, Sensor, DC + AC loop	Ring: (V_{BATR} − V_{AC} − V_{DC})/2 Tip: High impedance

[1]   load ext. C for switching from PDRH to ACTH in on-hook mode

[2]   load ext. C for switching from PDRR to ACTR in on-hook mode

3.5   Operating Modes and Power Management

In many applications, the power dissipated on the line card is a critical parameter. In larger systems, the mean power value (taking into account traffic statistics and line length distribution) determines cooling requirements. Particularly in remotely fed systems, the maximum power for a line must not exceed a given limit.

3.5.1   Introduction

Generally, system power dissipation is determined mainly by the high-voltage part. The most effective power-saving method is to limit SLIC functionality and reduce supply voltage in line with requirements. This is achieved using different operating modes.
The three main modes – Power Down, Active and Ringing – correspond to the main system states: on-hook, signal transmission (voice and/or TTX) and ring signal feed.

For power critical applications the Sleep mode can be used for even lower power consumption than in Power Down mode.

– Power Down

Off-hook detection is the only function available. It is realized by 5 kΩ resistors applied by the SLIC from Tip to V_{BGND} and Ring to V_{BAT}, respectively. A simple sensing circuit supervises the DC current through these resistors (zero in on-hook and non-zero in off-hook state). This scaled transversal line current is transferred to the IT pin and compared with a programmable current threshold in the *SLICOFI-2x*. Only the DC loop in the *SLICOFI-2x* is active.

In **Sleep** mode, all functions of the *SLICOFI-2x* are switched off except for off-hook detection which is still available via an analog comparator. Both AC and DC loops are inactive. To achieve the lowest power consumption of the DuSLIC chip set, the clock cycles fed to the MCLK and PCLK pins have to be shut off.
For changing into another state the DuSLIC has to be waked up.

– Active

Both AC and DC loops are operative. The SLIC provides low-impedance voltage feed to the line. The SLIC senses, scales and separates transversal (metallic) and longitudinal line currents. The voltages at Tip and Ring are always symmetrical with reference to half the battery voltage (no ground reference!). An integrated switch makes it possible to choose between two (SLIC-S/-S2, SLIC-E/-E2) or even three (SLIC-P) different battery voltages. With these voltages selected according to certain loop lengths, power optimized solutions can be achieved.

– Ringing

For SLIC-E/-E2 and SLIC-S, an auxiliary positive supply voltage V_{HR} is used to give a total supply range of up to 150 V. For SLIC-P the whole supply range is provided by V_{BATR}. The low-impedance line feed (R_{STAB} (2x30 Ω) + R_{FUSE} (2x20 Ω) + appr. 1 Ω $\approx$ 101 Ω output impedance) with a balanced sinusoidal Ring signal of up to 85 Vrms, plus a DC offset of 20 V, is sufficient to supply very long lines at any kind of ringer load and to reliable detect ring trip. Unbalanced ringing is supported by applying the Ring signal to only one line, while Ground is applied to the other line.

For an overview of all DuSLIC operating modes see **Table 9** for PEB 4264/-2, **Table 10** for PEB 4265/-2 and **Table 11** for PEB 4266.

3.5.2 Power Dissipation of the *SLICOFI-2x*

Table 12 and **Table 13** show typical power dissipation values for different operating modes of the SLICOFI-2 and SLICOFI-2S/-2S2 [1]. For an optimized power consumption of the SLICOFI-2 (**Table 12**) unused EDSP functions have to be switched off.

Conditions (all codecs):

$T_A = -40$ °C to 85 °C, unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{DDB} = V_{DDR} = V_{DDPLL} = 3.3$ V $\pm$ 5 %;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL} = 0$ V

Table 12   Power Dissipation PEB 3265 (SLICOFI-2)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power dissipation						
Sleep both channels	$P_{DDSleep}$	–	17	25	mW	(MCLK, PCLK = 2 MHz)
Power Down both channels	$P_{DDPDown}$	–	79	104	mW	–
Active one channel	P_{DDAct1}	–	129	160	mW	without EDSP
		–	142	174	mW	with 8 MIPS [1] (DTMF detection)
		–	155	191	mW	with 16 MIPS
Active both channels	P_{DDAct2}	–	182	243	mW	without EDSP
		–	231	315	mW	with 32 MIPS

[1] MIPS = million instructions per second (performed by the EDSP)

---

[1] For more detailed characteristics see the DuSLIC Data Sheet.

Table 13   Power Dissipation PEB 3264, PEB 3264-2 (SLICOFI-2S/-2S2)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power dissipation						
Power Down both channels	P_{DDPDown}	–	79	104	mW	–
Active one channel	P_{DDAct1}	–	129	160	mW	–
Active both channels	P_{DDAct2}	–	182	243	mW	–

3.5.3   Power Dissipation of the SLIC

The SLIC power dissipation mainly comes from internal bias currents and the buffers output stage (to a less extent from the sensor) where additional power is dissipated whenever current is fed to the line.

3.5.3.1   Power Down Modes

In Power Down modes, the internal bias currents are reduced to a minimum value and no current is fed to the line (see **Table 16**, **Table 18** and **Table 20**). Even with active off-hook detection the power dissipation of 5 mW (6 mW for SLIC-P) is negligible. Note that this is the dominant factor for low mean power value in large systems, as a large percentage of lines are always inactive.

3.5.3.2   Active Mode

In Active mode, the selected battery voltage V_{BATx}[1] has the strongest influence on power dissipation. The power dissipation in the output stage P_{O} is determined by the difference between V_{BATx} and the Tip-Ring voltage $V_{\text{TIP/RING}}$. At constant DC line current I_{Trans}, the shortest lines (lowest R_{L}) cause lowest $V_{\text{TIP/RING}}$, and accordingly exhibit the highest on-chip power dissipation. However, the minimum battery voltage required is determined by the longest line and therefore the maximum line resistance $R_{\text{L,MAX}}$ and in addition R_{PROT} and R_{STAB}.

$$V_{\text{BATx,min}} = I_{\text{Trans}} \times (R_{\text{L,MAX}} + R_{\text{PROT}} + R_{\text{STAB}}) + V_{\text{AC,P}} + V_{\text{DROP}}$$

$V_{\text{AC,P}}$.....................Peak value of AC signal

V_{DROP}...................Sum of voltage drop in the SLIC buffers (**Table 14**)

---

[1] $V_{\text{BATx}} = V_{\text{BATL}}, V_{\text{BATH}}$ or V_{BATR}

Table 14   Typical Buffer Voltage Drops (Sum) for I_{TRANS} (I_T or I_R)

Mode	Total Voltage drop V_{DROP} [V]	
	SLIC-E/-E2/-S/-S2	**SLIC-P**
ACTL	$I_{TRANS} \times 96\ \Omega$	$I_{TRANS} \times 88\ \Omega$
ACTH	$I_{TRANS} \times 100\ \Omega$	$I_{TRANS} \times 100\ \Omega$
ACTR	$(I_{TRANS} \times 100\ \Omega) + 1\ V$	$I_{TRANS} \times 92\ \Omega$
ROR, ROT	–	$I_{TRANS} \times 92\ \Omega$
HIR, HIT	$(I_{T\ or\ R} \times 48\ \Omega) + 1\ V$	$I_{T\ or\ R} \times 52\ \Omega$

The most efficient way to reduce short-loop power dissipation is to use a lower battery supply voltage (V_{BATL}) whenever line resistance is small enough. This method is supported on the SLIC-E/-E2 by integrating a battery switch. With a standard battery voltage of – 48 V, long lines up to 2 kΩ can be driven at 20 mA line current.

The SLIC-P PEB 4266 "low-power" version even allows three battery voltages (typically the most negative one, e.g. – 48 V, is used in Active mode (On-hook) and Power Down mode).

DuSLIC contains two mechanism which can be used as indication for the battery switching:

1. A threshold for the voltage at Tip/Ring can be set for generating an interrupt
2. The change between constant current and resistive feeding will generate an interrupt

3.5.3.3   SLIC Power Consumption Calculation in Active Mode

A scheme of a typical calulation is shown in **Figure 31**.

Circuit Diagram

OFF-HOOK

ezm14049.emf
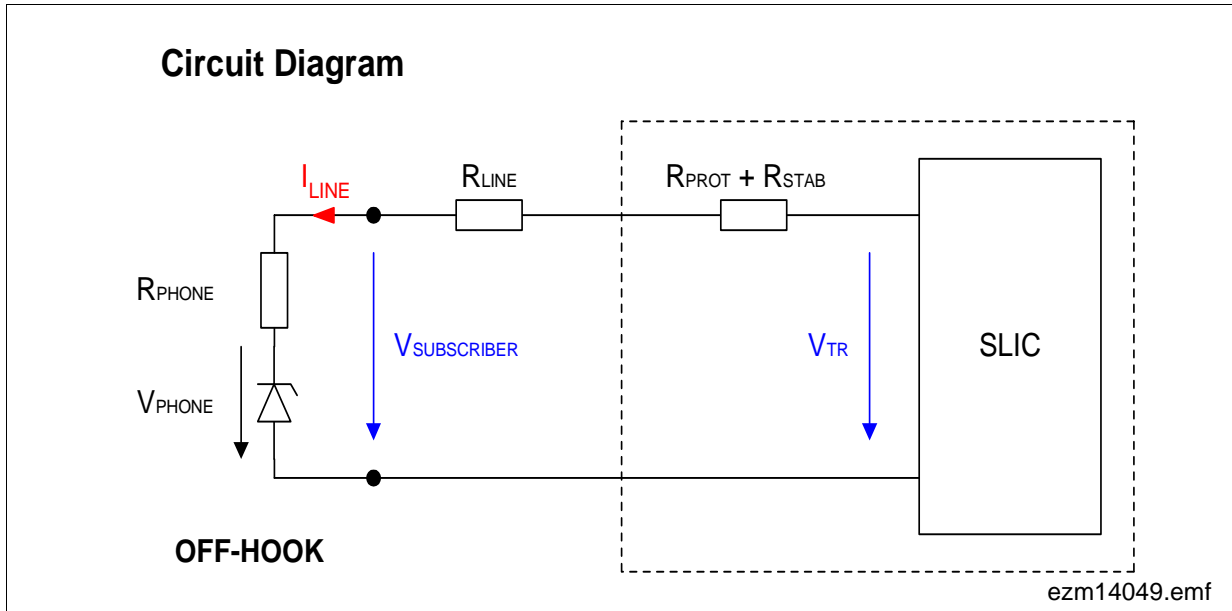
Figure 31   Circuit Diagram for Power Consumption

R_{PROT} = 40 Ω, R_{STAB} = 60 Ω, R_{PHONE} = 150 Ω, V_{PHONE} = 7 V, I_{LINE} = 20 mA
Conditions: $V_{\text{Voice peak}}$ = 2 V, $I_{\text{Voice peak}}$ = 2 mA, $V_{\text{TTX,rms}}$ (see example below)

Typical Power Consumption Calculation with SLIC-E/-E2

Assuming a typical application where the following battery voltages are used:

V_{DD} = 5 V, V_{BATL} = − 27 V, V_{BATH} = − 48 V, V_{HR} = 45 V and line feeding is guaranteed up to R_{Lmax} = 800 Ω. For longer lines (R_{L} > 800 Ω) the extended battery feeding option can be used (Mode ACTR).
Requirement for TTX: V_{TTX} = 0.6 Vrms at a load of 200 Ω.

Table 15 shows line currents and output voltages for different operating modes.

Table 15   Line Feed Conditions for Power Calculation of SLIC-E/-E2

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	–
ACTL	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 16 V
ACTH	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 24 V

With the line feed conditions given in the above table the total power consumption P_{TOT} and its shares at different operating modes are shown in **Table 16**.
The output voltage at Tip and Ring is calculated for a typical line length (R_L = 3/4*R_{Lmax} in ACTH, R_L = 1/4*R_{Lmax} in ACTL).

Table 16   SLIC-E/-E2 Typical Total Power Dissipation

	P_Q[1]	P_I	P_G	P_O	P_{TOT}
Operating Mode	[mW]	[mW]	[mW]	[mW]	**[mW]**
PDH	3.7	0	0	0	**3.7**
PDRH	4.4	0	0	0	**4.4**
ACTL	81.8	33.7	3.3	220	**339**
ACTH	173	56.8	0	480	**710**

[1] The formulas for the calculation of the power shares P_Q, P_I, P_G and P_O can be found in the DuSLIC Data Sheet.

Figure 32 shows the total power dissipation P_{TOT} of the SLIC-E/-E2 in Active Mode (ACTH and ACTL) with switched battery voltage (V_{BATH}, V_{BATL}) as a function of R_{Line}. The power dissipation in the SLIC is strongly reduced for short lines.
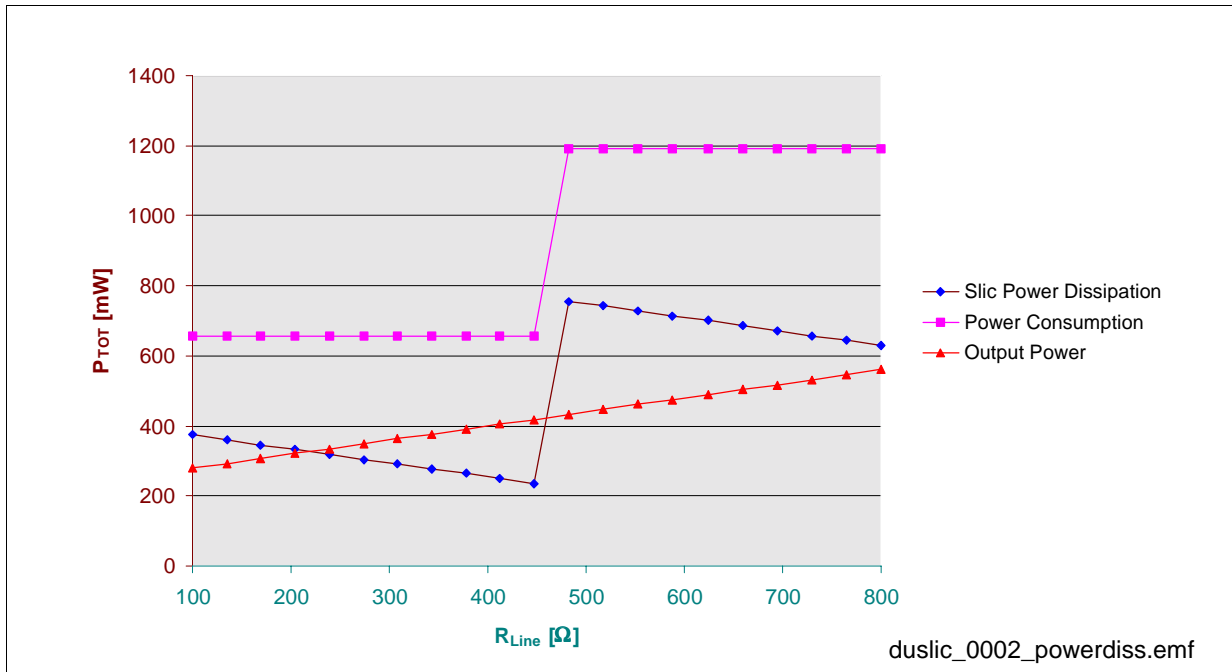
Figure 32   **SLIC-E/-E2 Power Dissipation with switched Battery Voltage**

Typical Power Consumption Calculation with SLIC-P (Internal Ringing)

Assuming a typical application where the following battery voltages are used:

V_{DD} = 3.3 V, V_{BATL} = − 22 V, V_{BATH} = − 48 V, V_{BATR} = − 80 V and a maximum line length of up to R_{Lmax}= 400 Ω is used.

Requirement for TTX: V_{TTX} = 0.4 Vrms at a load of 200 Ω.

Table 17 shows line currents and output voltages for different operating modes.

Table 17   **Line Feed Conditions for Power Calculation for SLIC-P**

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	–
ACTL	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 14 V
ACTH	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 18 V

With the line feed conditions given in the above table, the total power consumption P_{TOT} and its shares at different operating modes are shown in **Table 18**.
The output voltage at Tip and Ring is calculated for typical line length (R_L = 3/4*R_{Lmax} in ACTH, R_L = 1/4*R_{Lmax} in ACTL).

Table 18   SLIC-P PEB 4266 Power Dissipation

	P_Q[1]	P_I	P_G	P_O	P_{TOT}
Operating Mode	[mW]	[mW]	[mW]	[mW]	**[mW]**
PDH	6.4	0	0	0	**6.4**
PDRH	6.4	0	0	0	**6.4**
PDRR	7.7	0	0	0	**7.7**
ACTL	50.5	26.8	− 2	160	**235**
ACTH	133.4	55.4	0	600	**789**
ROR, ROT (Ring Pause)	194.6	0	− 20	0	**175**

[1] The formulas for the calculation of the power shares P_Q, P_I, P_G and P_O can be found in the DuSLIC Data Sheet.

Figure 34 shows the total power dissipation PTOT of the SLIC-P in Active mode (ACTH and ACTL) with switched battery voltage (V_{BATH}, V_{BATL}) as a function of R_{Line}.
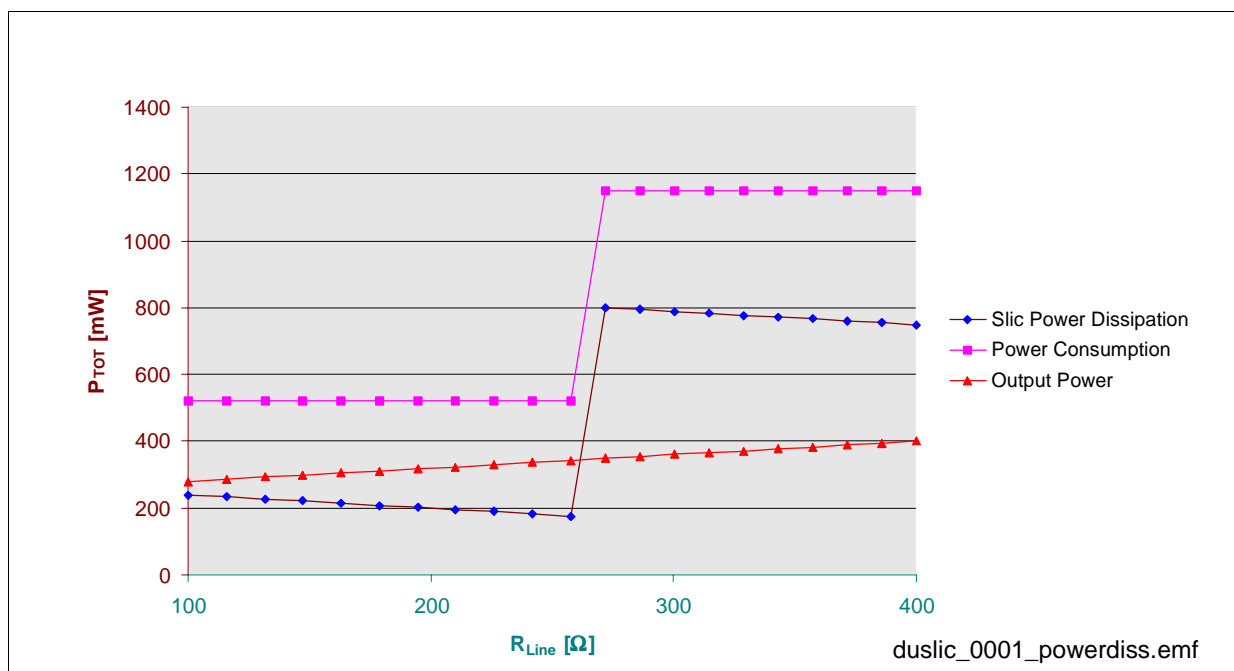

Figure 33   SLIC-P Power Dissipation (Switched Battery Voltage, Long Loops)

Typical Power Consumption Calculation with SLIC-P (External Ringing)

Assuming a typical application where the following battery voltages are used:

V_{DD} = 3.3 V, V_{BATL} = − 22 V, V_{BATH} = − 26 V, V_{BATR} = − 48 V and line feeding is guaran-teed up to R_L = 400 Ω.

Requirement for TTX: $V_{TTX,rms}$ = 0.4 Vrms.

This is a typical lowest-power application, where V_{BATR} is used just in the On-hook state and V_{BATH} and V_{BATL} is used in the active modes with battery switching.

Table 19 shows line currents and output voltages for different operating modes.

Table 19   Line Feed Conditions for Power Calculation for SLIC-P

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	–
ACTL	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 14 V
ACTH	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 18 V

With the line feed conditions given in the above table, the total power consumption P_{TOT} and its shares at different operating modes are shown in **Table 20**.

The output voltage at Tip and Ring is calculated for a typical line length (R_L = 3/4*R_{Lmax} in ACTH, R_L = 1/4*R_{Lmax} in ACTL).

Table 20   SLIC-P PEB 4266 Power Dissipation

	P_Q[1]	P_I	P_G	P_O	P_{TOT}
Operating Mode	[mW]	[mW]	[mW]	[mW]	**[mW]**
PDH	4.0	0	0	0	**4.0**
PDRH	3.9	0	0	0	**3.9**
PDRR	4.8	0	0	0	**4.8**
ACTL	49.9	26.8	− 2	160	**235**
ACTH	73.7	31.2	− 34.7	160	**230**

[1] The formulas for the calculation of the power shares P_Q, P_I, P_G and P_O can be found in the DuSLIC Data Sheet.

Figure 34 shows the total power dissipation P_{TOT} of the SLIC-P in Active mode (ACTH and ACTL) with switched battery voltage (V_{BATH}, V_{BATL}) as a function of R_{Line} (Lowest Power Applications).
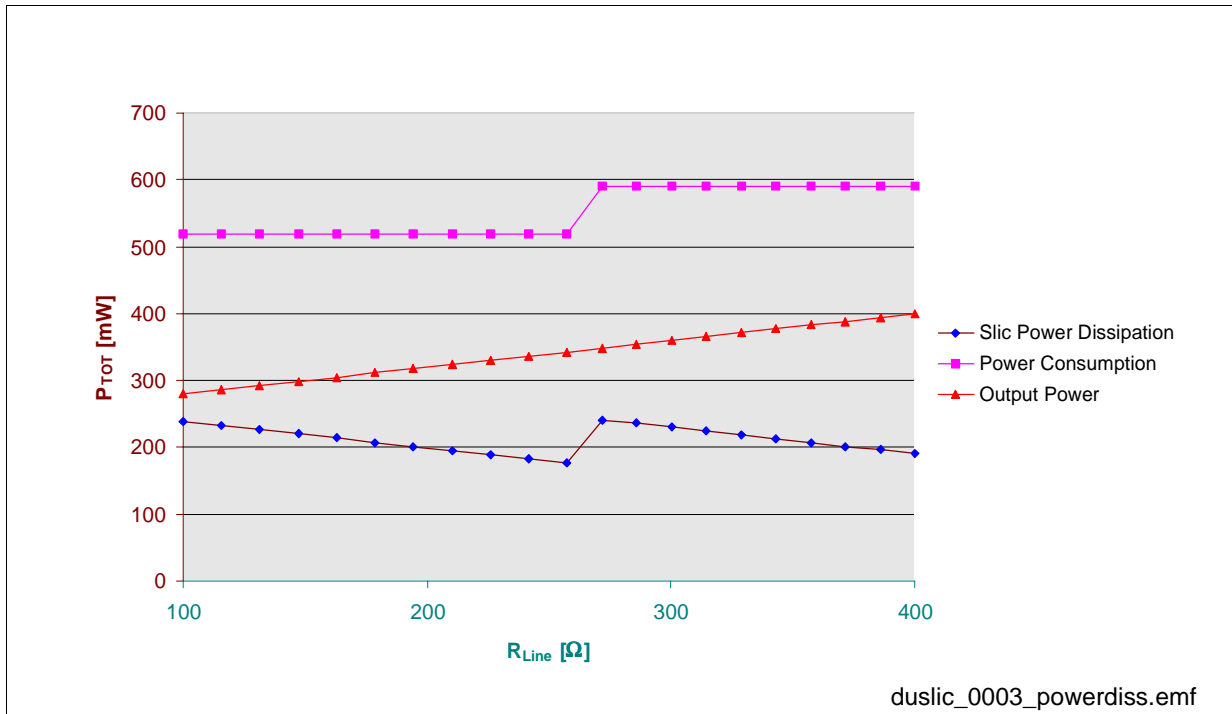
Figure 34   SLIC-P Power Dissipation (Switched Battery Voltage, Short Loops)

3.5.3.4   Ringing Modes

Internal Balanced Ringing (SLIC-E and SLIC-P)

The SLIC-E/-E2/-P internal balanced ringing facility requires a higher supply voltage (auxiliary voltage V_{HR}). The highest share of the total power is dissipated in the output stage of the SLIC-E/-E2/-P. The output stage power dissipation P_O (see **Table 21**, **Table 22**) depends on the ring amplitude ($V_{RNG,PEAK}$), the equivalent ringer load (R_{RNG} and C_{RNG}), the ring frequency (via $\cos\phi_L$) and the line length (R_L).

The minimum auxiliary voltage V_{HR} necessary for a required ring amplitude can be calculated using:

$$V_{HR} - V_{BATH} = V_{RNG,PEAK} + V_{RNG,DC} + V_{DROP} = V_{RNG,RMS} \times \text{crest factor} + V_{RNG,DC} + V_{DROP}$$

The crest factor is defined as peak value divided by RMS value (here always 1.41 because sinusoidal ringing is assumed).

$V_{RNG,DC}$ Superimposed DC voltage for Ring trip detection (10 to 20 V)

V_{DROP} Sum of voltage drops in SLIC buffers (**Table 14**)

$V_{RNG,PEAK}$ Peak ring voltage at Tip/Ring

The strong influence of the ringer load impedance Z_{LD} and the number of ringers is demonstrated by the formula for the current sensor power dissipation ($P_I + P_O$) in **Table 21** and **Table 22**.

The ringer load impedance Z_{LD} can be calculated as follows:

$$Z_{LD} = |Z_{LD}| \times e^{j\phi LD} = R_L + R_{RNG} + 1/j\omega C_{RNG} \text{ with}$$

Z_{LD}	Load impedance
R_{RNG}	Ringer resistance
C_{RNG}	Ringer capacitance
R_L	Line resistance

Internal Unbalanced Ringing with SLIC-P

The ring signal is present just on one line (modes ROR, ROT), while the other line is connected to a potential of GND.

The minimum battery voltage V_{BATR} necessary for a required ring amplitude can be calculated using:

$$- V_{BATR} - V_{DROP} = 2 \times V_{RNG, PEAK} = 2 \times V_{RNG,RMS} \times \text{crest factor}$$

External Ringing (SLIC-E/-E2 and SLIC-P)

When an external ring generator and ring relays are used, the SLIC can be switched to Power Down mode.

The "low-power" SLIC-P is optimized for extremely power-sensitive applications (see **Table 20**). SLIC-P has three different battery voltages. V_{BATR} can be used for on-hook, while V_{BATH} and V_{BATL} are normally used for off-hook mode.

3.5.3.5   SLIC Power Consumption Calculation in Ringing Mode

The average power consumption for a ringing cadence of 1 second on and 4 seconds off is given by

$$P_{\text{TOT, average}} = k \times P_{\text{TOT, Ringing}} + (1 - k) \times P_{\text{TOT, RingPause}}$$

with k = 0.20

The typical circuit for ringing is shown in **Figure 35**.
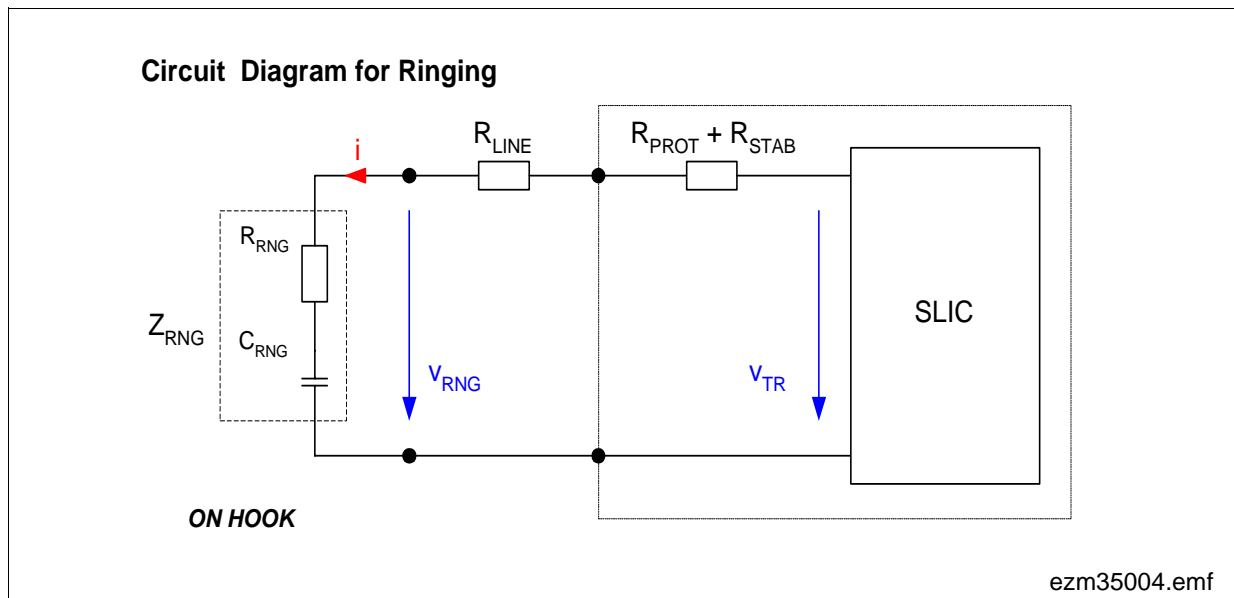

Figure 35   Circuit Diagram for Ringing

– Power Consumption Calculation for SLIC-E/-E2 in Balanced Ringing Mode

With the example of the above calculation for SLIC-E/-E2 (see **Chapter 3.5.3.3**) and a typical ringer load.

Typical ringer load: R_{RNG} = 450 Ω, C_{RNG} = 3.4 µF
Required ringing voltage V_{RNG} = 45 Vrms and ringing frequency f_{RNG} = 20 Hz
DC Offset Voltage for ring trip detection V_{DC} = 16 V.

Table 21 shows the power calculation for the total power dissipation P_{TOT} of the SLIC-E/SLIC-E2 in balanced ringing mode consisting of the quiescent power dissipation P_Q, the current sensor power dissipation P_I, the gain stage power dissipation P_G and the output stage power dissipation P_O.

Table 21   SLIC-E/-E2 Balanced Ringing Power Dissipation (typical)

$P_{TOT, RingPause}$ = P_Q + P_I + P_G + P_O (I_{Trans} = 0 mA)	**458 mW**
$P_{TOT, Ringing}$ = P_Q + P_I + P_G + P_O	**1526 mW**[1]
P_Q = $V_{DD} \times I_{DD}$ + $|V_{BATH}| \times I_{BATH}$ + $|V_{BATL}| \times I_{BATL}$ + $V_{HR} \times I_{HR}$	254 mW
P_I = $0.015 \times I_{Trans,rms} \times V_{HR}$ + $0.055 \times I_{Trans,rms} \times |V_{BATH}|$ + $0.04 \times I_{Trans,rms} \times V_{DD}$ with $I_{Trans,rms}$ = $V_{TIP/RING, rms}/|Z_{LD}|$	67 mW
P_G = $(V_{HR} + |V_{BATH}|) \times ($SQRT$((V_{HR} + V_{BATH} + V_{DC\text{-}offset})^2 + (V_{TIP/RING}^2)/2) - |V_{HR} + V_{BATH}|)/60k$ + $(V_{HR2} - 322 + V_{BATH}^2 - 48^2) \times (1/60k + 1/216k)$	99 mW
P_O = $(V_{HR} + |V_{BATH}|) \times I_{Trans,rms} \times 2 \times$ SQRT$(2)/\pi$ – $V_{TIP/RING, rms} \times I_{Trans,rms} \times \cos(\phi_{Load})$	1105 mW

[1] Values for V_{DD} = 5 V, V_{BATL} = – 27 V, V_{BATH} = – 48 V, V_{HR} = 45 V, T_J = 25 °C

– Power Consumption Calculation for SLIC-P in Balanced Ringing Mode

With the example of the above calculation with R_L = 400 Ω line length for SLIC-P (see **Chapter 3.5.3.3**) when the internal ringing feature will be used.

Typical ringer load: R_{RNG} = 1000 Ω, C_{RNG} = 3.7 μF.
Required ringing voltage V_{RNG} = 40 Vrms and ringing frequency f_{RNG} = 20 Hz.
DC Offset voltage for ring trip detection V_{DC} = 14 V.

Table 22 shows the power calculation for the total power dissipation P_{TOT} of the SLIC-P in balanced ringing mode consisting of the quiescent power dissipation P_Q, the current sensor power dissipation P_I, the gain stage power dissipation P_G and the output stage power dissipation P_O.

Table 22   SLIC-P Balanced Ringing Power Dissipation (typical)

$P_{TOT, RingPause} = P_Q + P_I + P_G + P_O$ (I_{Trans} = 0 mA)	**283 mW**
$P_{TOT, Ringing} = P_Q + P_I + P_G + P_O$	**1137 mW[1]**
$P_Q = V_{DD} \times I_{DD} + \|V_{BATR}\| \times I_{BATR} + \|V_{BATH}\| \times I_{BATH} + \|V_{BATL}\| \times I_{BATL}$	281 mW
$P_I = 0.055 \times I_{Trans,rms} \times \|V_{BATR}\| + 0.04 \times I_{Trans,rms} \times V_{DD}$ with $I_{Trans,rms} = V_{TIP/RING, rms}/\|Z_{LD}\|$	76 mW
$P_G = (V_{BATR}^2 - 80^2) \times (1/60k + 1/216k)$	– 1.6 mW
$P_O = \|V_{BATR}\| \times I_{Trans,rms} \times 2 \times SQRT(2)/\pi - V_{TIP/RING, rms} \times I_{Trans,rms} \times \cos(\phi_{Load})$	781 mW

[1] Values for V_{DD} = 3.3 V, V_{BATL} = – 22 V, V_{BATH} = – 48 V, V_{BATR} = – 80 V, T_J = 25 °C

– Power Consumption Calculation for SLIC-P in Unbalanced Ringing Mode

A similar power calculation is valid for internal unbalanced ringing mode, which is only available for the SLIC-P.

Example:

V_{DD} = 3.3 V, V_{BATL} = − 22 V, V_{BATH} = − 48 V, V_{BATR} = − 128 V and line feeding is guaranteed up to 400 Ω.
Typical ringer load: R_{RNG} = 1000 Ω, C_{RNG} = 3.7 μF
Required ringing voltage V_{RNG} = 40 Vrms and ringing frequency f_{RNG} = 20 Hz.

Table 23 shows the power calculation for the total power dissipation P_{TOT} of the SLIC-P in unbalanced ringing mode.

Note: For further power reduction in unbalanced ringing mode see the Application Note "DuSLIC Ringing Modes" (chapter 5: "Integrated Unbalanced Ringing with Reduced Power Dissipation Using SLIC-P")

Table 23   SLIC-P Unbalanced Ringing Power Dissipation (typical)

$P_{\text{TOT, RingPause}} = P_Q + P_I + P_G + P_O$ (I_{Trans} = 0 mA)	**530 mW**
$P_{\text{TOT, Ringing}} = P_Q + P_I + P_G + P_O$	**2125 mW[1]**
$P_Q = V_{DD} \times I_{DD} + |V_{BATR}| \times I_{BATR} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL}$	310 mW
$P_I = 0.055 \times I_{\text{Trans,rms}} \times |V_{BATR}| + 0.04 \times I_{\text{Trans,rms}} \times V_{DD}$ with $I_{\text{Trans,rms}} = V_{\text{TIP/RING, rms}}/|Z_{LD}|$	121 mW
$P_G = (0.5 \times V_{\text{TIP/RING}}^2 - (V_{BATR}/2)^2)/60k + (V_{BATR}^2 - 80^2) \times$ (1/60k + 1/216k)	177 mW
$P_O = |V_{BATR}| \times I_{\text{Trans,rms}} \times 2 \times \text{SQRT}(2)/\pi - V_{\text{TIP/RING, rms}} \times I_{\text{Trans,rms}} \times \cos(\phi_{\text{Load}})$	1518 mW

[1] Values for V_{DD} = 3.3 V, V_{BATL} = − 22 V, V_{BATH} = − 48 V, V_{BATR} = − 128 V, T_J = 25 °C

3.6 Integrated Test and Diagnosis Functions (ITDF)[1]

3.6.1 Introduction

Subscriber loops are affected by a variety of failures which have to be monitored. Monitoring the loop supposes the access to the subscriber loop and to have test equipment in place which are capable to perform certain measurements. The measurements or tests involve resistance, capacitance, leakage, and measurements of interfering currents and voltages.

3.6.2 Conventional Line Testing

Conventional linecards in Central Office (CO) applications usually need two test relays per channel to access the subscriber loop with the appropriate test equipment. One relay (test-out) connects the actual test unit to the local loop. All required line tests can be accomplished that way. The second relay (test-in) separates the local loop from the SLIC-E/-E2/-P and connects a termination impedance to it. Hence, by sending a tone signal the entire loop can be checked, including the SLICOFI-2 and SLIC-E/-E2/-P.

With an external test unit, every line has to be connected separately to the test unit and the tests have to be performed one line at a time. Testing thousands of lines takes several hours. Because of the time factor, these tests are typically carried out once a week or once a month. The test cycle for a specific subscriber line is therefore very long and any failures are usually detected at a very late stage. This reduces the network quality.

3.6.3 DuSLIC Line Testing

The DuSLIC with its Integrated Test and Diagnosis Functions (ITDF) is capable to perform all tests necessary to monitor the local loop without an external test unit and test relays. The fact, that measurements can be accomplished much faster as with conventional test capabilities makes it even more a compelling argument for the DuSLIC. With the DuSLIC both channels are able to perform line tests concurrently, which also has a tremendous impact on the test time. All in all, the DuSLIC increases the quality of service and reduces the costs in various applications.

---

[1] only available with DuSLIC-E/-E2/-P

3.6.4 Diagnostics

The two-channel chip set has a set of signal generators and features implemented to accomplish a variety of diagnostic functions. The SLICOFI-2 device generates all test signals, processes the information that comes back from the SLIC-E/-E2/-P and provides the data to a higher level master device, e.g. a microprocessor. All the tests can be initiated by the micropocessor and the results can be read back very easily. The Integrated Test and Diagnosis Functions (ITDF) might prevent any problem which affects service caused by the subscriber line or line equipment before the customer complains. IDTF has been integrated to facilitate the monitoring of the subscriber loop.

3.6.4.1 Line Test Capabilities

The line test comprises the following functions:

- Loop resistance measurement:
  The DC loop resistance can be determined by supplying a constant DC voltage $V_{TR,DC}$ to the Ring- and Tip line and measuring the DC loop current via the IT pin.
- Leakage current:
  – Leakage current Tip/Ring
  – Leakage current Tip/GND
  – Leakage current Ring/GND
- Ringer / Line capacitance:
  Capacitance measurements can be performed by using the integrated ramp generator function. Loading a capacitor $C_{Measure}$ with a constant voltage ramp results in a constant current which is proportional to $C_{Measure.}$
  – Line capacitance Tip/GND
  – Line capacitance Ring/GND
- Foreign voltage measurement:
  Two analog input pins (IO3, IO4) can be used for direct and differential measurement of two external voltages.
  – Foreign voltage measurement Tip/GND
  – Foreign voltage measurement Ring/GND
  – Foreign voltage measurement Tip/Ring
- Measurement of ringing voltage
- Measurement of line feed current
- Measurement of supply voltage V_{DD} of the SLICOFI-2
- Measurement of transversal- and longitudinal current

3.6.4.2 Integrated Signal Sources

The signal sources available on the DuSLIC chip set are:

- Constant DC voltage (three programmable ringing DC offset voltages)
- 2 independent tone generators TG1 and TG2:
- TTX metering signal generator (12/16 kHz)
- Ramp generator (used for capacitance measurements)
- Ring generator (5 Hz - 300 Hz)

3.6.4.3 DC Levelmeter

The DC levelmeter results will be determined and prepared depending on certain configuration settings. The selected input signal becomes digitized after pre-filtering and analog-to-digital conversion.

The following values can be measured:

DC Levelmeter Measurement Values:
DC out voltage on DCP-DCN
DC current on IT
DC current on IL
Voltage on IO3
Voltage on IO4
V_{DD}
Offset of DC-pre-filter (short circuit on DC-pre-filter input)
Voltage on IO4 – IO3

3.6.4.4 AC Levelmeter

The AC levelmeter allows access to the voice signal while the active voice signal is being processed. The input signal for the AC levelmeter might get processed with a programmable filter characteristic, i.e. bandpass- or notch filter.

The following values can be measured:

AC Levelmeter Measurement Values:
AC level in transmit
AC level in receive
AC level receive + transmit

3.6.5 Signal Path and Test Loops

The following figures show the main AC and DC signal path and the integrated analog and digital loops of SLICOFI-2, SLICOFI-2S and SLICOFI-2S2.

Please note the interconnections between the AC and DC pictures of the respective chip set. For further information on the shown registers and bits/switches please see the DuSLIC Data Sheet.
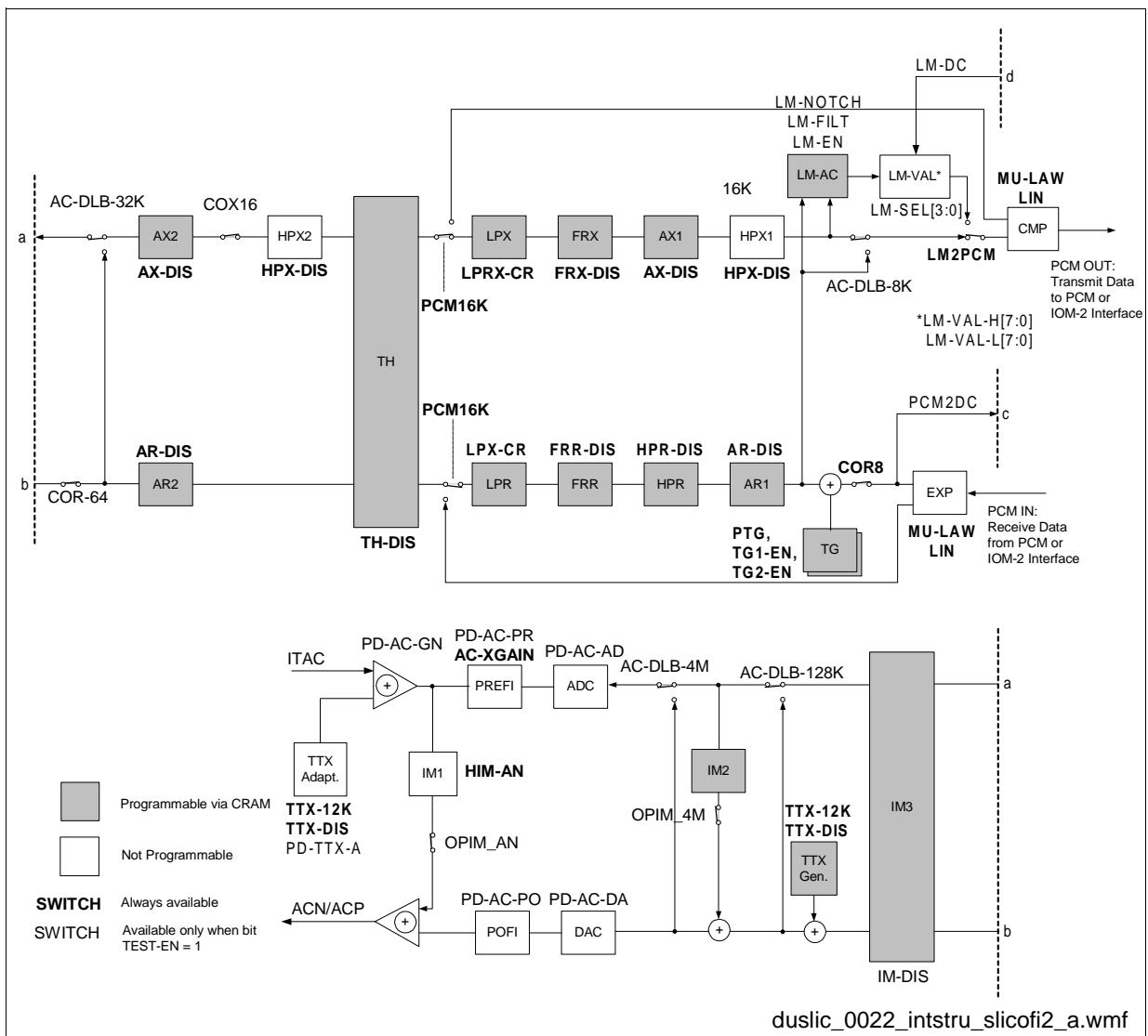
3.6.5.1 Test Loops SLICOFI-2
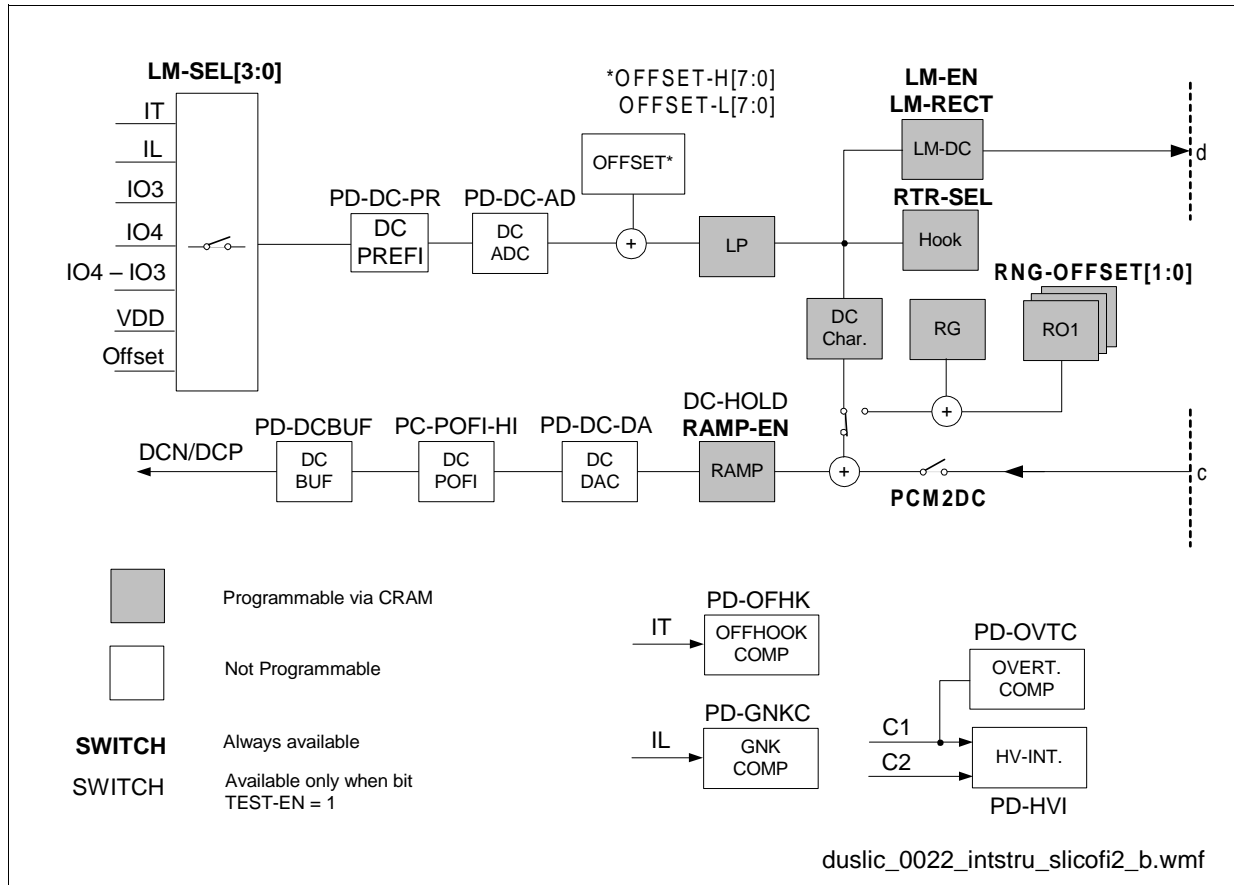

Figure 36   AC Test Loops SLICOFI-2

Figure 37   DC Test Loops SLICOFI-2

3.6.5.2 Test Loops SLICOFI-2S/-2S2

The AC test loops for SLICOFI-2S (**Figure 38**) and SLICOFI-2S2 (**Figure 39**) are different since Teletax (TTX) is not available with SLICOFI-2S2. The DC test loops are identical.
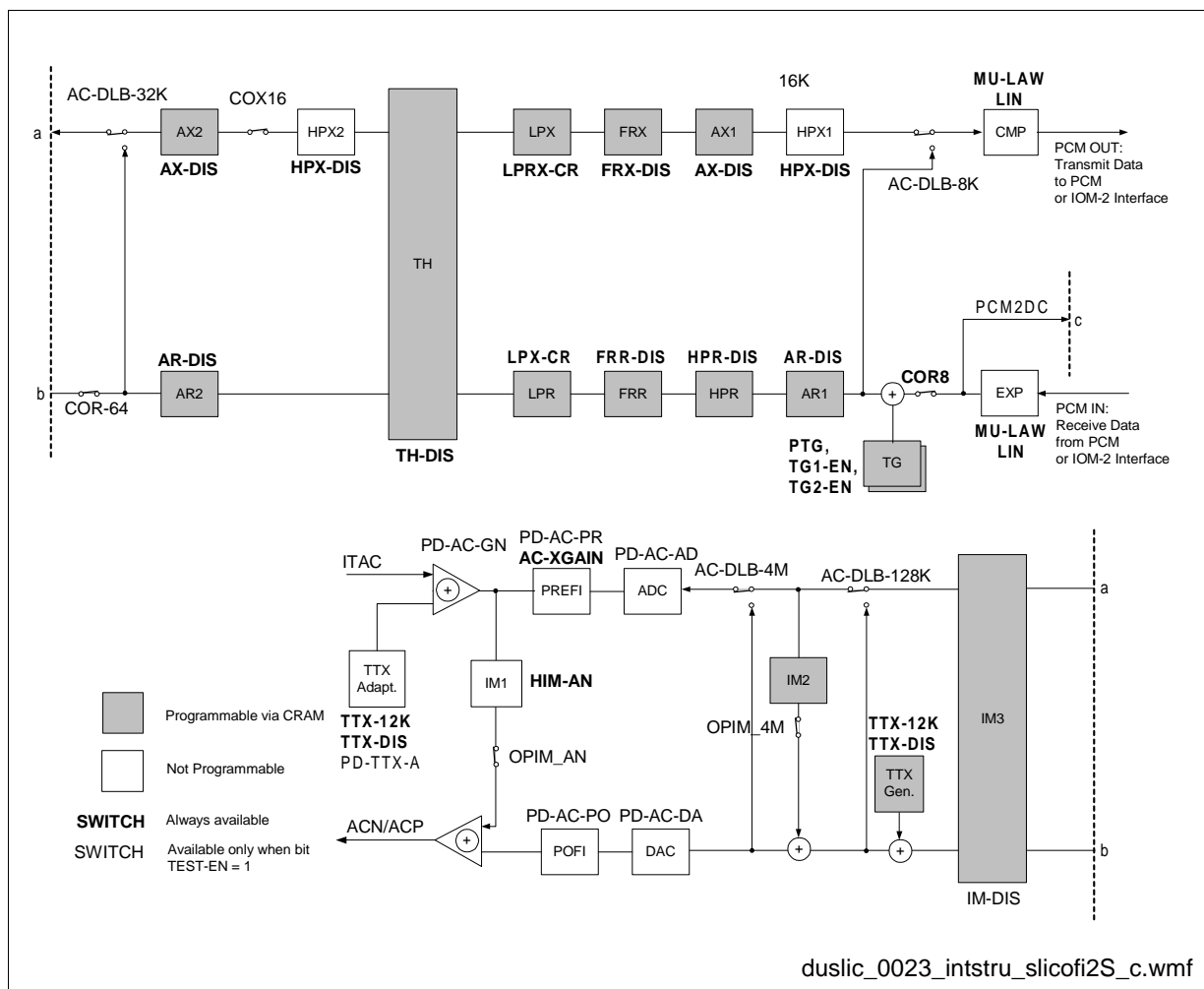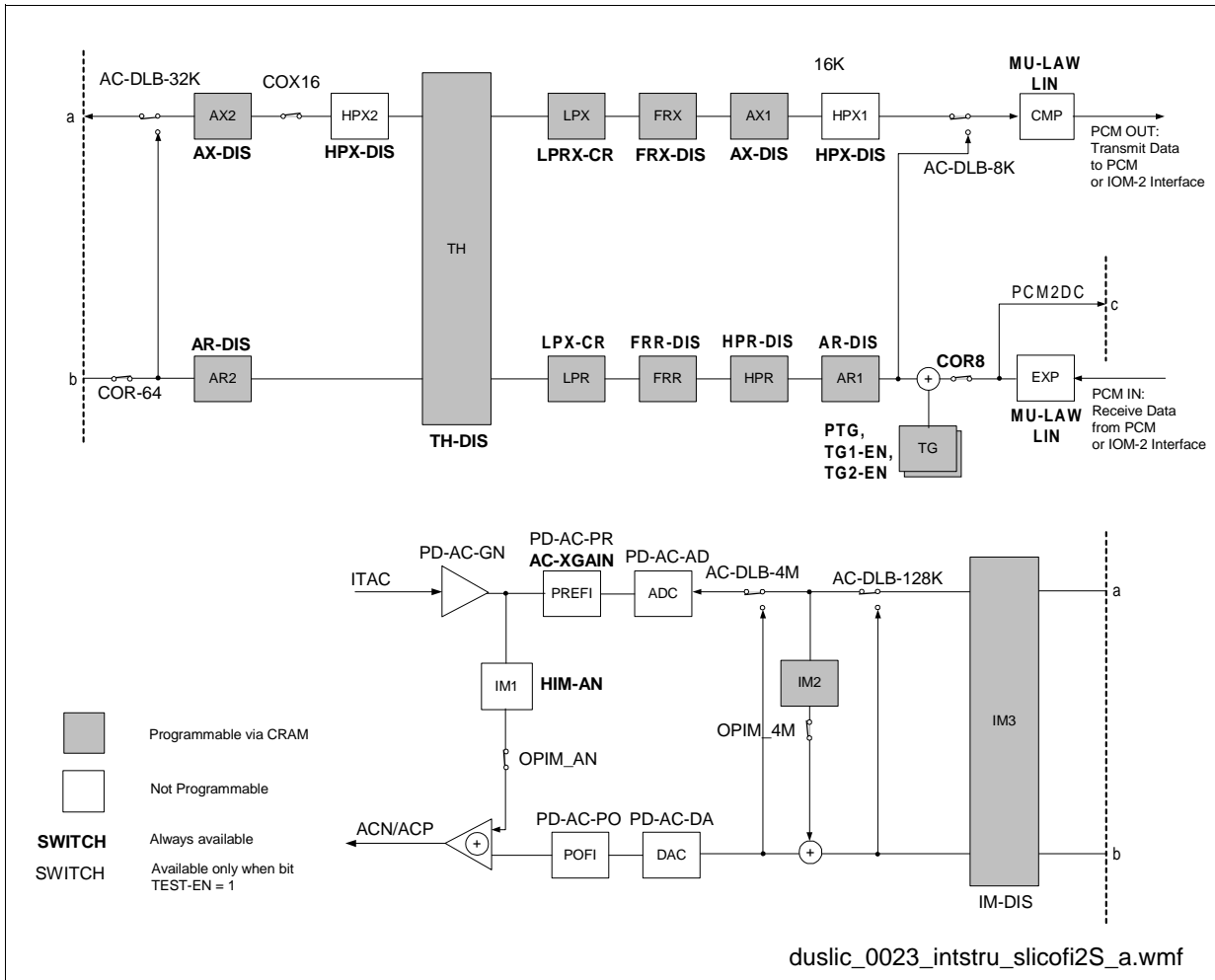

Figure 38   AC Test Loops SLICOFI-2S

Figure 39   AC Test Loops SLICOFI-2S2

Figure 40   DC Test Loops SLICOFI-2S/-2S2

4 Interfaces

The DuSLIC connects the analog subscriber to the digital switching network by two different types of digital interfaces to allow for the highest degree of flexibility in different applications:

• PCM interface combined with a serial microcontroller interface
• IOM-2 interface.

The PCM/$\overline{\text{IOM-2}}$ pin selects the interface mode.

PCM/$\overline{\text{IOM-2}}$ = 0: The IOM-2 interface is selected.
PCM/$\overline{\text{IOM-2}}$ = 1: The PCM/µC interface is selected.

The analog TIP/RING interface connects the DuSLIC to the subscriber.

4.1 PCM Interface with a Serial Microcontroller Interface

In PCM/µC interface mode, voice and control data are separated and handled by different pins of the *SLICOFI-2x*. Voice data are transferred via the PCM highways while control data are using the microcontroller interface.

4.1.1 PCM Interface

The serial PCM interface is used to transfer A-law or µ-law-compressed voice data. In test mode, the PCM interface can also transfer linear data. The eight pins of the PCM interface are used as follows (two PCM highways):

PCLK: PCM Clock, 128 kHz to 8192 kHz

FSC: Frame Synchronization Clock, 8 kHz

DRA: Receive Data Input for PCM Highway A

DRB: Receive Data Input for PCM Highway B

DXA: Transmit Data Output for PCM Highway A

DXB: Transmit Data Output for PCM Highway B

$\overline{\text{TCA}}$:   Transmit Control Output for PCM Highway A, Active low during transmission

$\overline{\text{TCB}}$:   Transmit Control Output for PCM Highway B, Active low during transmission

The FSC pulse identifies the beginning of a receive and transmit frame for both channels. The PCLK clock signal synchronizes the data transfer on the DXA (DXB) and DRA (DRB) lines. On all channels, bytes are serialized with MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to buffer the contents of the received data on DRA (DRB).

If double clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to buffer the contents of the data line DRA (DRB).
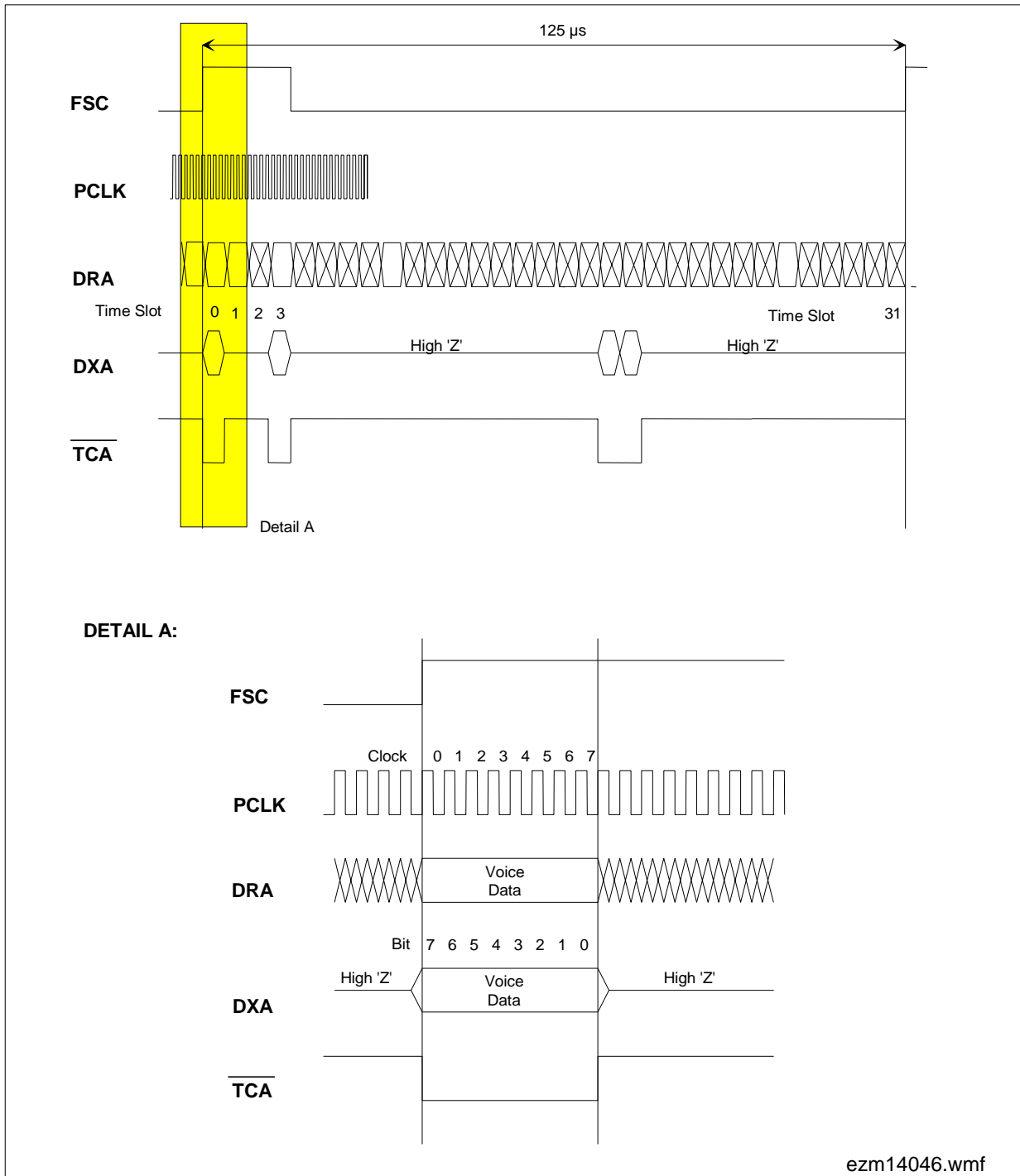

Figure 41   General PCM Interface Timing

The data rate of the interface can vary from 2×128 kbit/s to 2×8192 kbit/s (two highways). A frame may consist of up to 128 time slots of 8 bits each. The time slot and PCM highway assignment for each DuSLIC channel can be programmed. Receive and transmit time slots can also be programmed individually.

When DuSLIC is transmitting data on DXA (DXB), pin $\overline{\text{TCA}}$ ($\overline{\text{TCB}}$) is activated to control an external driving device.

The DRA/B and DXA/B pins may be connected to form a bidirectional data pin for special purposes, e.g., for the Serial Interface Port (SIP) with the Subscriber Line Data (SLD) bus. The SLD approach provides a common interface for analog or digital per-line components. For more details, please see the "ICs for Communications"[1] User's Manual available from Infineon Technologies on request.

Table 24 shows PCM interface examples; other frequencies (e.g., 1536 kHz) are also possible.

Table 24   *SLICOFI-2x* PCM Interface Configuration

Clock Rate PCLK [kHz]	Single/Double Clock [1/2]	Time Slots [per highway]	Data Rate [kbit/s per highway]
128	1	2	128
256	2	2	128
256	1	4	256
512	2	4	256
512	1	8	512
768	2	6	384
768	1	12	768
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
f	1	f/64	f

---

[1] Ordering No. B115-H6377-X-X-7600, published by Infineon Technologies.

Table 24 *SLICOFI-2x* **PCM Interface Configuration**

f	2	f/128	f/2

Valid PCLK clock rates are: f = n × 64 kHz (2 ≤ n ≤ 128)

4.1.2 Serial Microcontroller Interface

The microcontroller interface consists of four lines: $\overline{CS}$, DCLK, DIN and DOUT.

$\overline{CS}$ A synchronization signal starting a read or write access to *SLICOFI-2x*.

DCLK   A clock signal (up to 8.192 MHz) supplied to *SLICOFI-2x*.

DIN   Data input carries data from the master device to the *SLICOFI-2x*.

DOUT   Data output carries data from *SLICOFI-2x* to a master device.

There are two different command types. Reset commands have just one byte. Read/write commands have two command bytes with the address offset information located in the second byte.

A write command consists of two command bytes and the following data bytes. The first command byte determines whether the command is read or write, how the command field is to be used, and which DuSLIC channel (A or B) is written. The second command byte contains the address offset.

A read command consists of two command bytes written to DIN. After the second command byte is applied to DIN, a dump-byte consisting of '1's is written to DOUT. Data transfer starts with the first byte following the 'dump-byte'.
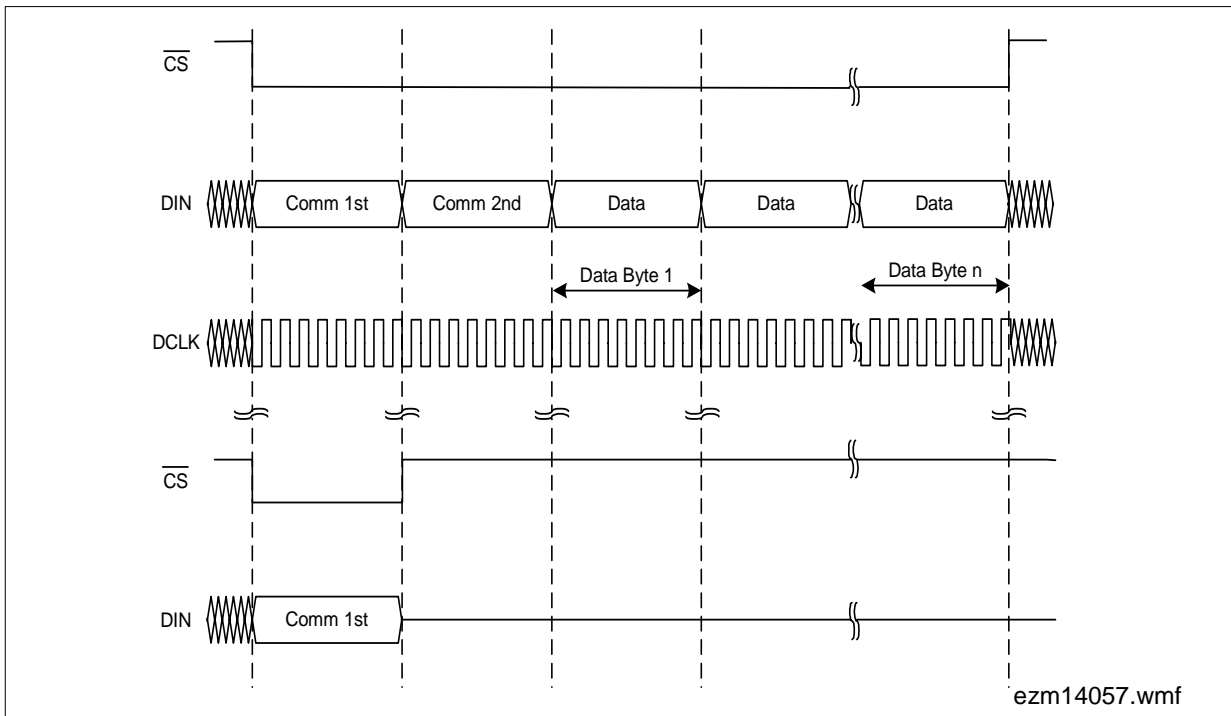
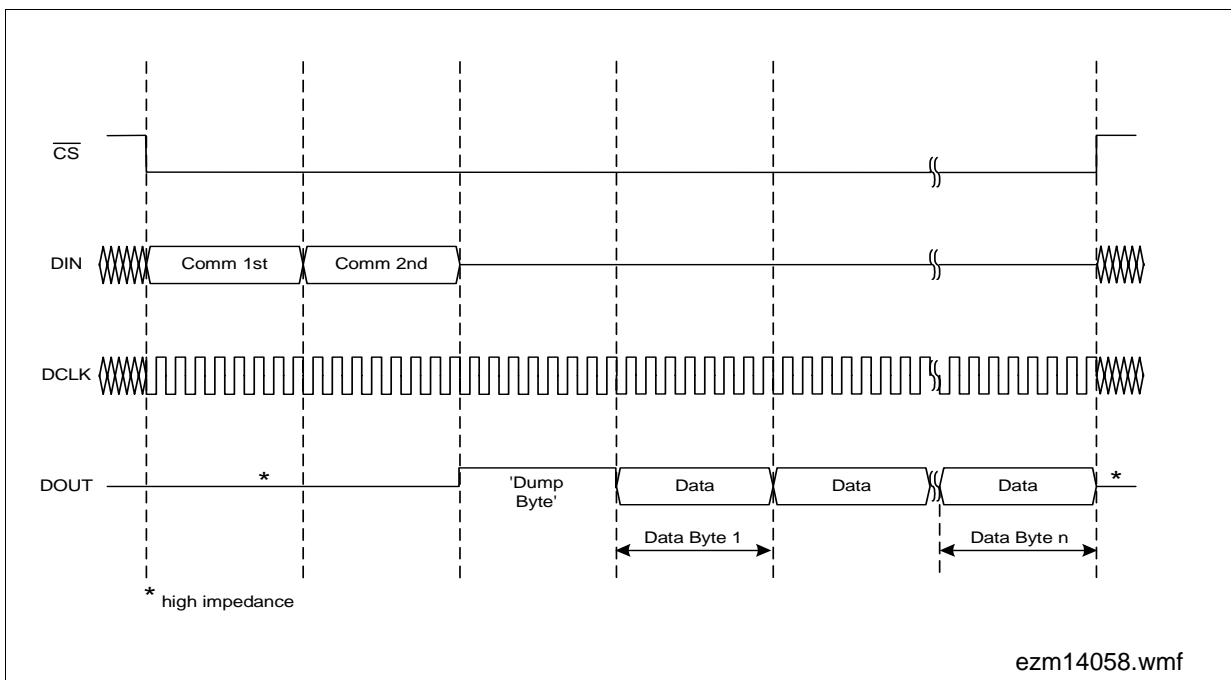**Figure 42   Serial Microcontroller Interface Write Access[1]**

Figure 43   Serial Microcontroller Interface Read Access

---

[1] for n data bytes and single byte command

Programming the Microcontroller Interface Without Clocks at FSC, MCLK, PCLK

The *SLICOFI-2x* can also be programmed via the µC interface without any clocks connected to the FSC, MCLK, PCLK pins. This can be useful in Power Down modes when further power saving on system level is necessary. In this case a data clock of up to 1.024 MHz can be used on pin DCLK.

Since the *SLICOFI-2x* will leave the basic reset routine only if clocks at the FSC, MCLK and PCLK pins are applied, it is not possible to program the *SLICOFI-2x* without any clocks at these pins directly after the hardware reset or power on reset.

4.2 The IOM-2 Interface

IOM-2 defines an industry-standard serial bus for interconnecting telecommunication ICs for a broad range of applications - typically ISDN-based applications.

The IOM-2 bus provides a symmetrical full-duplex communication link containing data, control/programming and status channels. Providing data, control and status information via a serial channel reduces pin count and cost by simplifying the line card layout.

The IOM-2 Interface consists of two data lines and two clock lines as follows:

DU: Data Upstream carries data from the *SLICOFI-2x* to a master device.

DD: Data Downstream carries data from the master device to the *SLICOFI-2x*.

FSC: A Frame Synchronization Signal (8 kHz) supplied to *SLICOFI-2x*.

DCL: A Data Clock Signal (2048 kHz or 4096 kHz) supplied to *SLICOFI-2x*.

SLICOFI-2x handles data as described in the IOM-2 specification[1] for analog devices.
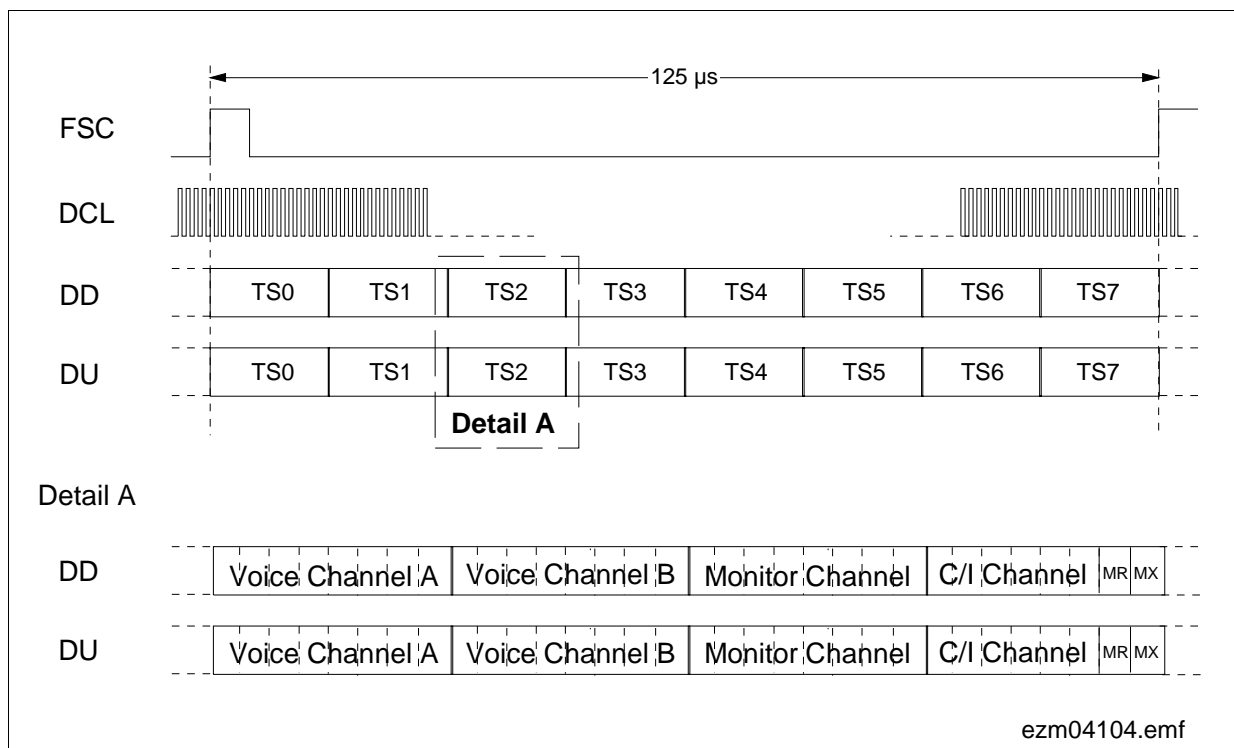

Figure 44   IOM-2 Int. Timing for up to 16 Voice Channels (Per 8 kHz Frame)

[1] Available on request from Infineon Technologies.

The information is multiplexed into frames, which are transmitted at an 8-kHz rate. The frames are subdivided into 8 sub-frames, with one sub-frame dedicated to each transceiver or pair of codecs (in this case, two *SLICOFI-2x* channels). The sub-frames provide channels for data, programming and status information for a single transceiver or codec pair.
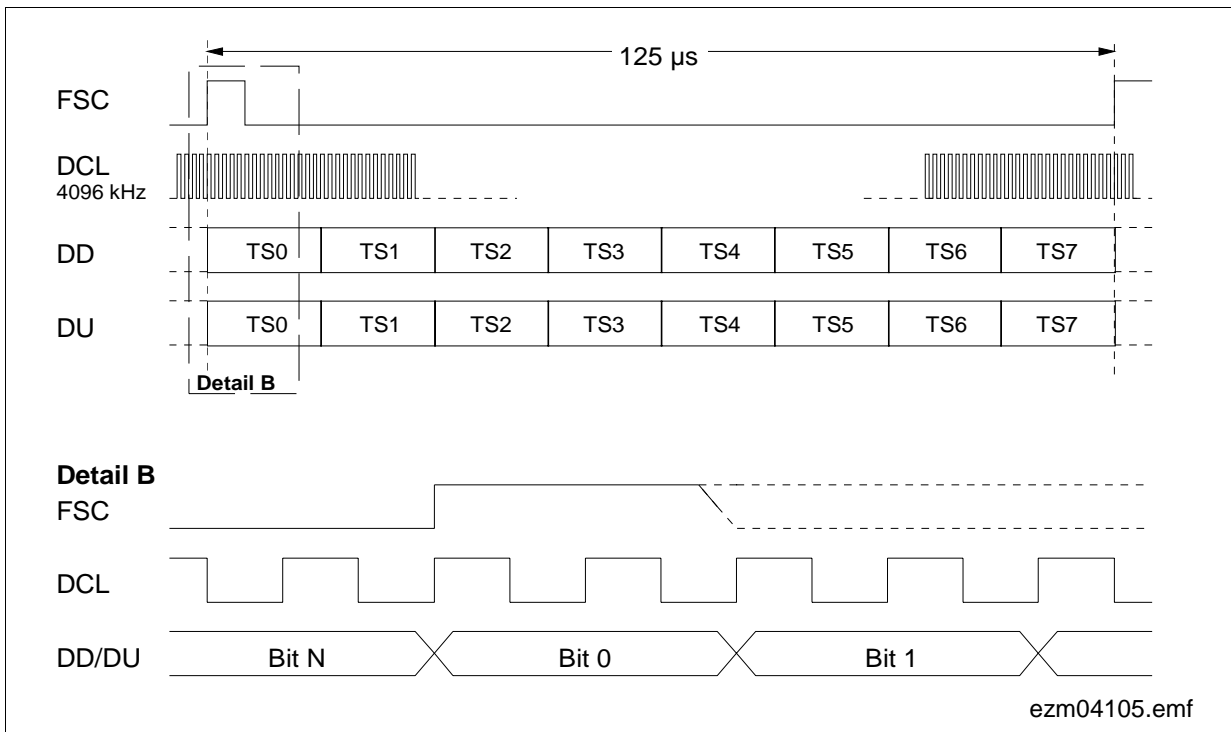

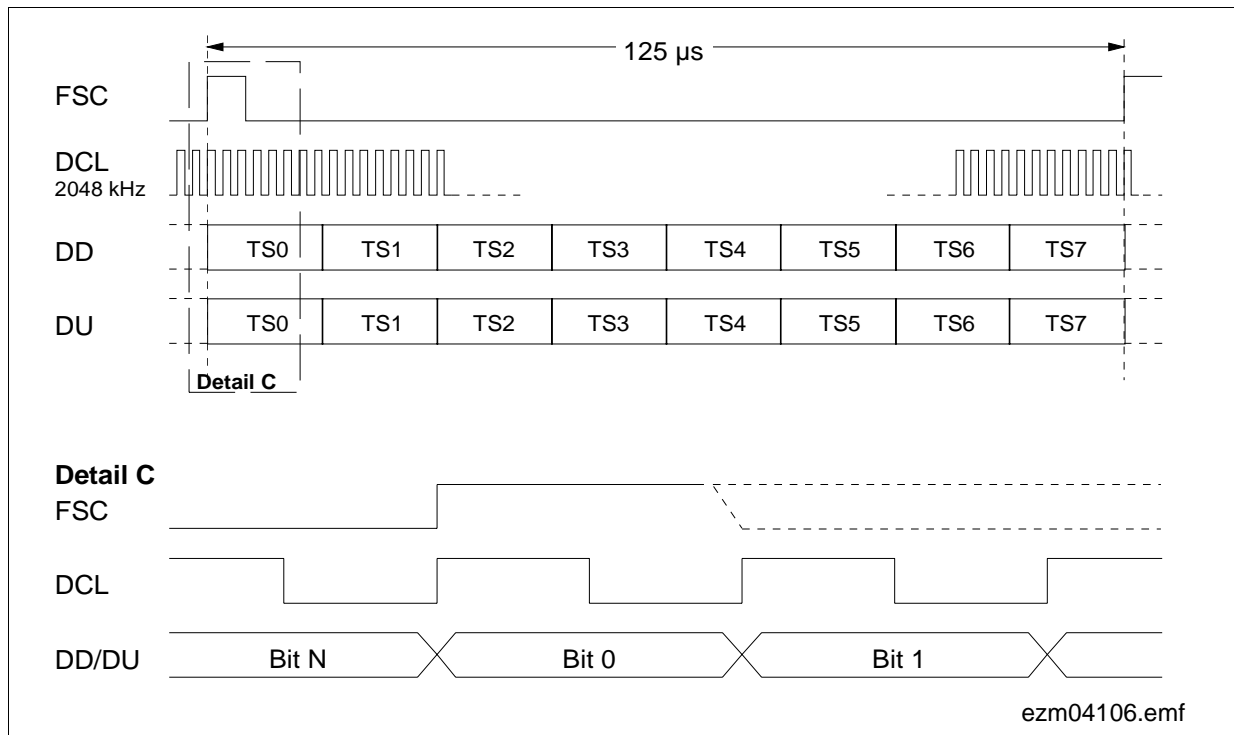**Figure 45   IOM-2 Interface Timing (DCL = 4096 kHz, Per 8 kHz Frame)**

Figure 46   IOM-2 Interface Timing (DCL = 2048 kHz, Per 8-kHz Frame)

Both DuSLIC channels (see **Figure 44**) can be assigned to one of the eight time slots. Set the IOM-2 time slot selection as shown in **Table 25** below by pin-strapping. In this way, up to 16 channels can be handled with one IOM-2 interface on the line card.

Table 25   IOM-2 Time Slot Assignment

TS2	TS1	TS0	IOM-2 Operating Mode
0	0	0	Time slot 0; DCL = 2048, 4096 kHz
0	0	1	Time slot 1; DCL = 2048, 4096 kHz
0	1	0	Time slot 2; DCL = 2048, 4096 kHz
0	1	1	Time slot 3; DCL = 2048, 4096 kHz
1	0	0	Time slot 4; DCL = 2048, 4096 kHz
1	0	1	Time slot 5; DCL = 2048, 4096 kHz
1	1	0	Time slot 6; DCL = 2048, 4096 kHz
1	1	1	Time slot 7; DCL = 2048, 4096 kHz

2 MHz or 4 MHz DCL is selected by the SEL24 pin:

SEL24 = 0: DCL = 2048 kHz

SEL24 = 1: DCL = 4096 kHz

4.3 TIP/RING Interface

The TIP/RING interface is the interface that connects the subscriber to the DuSLIC. It meets the ITU-T recommendation Q.552 for a Z-interface and applicable LSSGR.

4.4 SLICOFI-2S/-2S2 and SLIC-S/-S2 Interface

The SLIC-S/-S2 PEB 4264/-2 operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 26   SLIC-S/-S2 Interface Code

		C2 (Pin 17)		
		L	**M**	**H**
C1 (Pin 18)	**L**[1)	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	unused	HIT	HIR

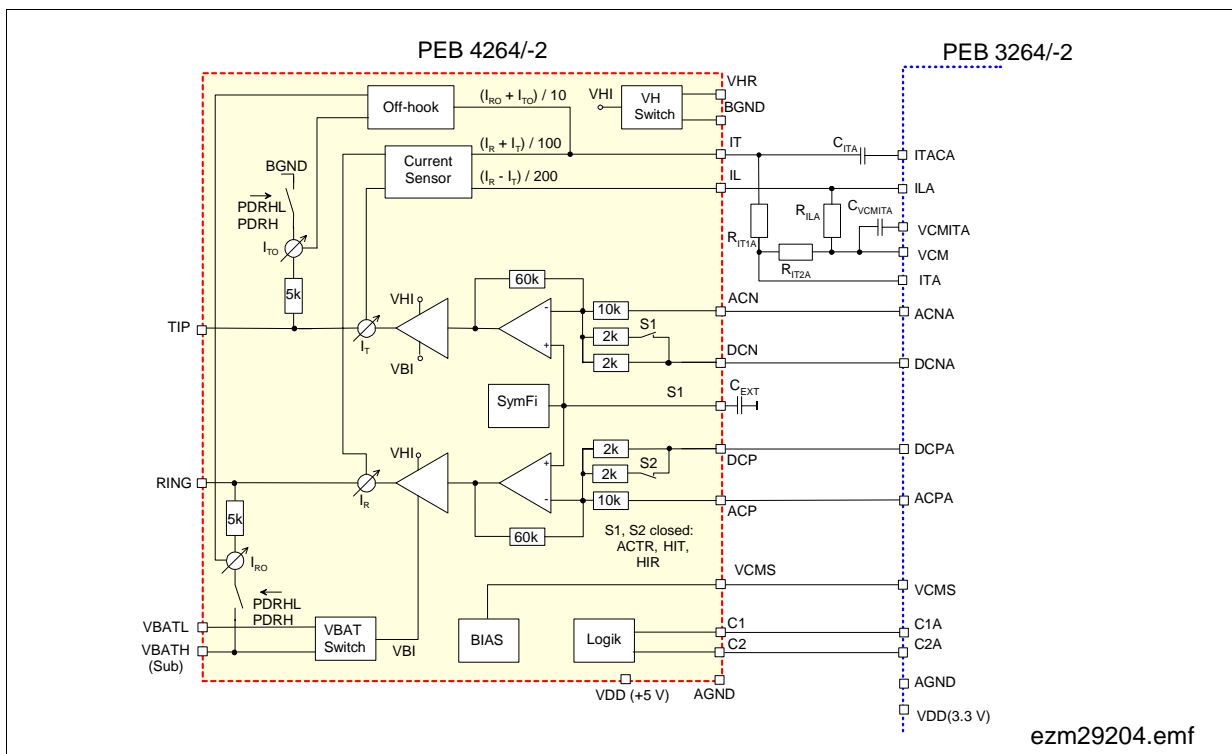[1)   no "Overtemp" signaling possible via pin C1 if C1 is low.

Figure 47   Interface SLICOFI-2S/-2S2 and SLIC-S/-S2

4.5   SLICOFI-2 and SLIC-E/-E2 Interface

The SLIC-E/-E2 PEB 4265/-2 operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 27   SLIC-E/-E2 Interface Code

		C2		
		L	**M**	**H**
C1	**L**[1]	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

[1] no "Overtemp" signaling possible via pin C1 if C1 is low.
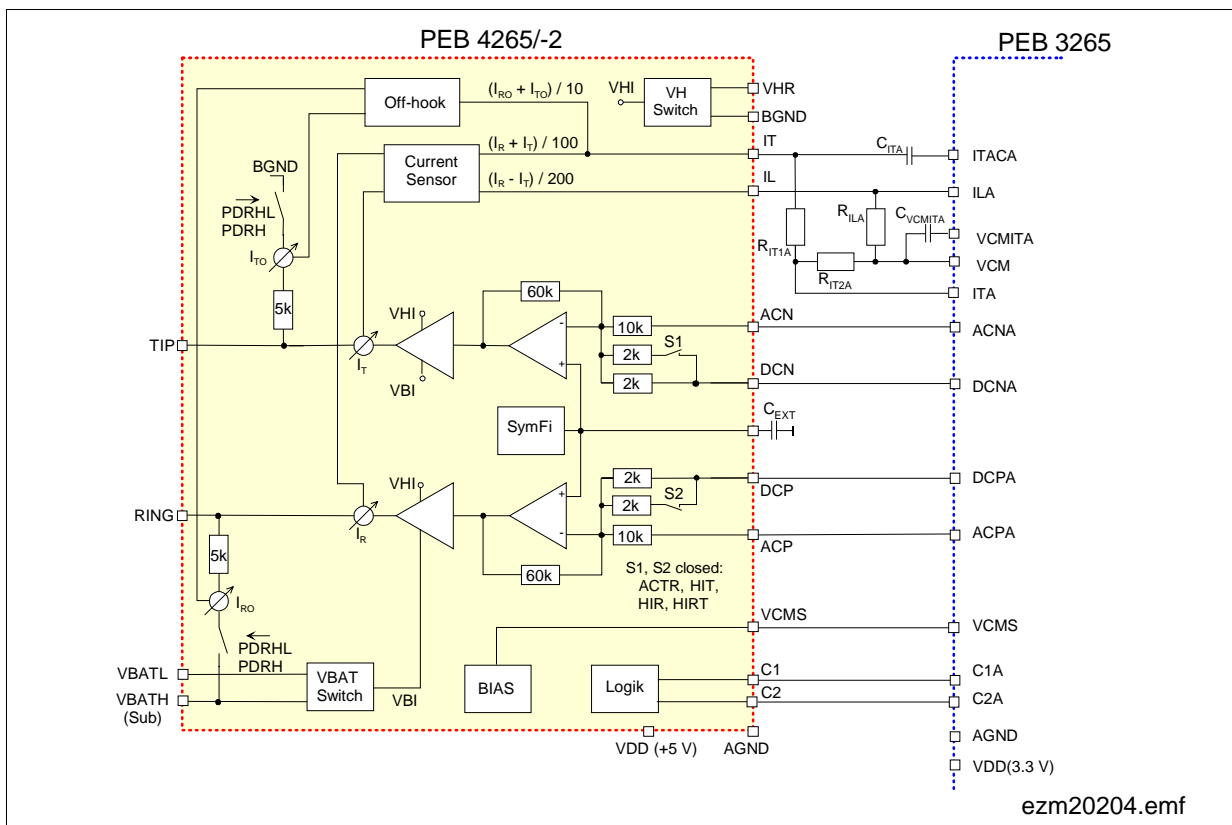
Figure 48   Interface SLICOFI-2 and SLIC-E/-E2

4.6 SLICOFI-2 and SLIC-P Interface

The SLIC-P PEB 4266 operates in the following modes controlled by a ternary logic signal at the C1, C2 inputs and a binary logic signal at C3 input:

Table 28 **SLIC-P Interface Code**

		C2		
		L	**M**	**H**
	L[1]	PDH	PDRR	PDRRL
			PDRHL	PDRH
C1	**M**	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR
			ROT	ROR

C3 = H or L	C3 = H[2]	C3 = L[2]

[1] no "Overtemp" signaling possible via pin C1 if C1 is low.

[2] C3 pin of SLIC-P is typically connected to IO2 pin of SLICOFI-2. For extremely power-sensitive applications using external ringing the C3 pin can be connected to GND.
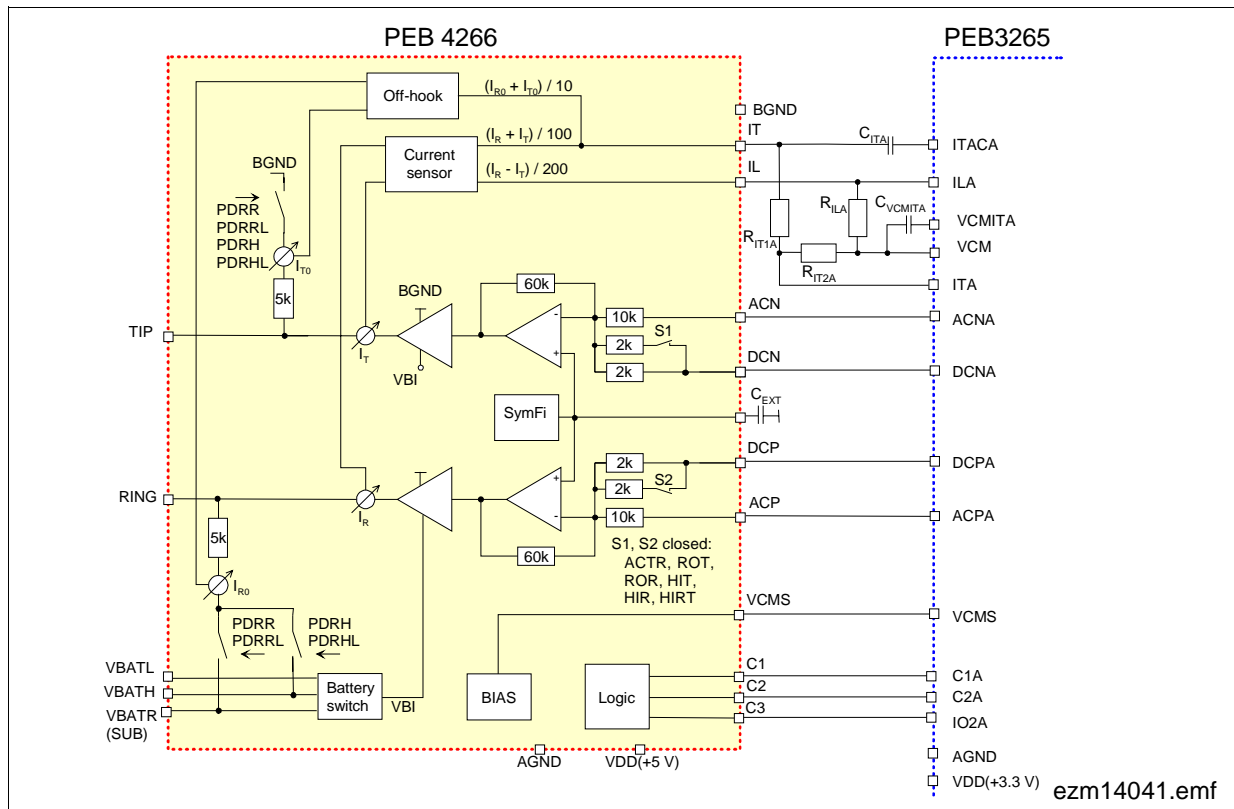

Figure 49 **Interface SLICOFI-2 and SLIC-P**

5 Application Circuits

Application circuits are shown for internal ringing with DuSLIC-E/-E2/-S/-P (balanced and unbalanced) and for external unbalanced ringing with DuSLIC-E/-E2/-S/-S2/-P for one line. Channel A and the SLIC have to be duplicated in the circuit diagrams to show all components for 2 channels.

5.1 Internal Ringing (Balanced/Unbalanced)

Internal balanced ringing is supported up to 85 Vrms for DuSLIC-E/-E2/-P and up to 45 Vrms for DuSLIC-S. Internal unbalanced ringing is supported for SLIC-P with ringing amplitudes up to 50 Vrms without any additional external components. Off-hook detection and ring trip detection are also fully internal in the DuSLIC chip set.

DuSLIC

Application Circuits

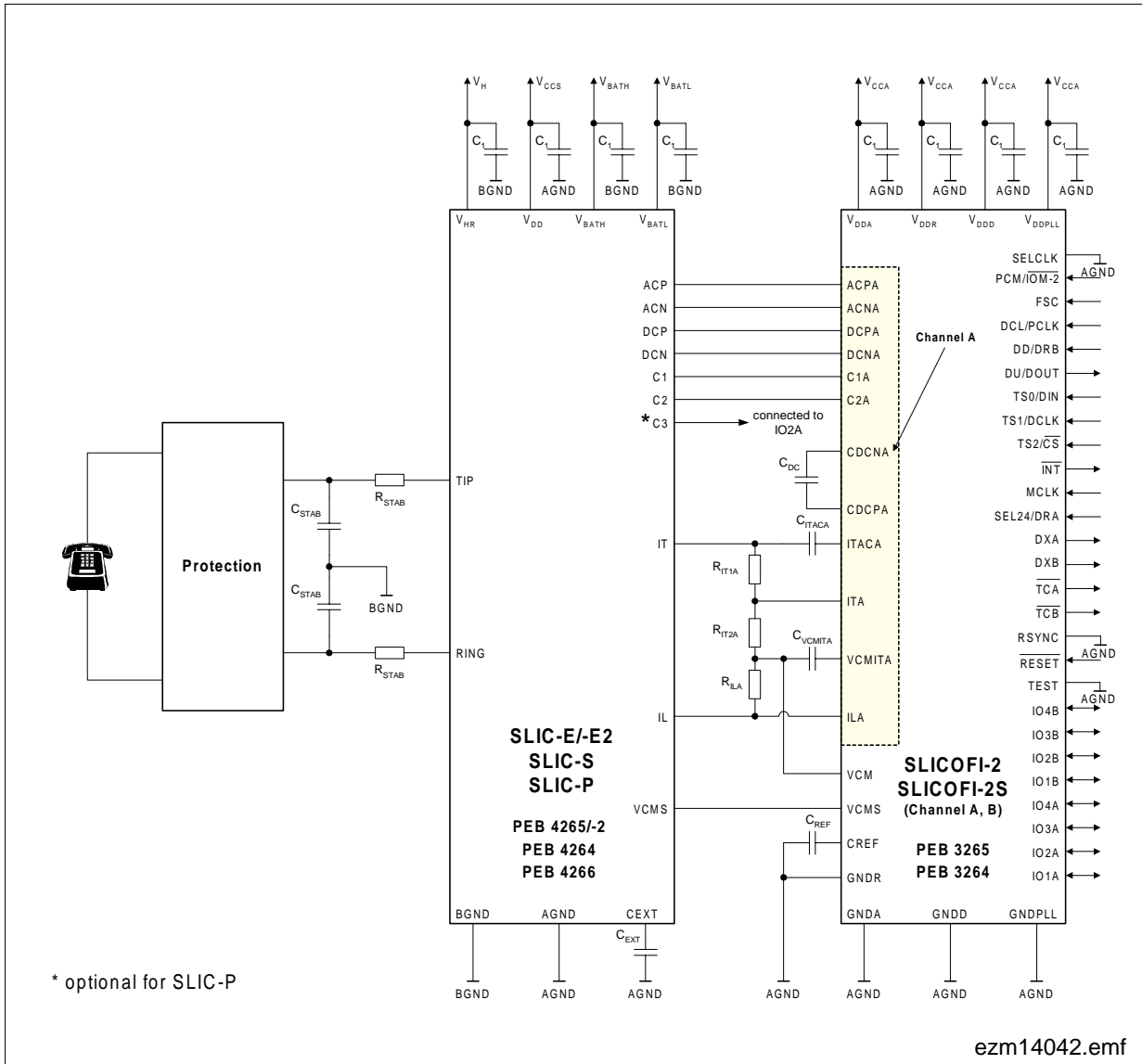## 5.1.1   Circuit Diagram Internal Ringing

ezm14042.emf

Figure 50   Application Circuit, Internal Ringing (Balanced & Unbalanced)

As shown in **Figure 50** both balanced and unbalanced internal ringing uses the same line circuit.

*Note: Only the codec/SLIC combinations shown in **Table 1 "DuSLIC Chip Sets" on Page 2** are possible.*

5.1.2 Protection Circuit for SLIC-E/-E2 and SLIC-S

A typical overvoltage protection circuit for SLIC-E/S is shown in **Figure 51**. Other proved application schemes are available on request.
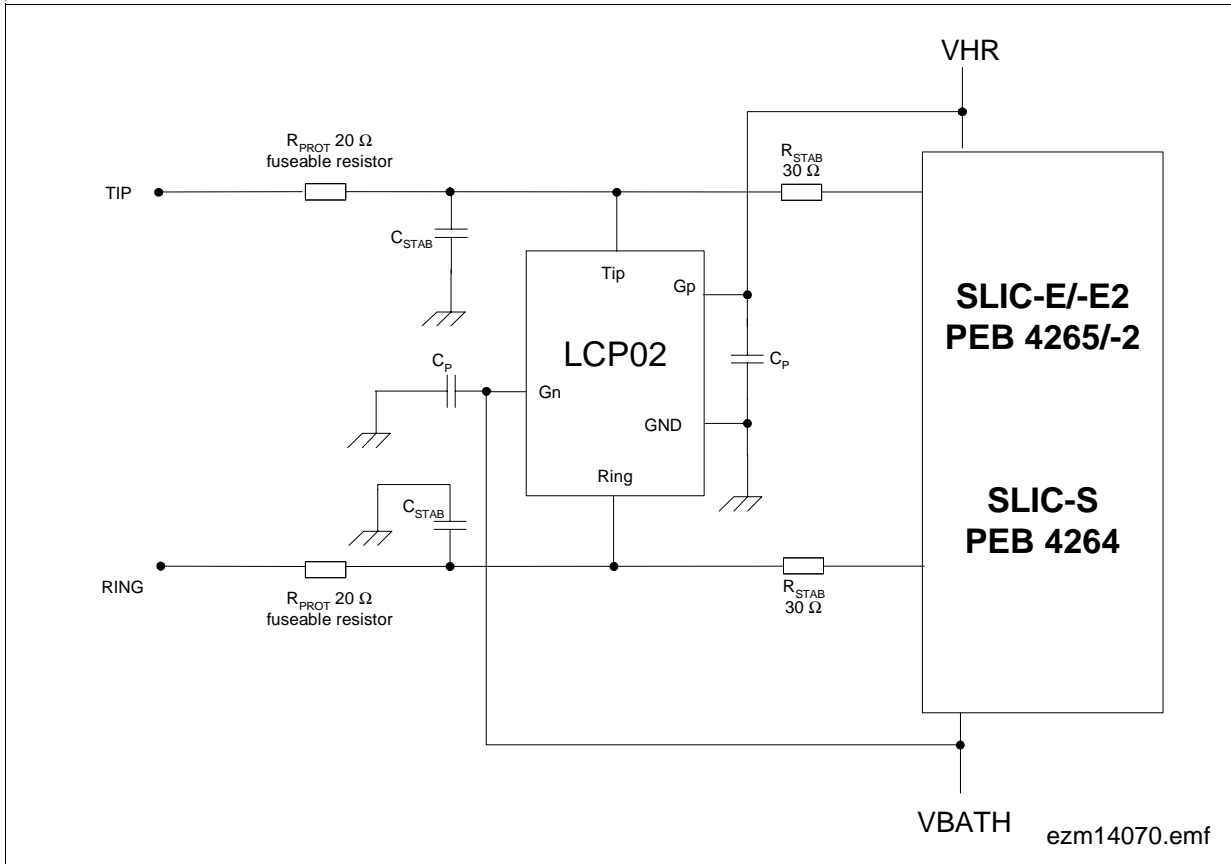

Figure 51   Typical Overvoltage Protection for SLIC-E/-E2 and SLIC-S

The LCP02 (from STM) protects against overvoltage strikes exceeding V_{HR} and V_{BATH}. Protection resistors must be rated for lightning pulses. In case of power contact, protection resistors must become high impedance or additional fuses are needed.

5.1.3 Protection Circuit for SLIC-P

A typical protection circuit for SLIC-P is shown in **Figure 52**. Other proved application schemes are available on request.
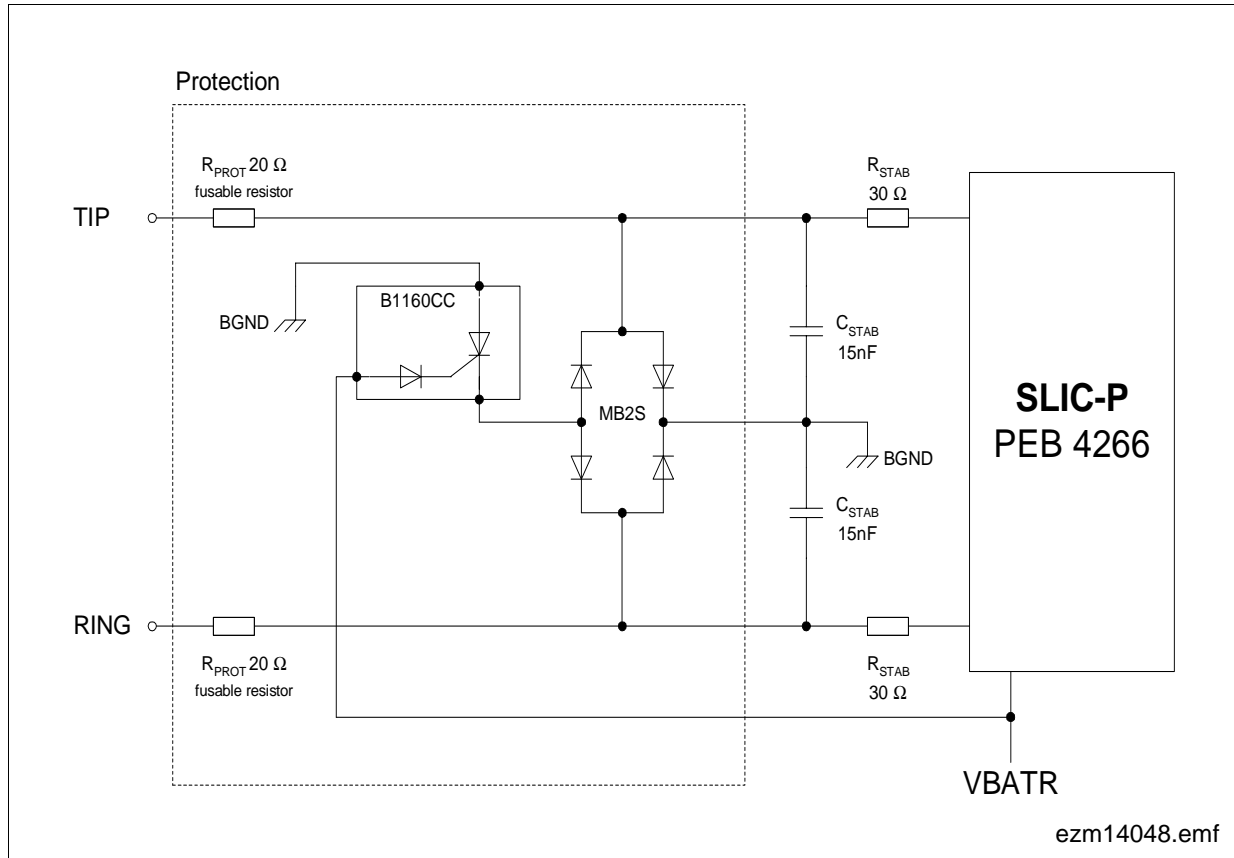

Figure 52   Typical Overvoltage Protection for SLIC-P

The gate trigger voltage of the Battrax B1160CC (Teccor) can be set down to the battery voltage of V_{BATR} (− 150 V).

Protection resistors must be rated for lightning pulses. In case of power contact, protection resistors must become high impedance or additional fuses are needed.

5.1.4   Bill of Materials (Including Protection)

Table 29 shows the external passive components needed for a dual channel solution consisting of one SLICOFI-2/-2S and two SLIC-E/-E2/-S/-P.

Table 29   External Components in Application Circuit for DuSLIC-E/-E2/-S/-P

No.	Symbol	Value	Unit	Tolerance	Rating	DuSLIC -E/-E2/-S	DuSLIC -P
2	R_{IT1}	470	Ω	1 %		x	x
2	R_{IT2}	680	Ω	1 %		x	x
2	R_{IL}	1.6	kΩ	1 %		x	x
4	R_{STAB}	30	Ω	1 %[1]		x	x
4	R_{PROT}	20	Ω	1 %[1]		x	x
4	C_{STAB}	15	nF	10 %	see [2]	x	x
2	C_{DC}	120	nF	10 %	10 V	x	x
2	C_{ITAC}	680	nF	10 %	10 V	x	x
2	C_{VCMIT}	680	nF	10 %	10 V	x	x
1	C_{REF}	68	nF	20 %	10 V	x	x
2	C_{EXT}	470	nF	20 %	10 V	x	x
12	C_1	100	nF	10 %		x	x
2	Battrax	B1160CC	–	–	according to supply voltage V_{BATR}		x
2	Diode-bridge	MB2S					x
2	STM	LCP-02				x	
4	C_P	220	nF	20 %	according to supply voltage V_{BATH} and V_{HR}	x	

[1] matching tolerance is dependent on longitudinal balance requirement

[2] according to the highest used battery voltage IV_{BATR}I for SLIC-P and IV_{HR}I or IV_{BATH}I for SLIC-E/-E2/-S

For handling higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, e.g., a current-compensated choke of 470 µH in the Ring/Tip lines.

Additionally to the capacitors C_1 a 22 µF capacitor per 8 Ring/Tip lines is recommended for buffering the supply voltages.

5.2 External Unbalanced Ringing with DuSLIC-E/-E2/-S/-S2/-P

External unbalanced ringing applications are shown for a standard solution (see **Figure 53**) and for a solution dedicated to higher loop lengths (see **Figure 54**).

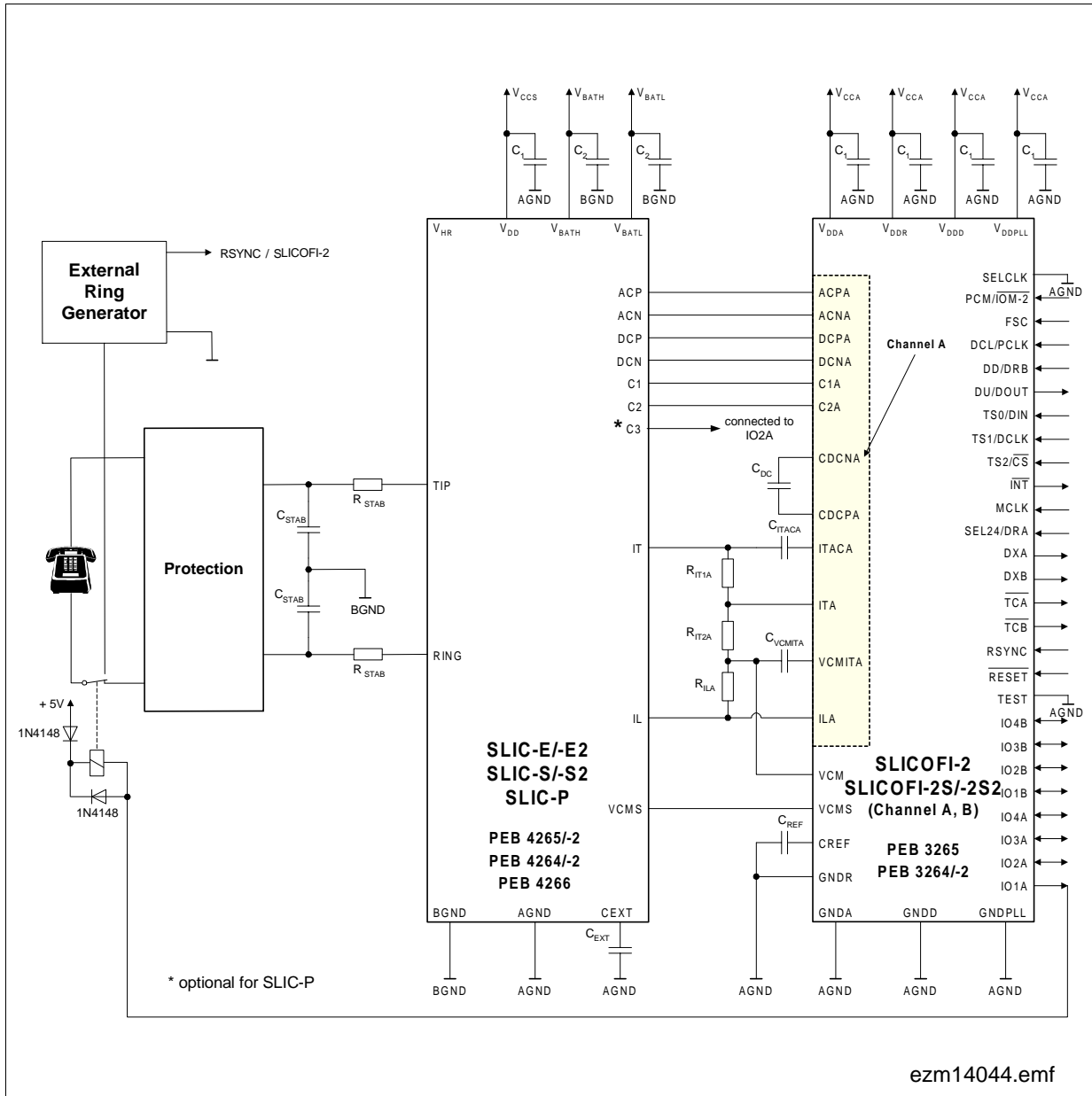*Note: Only the codec/SLIC combinations shown in **Table 1 "DuSLIC Chip Sets" on Page 2** are possible.*

ezm14044.emf

Figure 53   Application Circuit, External Unbalanced Ringing

This circuit senses the ring current on only one line (Tip line). It is therefore restricted to applications with low longitudinal influence (short lines).
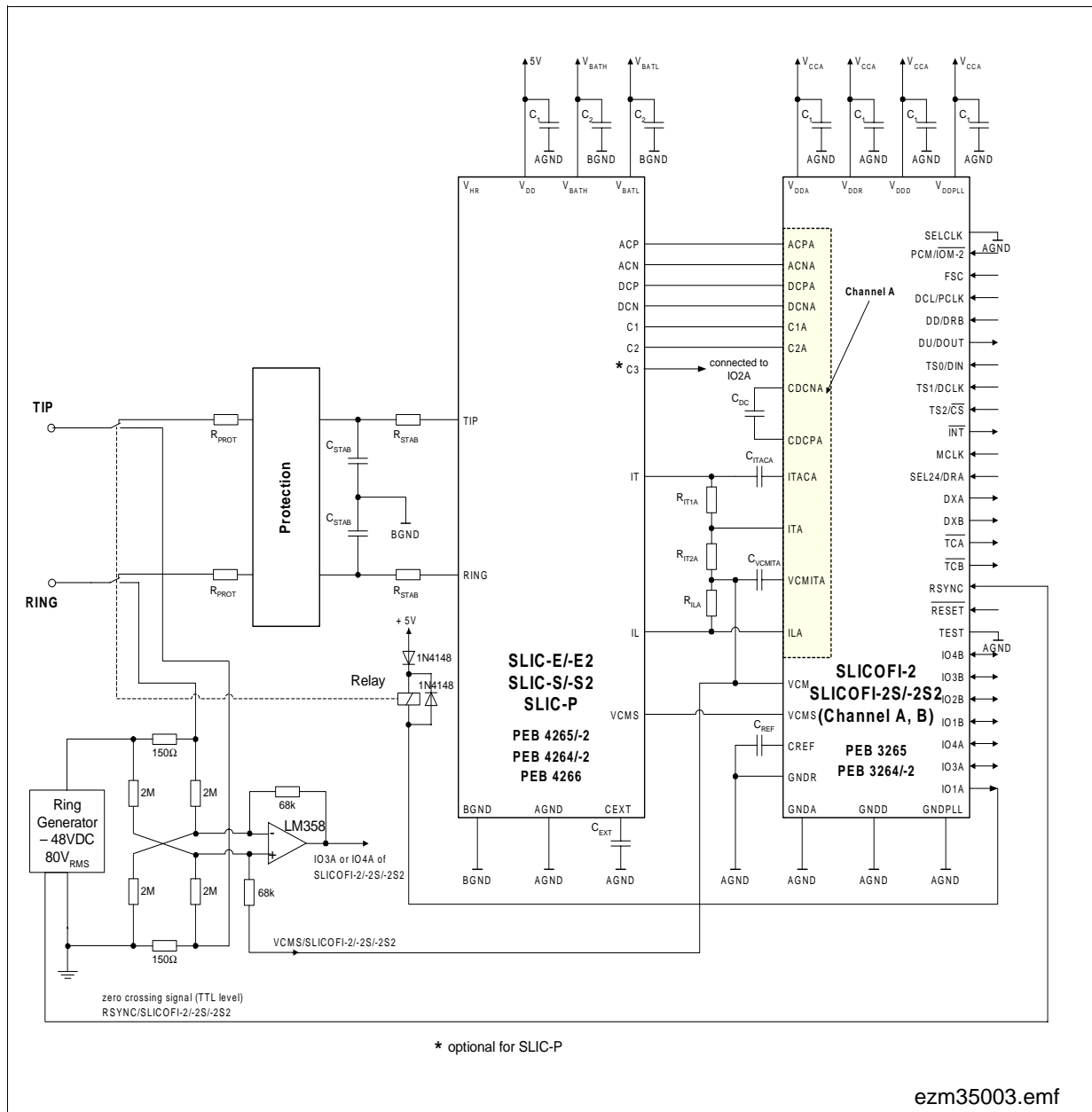
Figure 54   Application Circuit, External Unbalanced Ringing for Long Loops

For handling higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, e.g., a current-compensated choke of 470 µH in the Ring/Tip lines.

This circuit senses the ring current in both Tip and Ring lines. Longitudinal influence is cancelled out. This circuit therefore is recommended for long line applications.

6   Index

Numerics

170V technology 27

A

Active 60
Active High 52, 54, 56, 58
Active Low 52, 54, 56, 58
Active Ring 52, 54, 56, 59
Active State 36, 62
Active with HIR 53, 55, 57, 59
Active with HIT 53, 55, 57, 59
Active with Metering 53

B

Balanced ringing 95
Battery feed 9

C

Caller ID 5, 12
Central Office 6
Coding 9

D

Digital Loop Carrier 6
DTMF 12
DTMF decoder 5
DTMF generator 5
DuSLICOS 11

E

Enhanced Digital Signal Processor 40
External Components
    DuSLIC-P 99
External conference 49
External Ringing 32, 75

F

Fiber in the Loop 6
Frequency response 11
FSK 12

G

Ground Start 53

H

Hybrid 9
Hybrid balance 11

I

Impedance matching 11
Intelligent NT 6
Internal conference 49
IOM-2 interface 83, 89
ISDN Terminal Adapters 6

L

Levelmeter
    AC 77
    DC 77
LIN mode 51
LIN16 mode 51
Line Echo Cancellation 12
Line Resistance 70

M

Message waiting 5
Metering 5
Microcontroller interface 83, 86

O

Operating Modes
    DuSLIC-E/-E2 56
    DuSLIC-P 58
    DuSLIC-S/-S2 54
Overvoltage protection 9

P

PCM interface 24, 83
PCM mode 50
PCM/µC interface 50, 83
PCM16 mode 51
PCM-active 49
PCM-off 49

Infineon goes for Business Excellence

"Business excellence means intelligent approaches and clearly
defined processes, which are both constantly under review and
ultimately lead to good operating results.
Better operating results and business excellence mean less
idleness and wastefulness for all of us, more professional
success, more accurate information, a better overview and,
thereby, less frustration and more satisfaction."

Dr. Ulrich Schumacher

h t t p : / / w w w . i n f i n e o n . c o m