

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SGM0410S provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The SOT-89 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

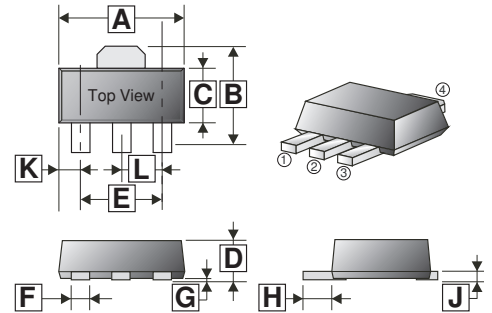
MARKING



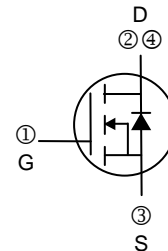
PACKAGE INFORMATION

Package	MPQ	Leader Size
SOT-89	1K	7 inch

SOT-89



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.40	4.60	G	-	-
B	4.05	4.25	H	0.89	1.20
C	2.40	2.60	J	0.35	0.41
D	1.40	1.60	K	0.70	0.80
E	3.00 REF.		L	1.50 REF.	
F	0.40	0.52			



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	V_{DS}	100	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current ¹ @ $V_{GS}=10\text{V}$	I_D	$T_A=25^\circ\text{C}$	2.2	A
		$T_A=70^\circ\text{C}$	1.7	A
Pulsed Drain Current ²	I_{DM}	5.5	A	
Power Dissipation ³	P_D	1.5	W	
Operating Junction & Storage Temperature	T_J, T_{STG}	-55~150	$^\circ\text{C}$	
Thermal Resistance Rating				
Thermal Resistance Junction-Ambient ¹ (Max).	$R_{\theta JA}$	85	$^\circ\text{C} / \text{W}$	
Thermal Resistance Junction-Case ¹ (Max).	$R_{\theta JC}$	36	$^\circ\text{C} / \text{W}$	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Forward Transconductance	g_{fs}	-	5.4	-	S	$V_{DS}=5\text{V}, I_D=2\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}= \pm 20\text{V}$
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	$V_{DS}=80\text{V}, V_{GS}=0, T_J=25^\circ\text{C}$
		-	-	5		$V_{DS}=80\text{V}, V_{GS}=0, T_J=55^\circ\text{C}$
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	-	310	m Ω	$V_{GS}=10\text{V}, I_D=2\text{A}$
		-	-	320		$V_{GS}=4.5\text{V}, I_D=1\text{A}$
Gate Resistance	R_g	-	2	-	Ω	$V_{GS}=V_{DS}=0, f=1.0\text{MHz}$
Total Gate Charge(10V)	Q_g	-	9.1	-	nC	$I_D=2\text{A}$ $V_{DS}=50\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	Q_{gs}	-	2	-		
Gate-Drain Change	Q_{gd}	-	1.4	-		
Turn-on Delay Time ²	$T_{d(on)}$	-	2	-	nS	$V_{DD}=50\text{V}$ $I_D=2\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$
Rise Time	T_r	-	21.6	-		
Turn-off Delay Time	$T_{d(off)}$	-	11.2	-		
Fall Time	T_f	-	18.8	-		
Input Capacitance	C_{iss}	-	508	-	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=1.0\text{MHz}$
Output Capacitance	C_{oss}	-	29	-		
Reverse Transfer Capacitance	C_{rss}	-	16.4	-		
Source-Drain Diode						
Diode Forward Voltage ²	V_{SD}	-	-	1.2	V	$I_S=1\text{A}, V_{GS}=0$
Continuous Source Current ^{1,4}	I_S	-	-	2.2	A	$V_D=V_G=0, \text{Force Current}$
Pulsed Source Current ^{2,4}	I_{SM}	-	-	5.5	A	
Reverse Recovery Time	T_{rr}	-	17.5	-	nS	$I_F=2\text{A}, di/dt=100\text{A}/\mu\text{S}, T_J=25^\circ\text{C}$
Reverse Recovery Charge	Q_{rr}	-	14	-	nC	

Note:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.
- The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The power dissipation is limited by 150 $^\circ\text{C}$, junction temperature.
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

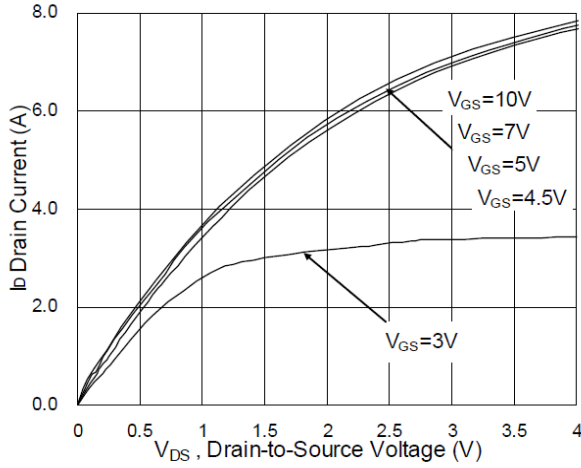


Fig.1 Typical Output Characteristics

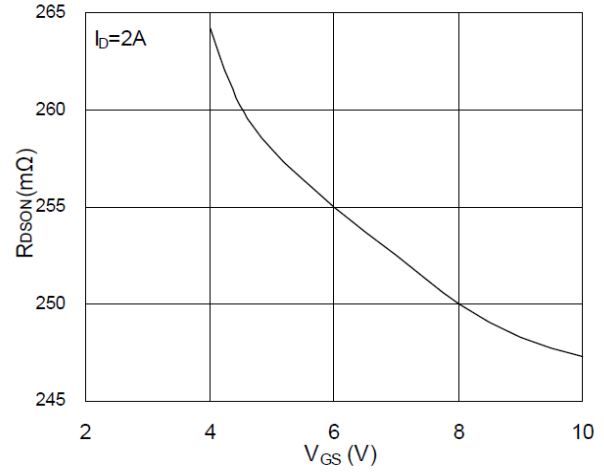


Fig.2 On-Resistance vs. Gate-Source

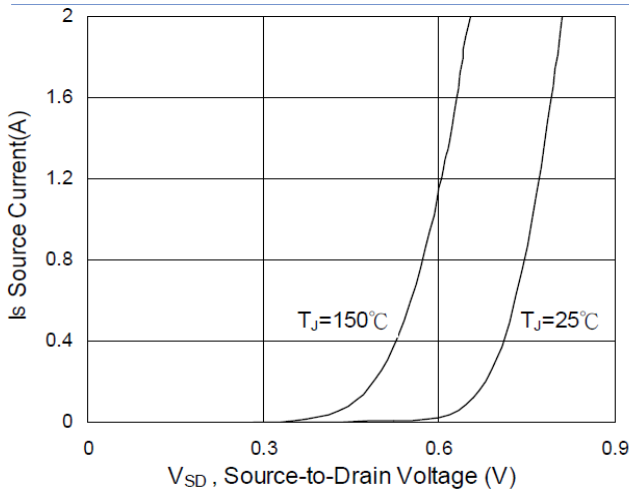


Fig.3 Forward Characteristics of Reverse

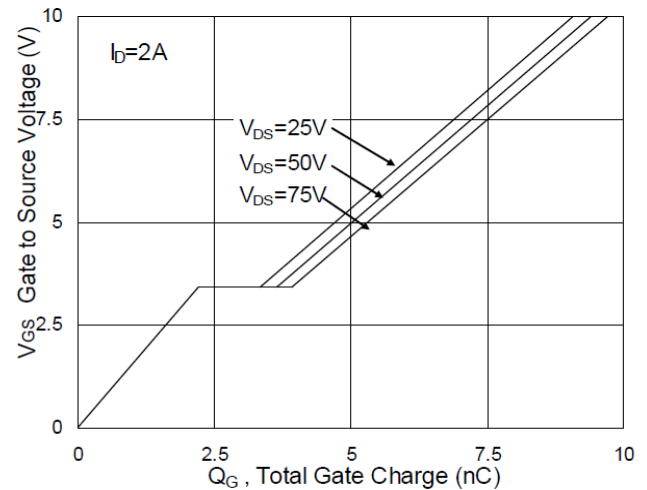


Fig.4 Gate-Charge Characteristics

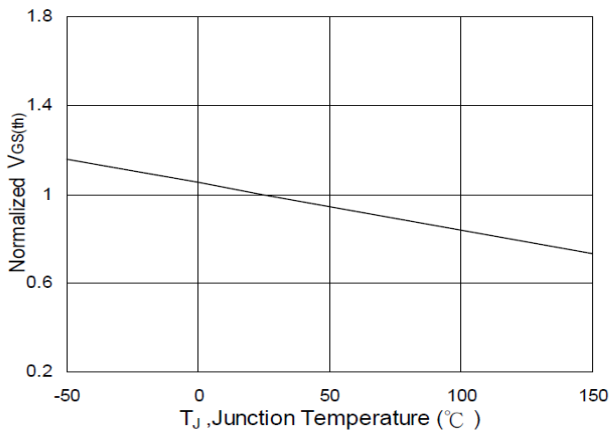


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

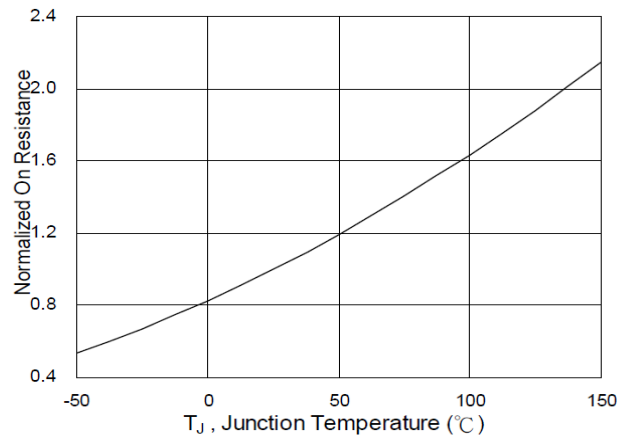


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

CHARACTERISTIC CURVES

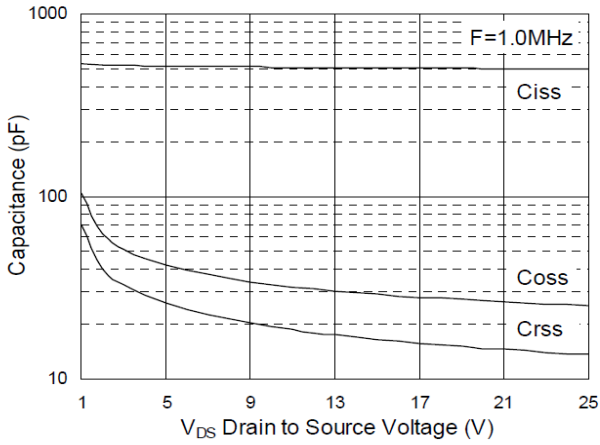


Fig.7 Capacitance

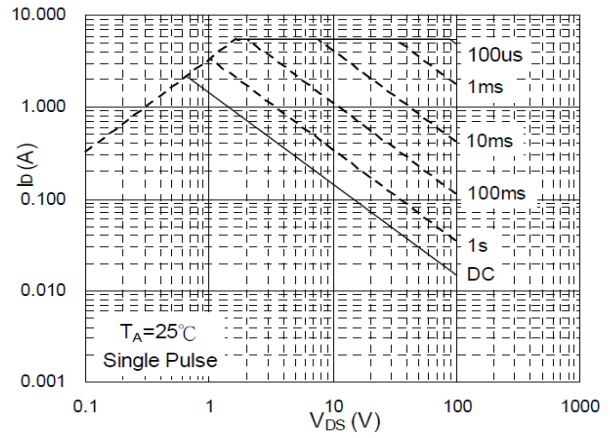


Fig.8 Safe Operating Area

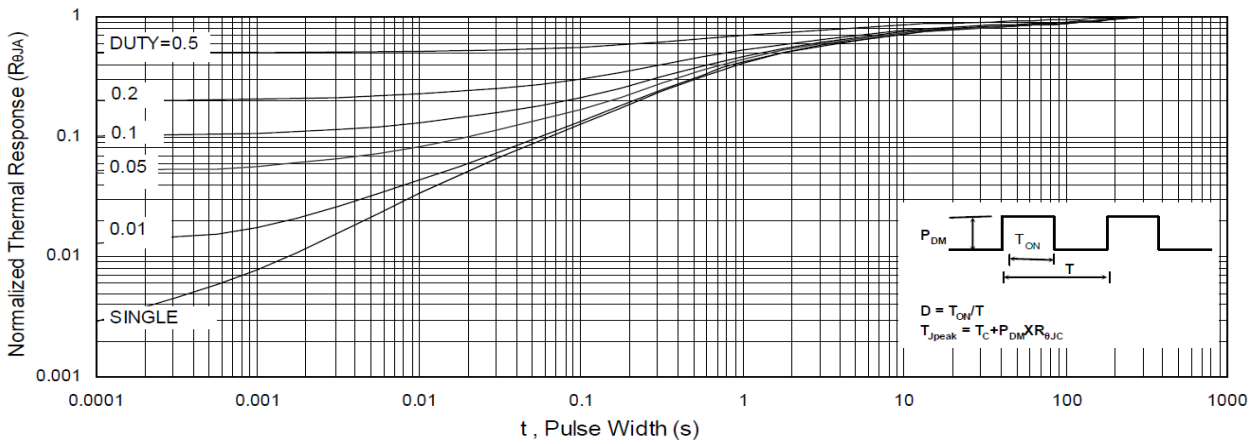


Fig.9 Normalized Maximum Transient Thermal Impedance

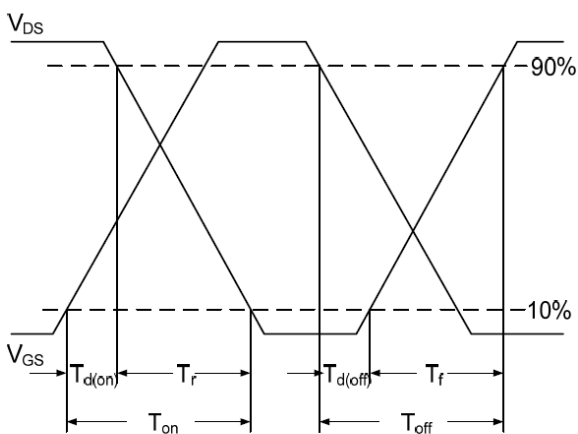


Fig.10 Switching Time Waveform

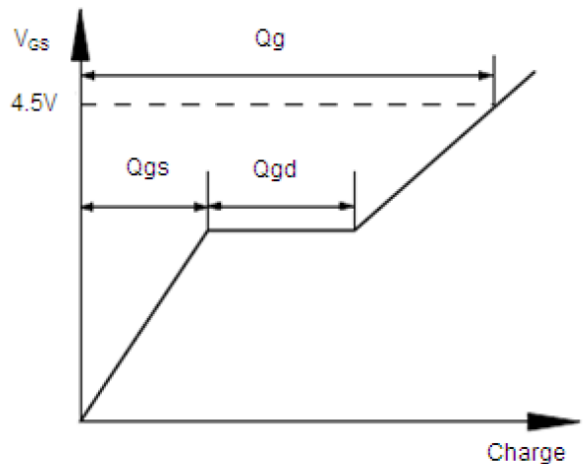


Fig.11 Gate Charge Waveform