MINDSPEED™

CX28560

Product Bulletin

Product Affected: **CX28560-11P, 680-pin TBGA package (40 mm)**

This document describes conditions that may cause the operation of the above device to deviate from published specifications.

TSLP Channel Status Register Always Reads Zero

Description:

Reading of the TSLP channel status register for any channel (at address: 0x128800 + channel number) always returns zero, regardless of the actual channel status.

Recommended Action:

Use the alternative method below to access the channel status:

1. Enable access to extended addresses by writing 1 to the direct access register at offset 0x10C84 (in dwords from the PCI base address)
2. Using the Service Request Mechanism, read the CX28560 register at address 0x12C000 + 4 * channel number.
   - Look at the value of bits 14–16:
     If the channel is *active*, bits 14–16 contain a value other than zero;
     If the channel is *inactive*, bits 14–16 contain a value of zero.
3. Disable access to extended addresses as soon as possible by writing 0 to the direct access register at offset 0x10C84 (in dwords from the PCI base address)

NOTE: When using the driver, the procedure outlined above is incorporated into the MICn856xGetTxChanStatus () function so that no code changes are required.

Possible Miscalculation of FCS in Transmit Direction When PAD Count is Less than Two or Pad Adjust is Enabled

Description:

For channels configured in HDLC FCS-16 or FCS-32 modes, the FCS may be incorrectly calculated in the transmit direction when the Pad Count is less than two, or the Pad Adjust is enabled.

Recommended Action:

1. Use Pad Count >= 2

   and

2. Disable Pad Adjust.

Pad Count is set in the transmitted fragment header (only for the last fragment in a packet), in bits 11:4.

Pad Adjust is disabled by clearing bit #2 (TPADJ) in the TSLP Channel Configuration Register (address 0x129000 + channel number).

The relative amount of bandwidth left unexploited by using this method is at most 4.44% for 40-byte packets.