ANALOG DEVICES

Complete, Voltage Output
12-Bit Buffered DAC
AD3860

FEATURES
Resolution: 12 Bits
Nonlinearity: ±1/2LSB T_{min} to T_{max}
12-Bit Input Register
Small Size: 24 pin DIP
Fast Settling: 5µs to ±0.01%
Internal Reference
Internal Output Amplifier

AD3860 FUNCTIONAL BLOCK DIAGRAM
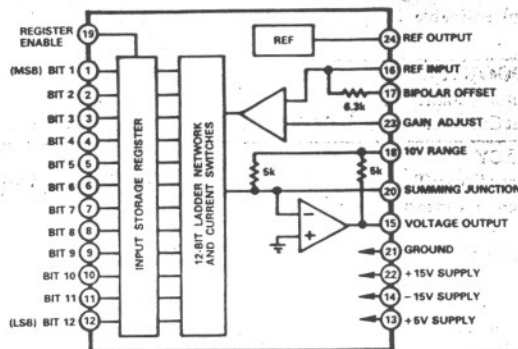
PRODUCT DESCRIPTION
The AD3860 is a precision 12-bit D/A converter designed for direct interface to microprocessors.

The functional diagram shows that the AD3860 consists of a 12-bit input storage register, a 12-bit DAC, internal reference, and a fast output amplifier. It is TTL compatible and the register enable facilitates deglitching and microprocessor interfacing. The low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, external current capability and temperature drift characteristics. The output amplifier gives the user a voltage output and combines with the other features of this circuit to produce a functionally complete digital to analog converter.

The AD3860 is laser trimmed to achieve ±1/4LSB linearity typical and ±1/2LSB maximum over the full operating temperature range. The low T.C. Binary ladder guarantees that the AD3860 will be monotonic over the specified temperature range.

The AD3860 is available in two versions. The AD3860K is specified for use over 0 to +70°C temperature range. The AD3860S is specified for the −55°C to +125°C temperature range and is especially recommended for high reliability needs in harsh environments. All units are in supplied in 24-pin, hermetically-sealed ceramic DIPs.

PRODUCT HIGHLIGHTS
1. The AD3860 is a functionally complete voltage output DAC with voltage reference, digital latches, and output amplifier in a single hybrid package.

2. The input buffer latches permit interface to microprocessor data buses. All logic inputs are TTL or 5 volt CMOS compatible.

3. Laser trimming the thin-film resistors assures superior linearity and accuracy stability over temperature. Both commercial and military temperature range models have ±1/2LSB linearity maximum guaranteed over the full operating temperature range.

4. Monotonicity is also guaranteed over the full operating temperature range. The typical full scale temperature coefficient is 10ppm/°C.

5. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.

6. The fast output amplifier provides a voltage output with a 5µs settling time to 0.01% for a 20 volt step. The AD3860 is designed for military and industrial applications where high speed D/A conversion is required.

SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted)

Model	AD3860K	AD3860S
DIGITAL INPUTS		
Resolution	12 Bits	*
Logic Coding: Unipolar Ranges	Complementary Straight Binary	*
Bipolar Ranges	Complementary Offset Binary	*
Logic Levels (TTL Compatible): Logic "1"	+2.0V dc min, +5.5V dc max	*
Logic "0"	0V dc min, 0.8V dc max	*
Input Currents		
Data Inputs: Logic "1"	30µA max	*
Logic "0"	−0.6mA max	*
Register Enable: Logic "1"	60µA max	*
Logic "0"	−1.2mA max	*
ANALOG OUTPUT		
Output Impedance	0.5Ω	*
Output Current @ $Z_L = 2k\Omega \| 250pF$	±10mA, ±5mA min	*
ACCURACY		
Linearity Error (T_{min} to T_{max})	±1/4LSB[1], ±1/2LSB max	±1/2LSB max
Differential Linearity Error	±1/2LSB, ±1LSB max	±1LSB
Monotonicity	Guaranteed Over Temperature	
Full Scale Absolute Accuracy Error[2]	±0.05% FSR[3], ±0.1% FSR max	*
T_{min} to T_{max}	±0.15% FSR, ±0.3% FSR max	*
Zero Error	±0.025% FSR, ±0.05% FSR max	*
T_{min} to T_{max}	±0.05% FSR, ±0.1% FSR max	*
Gain Error	±0.1%	*
DRIFT		
Gain	±10ppm/°C	*
Offset	±5ppm/°C	*
DYNAMIC CHARACTERISTICS		
Settling Time to ±0.01% for: 20V Step	5µs, 7µs max	*
10V Step	3µs, 5µs max	*
Output Slew Rate	20V/µs	
Register Enable[4]		
Pulse Width	60ns min	*
Setup Time Digital Data to Enable	40ns min	*
INTERNAL REFERENCE VOLTAGE		
Voltage	+6.3V	*
Accuracy	±2%	*
External Current	2.5mA max	*
POWER SUPPLIES		
Power Supply Range: +15V Supply	+14.55V min, +15.45V max	*
−15V Supply	−14.55V min, −15.45V max	*
+5V Supply	+4.75V min, +5.25V max	*
Power Supply Rejection: +15V Supply	±0.002% FSR/% V_S	*
	±0.01% FSR/% V_S max	
−15V Supply	±0.002% FSR/% V_S	*
	±0.004% FSR/% V_S max	
Current Drain: +15V Supply	10mA, 20mA max	*
−15V Supply	−12mA, −30mA max	*
+5V Supply	30mA, 50mA max	*
Power Consumption	675mW, 1W max	*
TEMPERATURE RANGE		
Operating	0 to +70°C	−55°C to +125°C
Storage	−65°C to +150°C	*
PACKAGE OPTION[5]		
24-Pin DIP	HY24C	*

NOTES
[1] Least Significant Bit (LSB).
[2] Absolute Accuracy Error includes gain, offset, linearity, noise and all other errors and is specified. without adjustment.
[3] FSR is Full Scale Range and is 20V for ±10 range.
[4] The AD3860's analog output will follow its digital input when register enable is a logic "0". Digital Input date will be latched and analog output voltage constant when register enable is a logic "1".
[5] See Section 19 for package outline information.

*Same as AD3860K.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

+15 Volt Supply (pin 22) . . . . . . +18V
−15 Volt Supply (pin 14) . . . . . . −18V
+5 Volt Supply (pin 13) . . −0.5V to +7V
Register Enable (pin 19) . −0.5V to +5.5V
Digital Inputs (pins 1–12) . −0.5V to +5.5V

PIN CONFIGURATION
24 LEAD DUAL IN-LINE-PACKAGE

PIN NO.	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12 (LSB)
13	LOGIC SUPPLY
14	$-V_S$
15	V_{OUT}
16	REF INPUT
17	BIPOLAR OFFSET
18	10V RANGE
19	REGISTER ENABLE
20	SUMMING JUNCTION
21	COMMON
22	$+V_S$
23	GAIN ADJUST
24	$6.3V_{REF}$ OUT

APPLICATIONS INFORMATION

OUTPUT VOLTAGE RANGE SELECTION

Output Range	0 to +10V	±5V	±10V
Pin Connection			
Connect Pin 24 to	16	16	16
Connect Pin 17 to	21	20	20
Connect Pin 15 to	18	18	NC
Connect Pin 20 to	NC	17	17

INPUT LOGIC CODING

Digital Input		Analog Output		
MSB	LSB	0 to +10V	±5V	±10V
0000 0000 0000		+9.9976V	+4.9976V	+9.9951V
0000 0000 0001		+9.9951V	+4.9951V	+9.9902V
0111 1111 1111		+5.0000V	0.0000V	0.0000V
1000 0000 0000		+4.9976V	−0.0024V	−0.0049V
1111 1111 1110		+0.0024V	−4.9976V	−9.9951V
1111 1111 1111		0.0000V	−5.0000V	−10.0000V

CODING NOTES:
1. For unipolar operation the coding complementary straight binary (CSB).
2. For bipolar operation, the coding complementary offset binary (COB).
3. For FSR = 20V, 1LSB = 4.88mV.
4. For FSR = 10V, 1LSB = 2.44mV.

Layout Considerations

Proper layout and decoupling is necessary to obtain the AD3860's specified accuracy. Ground (pin 21) must be tied to circuit analog ground as close to the package as possible. Grounding through a large ground plane beneath the package is preferred.

Power supplies should be decoupled with electrolytic or tantalum capacitors near the unit. A 1µF capacitor is parallel with a 0.01µF ceramic capacitor on all supplies is recommended, see Figure 1.
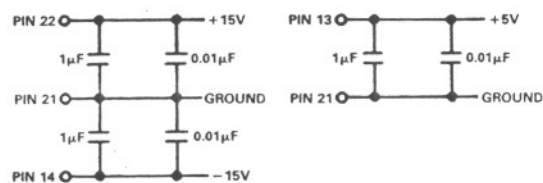

Figure 1. Power Supply Decoupling

Coupling between analog and digital signals should be minimized to avoid noise pick up. Use short jumpers to tie the reference output (pin 24) to the reference input (pin 16) and to tie the bipolar offset (pin 17) to the summing junction (pin 20).

If the external full scale and zero adjustments are used, the series 6.8MΩ resistors should be placed as close to the unit as possible.

Reference Output

The AD3860 is laser trimmed to operate from the internal 6.3 volt voltage reference. The user has the option of supplying an external reference but for specified operation the reference output (pin 24) must be connected to the reference input (pin 16). The internal reference can be used to drive an external load, but it should be buffered if load current will exceed 2.5mA.

Optional Full Scale and Zero (−Full Scale) Adjustments

The AD3860 will operate as specified without adjustment, however, absolute accuracy error can be reduced to ±1LSB by trimming as described below. Adjustments should be made after warmup. As shown in Figures 2 and 3 the zero
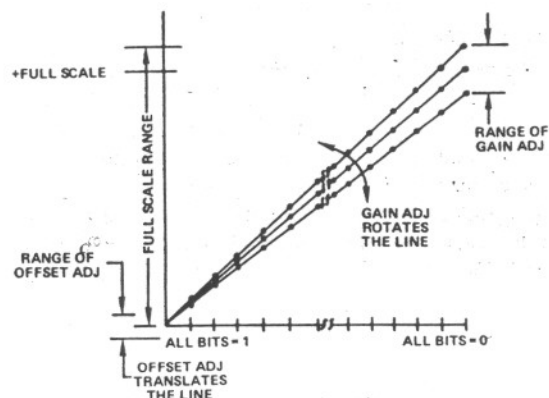

Figure 2. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)
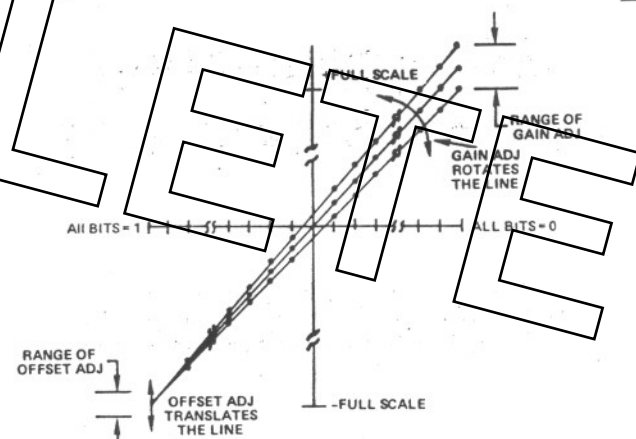

Figure 3. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)

(−full scale) adjustment should be made before the full scale adjustment. We recommend multiturn potentiometers with maximum temperature coefficients of 100ppm/°C. Series resistors can be ±20% carbon composition or better. If these adjustments are not used pins 20 and 23 should not be grounded.

Zero (−Full Scale) Adjustment

Connect the potentiometer as shown and apply all "1s" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for unipolar output ranges and minus full scale for bipolar output ranges.
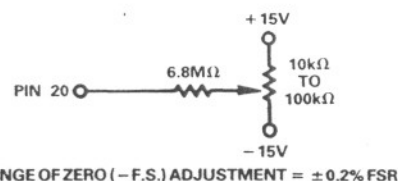

RANGE OF ZERO (−F.S.) ADJUSTMENT = ±0.2% FSR

Full Scale Adjustment

Connect the potentiometer as shown and apply all "0s" to the digital inputs. Adjust the potentiometer for maximum chosen analog output.

RANGE OF GAIN (F.S.) ADJUSTMENT = 0.35% FSR
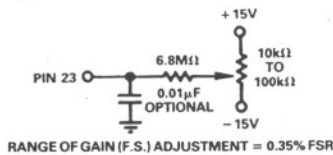
REGISTER ENABLE

When the register enable (pin 19) is high (hold mode) the digital data in the input register will be latched. When the register enable is low (track mode) the converter's output will follow its input. To latch new digital data into the register, the register enable must go low for a minimum of 60ns and the digital input data must be valid for a minimum of 40ns before the register enable goes high again. See the timing diagram below.
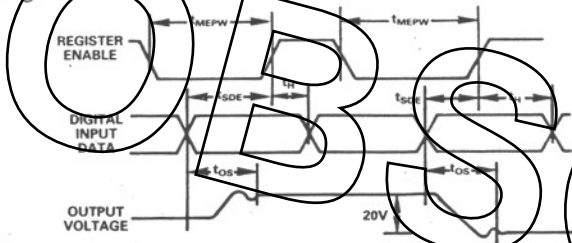
TIMING NOTES:

t_{MEPW} MINIMUM ENABLE PULSE WIDTH IS 60ns.

t_{SDE} MINIMUM SETUP TIME DIGITAL INPUT DATA TO ENABLE IS 40ns.

t_H HOLD TIME IS DEFINED AS THE REQUIRED DELAY BETWEEN THE LEADING EDGE OF REGISTER ENABLE AND THE END OF VALID INPUT DATA. THE HOLD TIME IS ZERO FOR THE AD3860.

t_{OS} OUTPUT SETTLING TIME FOR A 20 VOLT CHANGE TO ±1/2LSB IS 7µs MAX.

Figure 4. Input Register Timing Diagram

8-BIT MICROPROCESSOR INTERFACE

Whenever a 12-bit DAC is loaded from an 8-bit bus, two write cycles are required. The organization most often used is "right justified." Right-justified data calls for the eight least significant bits to occupy one byte, with the four most significant bits residing in the lower half of another byte. This organization simplifies integer arithmetic. Figure 5 shows an addressing
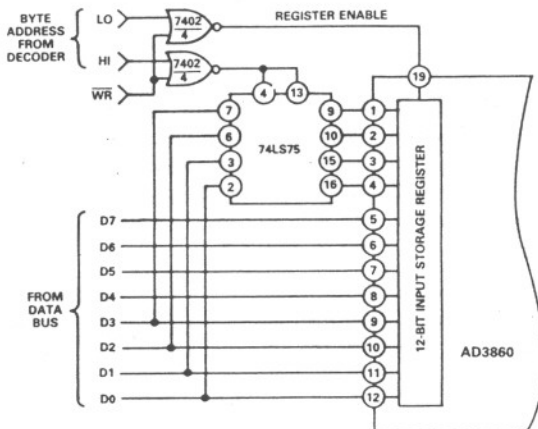
Figure 5. Right-Justified 8-Bit Bus Interface

scheme for the AD3860 set up for right justified data in an 8-bit system. The four MSBs are latched into the 74LS75 latch in the first write cycle. The entire 12-bit word is then loaded into the AD3860's internal input storage register on the next write cycle. An alternate scheme is to use an eight-bit intermediate register,

such as the 74LS373, to allow the user to load the lower order bits in the first write cycle.

Left-justified data can be similarly accommodated. The overlapping of data lines is reversed as shown in Figure 6. The AD3860
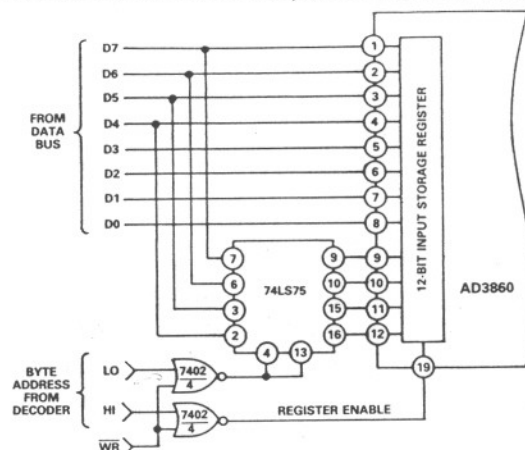
Figure 6. Left-Justified 8-Bit Bus Interface

still occupies two adjacent locations in the processor's memory map. A left-justified format is convenient in applications when the data represents a 12-bit binary fraction (between 0 and $\frac{4095}{4096}$).

Left-justified data has the four least significant bits in the upper half of the first byte and the eight most significant bits in the second byte. The four LSBs on the intermediate latch and the eight MSBs on the data bus are all latched into the AD3860 latch simultaneously. This double buffering technique avoids the analog output slewing to an undesirable state determined by the MSBs of the new digital data and the LSBs of the previous digital data.

Many of the popular microprocessor families include components specifically designed to ease the interface between the microprocessor and a peripheral device such as a converter. These components are called Programmable Peripheral Interface (PPI), Peripheral Interface Adaptor (PIA), Parallel I/O Controller (PIO), or similar names. They typically feature two or more 8-bit wide parallel data ports which can, under program control, be configured as either inputs or outputs. Their control signals are made compatible with the particular processor they serve, and in many systems can provide an attractive alternative to a collection of random logic. For example, the 8255 PPI has two 8-bit and two 4-bit ports which can be used as input, as output, or as a combination of input, output, and control. Each of the 4-bit words can be grouped with one of the 8-bit words so that the interface is split into two 12-bit ports. The ports can be set up as outputs, under program control, for controlling two AD3860s with a single PPI. The 8255 contains two bits of address input. That is, A0 and A1 of the 8255 are driven directly by the address bus, and these bits need not be used by the address decoder. Though the 8255 is an 8080 system component, it is adaptable to other µP systems.

USING THE AD3860 WITH 12- AND 16-BIT BUSES

The AD3860 is easily interfaced to 12- and 16-bit data buses. The AD3860's Register Enable signal can usually be derived by NANDing the desired address lines with the processor's MEMORY WRITE or I/O WRITE line. For most processors, valid data remains on the data bus for some time after either the valid address or control signals are removed. Therefore, the data is latched into the AD3860 immediately after one of the address or control signals changes but before valid data goes away. The AD3860 thus occupies a single memory location.