High Power Step-Down Synchronous DC/DC Controller

Features

- Operates from +5V Input
- 0.8V Internal Reference Voltage
  - ±1.5% Accuracy Over Line, Load and Temperature
- 0.8V to V_{CC} Output Range
- Full Duty Cycle Range
  - 0% to 100%
- Internal Loop Compensation
- Internal Soft-Start
  - Typical 2ms
- Programmable Over-Current Protection
  - Lossless Sensing Using MOSFET $R_{DS(ON)}$
- Under-Voltage Protection
- Drives External N-Channel MOSFETs
- Shutdown Control
- Small SOP-8 Package
- Lead Free and Green Devices Avaliable (RoHS Compliant)

Applications

- Motherboard
- Graphics Cards
- Cable or DSL Modems, Set Top Boxes
- DSP Supplies
- Memory Supplies
- 5V Input DC-DC Regulators
- Distributed Power Supplies

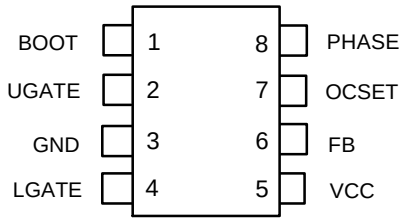
General Description

The APW7057 is a 300kHz constant frequency voltage mode synchronous switching controller that drives external N-channel MOSFETs. When the input supply drops close to output, the upper MOSFET remains on, achieving 100% duty cycle. Internal loop compensation is optimized for fast transient response, eliminating external compensation network. The precision 0.8V reference makes this part suitable for a wide variety of low voltage applications. Soft-start is internally set to 2ms, limiting the input in-rush current and preventing the output from overshoot during powering up.

The APW7057 has over current and short circuit protections. Over current protection is achieved by monitoring the voltage drop across the high side MOSFET, eliminating the need for a current sensing resistor and short circuit condition is detected through the FB pin. If either fault conditions occur, the APW7057 would initiate the soft-start cycle. After three cycles and if the fault condition persists, the controller will be shut down. To restart the controller, either recycle the V_{CC} supply or momentarily pull the OSCSET pin below 1.25V.

The APW7057 can be shutdown by pulling the OCSET pin below 1.25V. In shutdown, both gate drive signals will be low. The controller is available in a small SOP-8 package.

Pin Configuration



SOP-8 (Top View)

Ordering and Marking Information

APW7057 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-8 Operating Junction Temperature Range C : 0 to 70°C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APW7057 K : APW7057 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{BOOT}	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 15	V
	PHASE, OCSET to GND Input Voltage	-0.3 ~ 12	V
	FB to GND Input Voltage	-0.3 ~ VCC+0.3	V
	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air SOP-8	160	°C/W

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	5 ± 5%	V
V_{OUT}	Output Voltage of the Switching Regulator (Note)	0.8 ~ VCC	V
V_{IN}	Input Voltage of the Switching Regulator (Note)	3.3 ~ VCC	V
T_A	Ambient Temperature	0 ~ 70	°C
T_J	Junction Temperature	0 ~ 125	°C

Note : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=5V, V_{BOOT}=12V and T_A= 0~70 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7057			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Nominal Supply Current	UGATE and LGATE Open	-	2.1	-	mA
I_{BOOT}	BOOT Nominal Supply Current	UGATE Open	-	2.1	-	mA
UNDER VOLTAGE LOCKOUT (UVLO)						
	Rising VCC Threshold		4.0	4.2	4.4	V
	Falling VCC Threshold		3.8	4.0	4.2	V
OSCILLATOR						
F_{OSC}	Free Running Frequency		250	300	340	kHz
	Ramp Upper Threshold		-	2.85	-	V
	Ramp Lower Threshold		-	0.95	-	V
ΔV_{OSC}	Ramp Amplitude		-	1.9	-	VP-P
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.8	-	V
	Reference Voltage Accuracy		-1.5	-	+1.5	%
ERROR AMPLIFIER						
	DC Gain		-	75	-	dB
F_P	First Pole Frequency		-	10	-	Hz
F_Z	First Zero Frequency		-	1	-	kHz
	UGATE Duty Range		0	-	100	%
	FB Input Current		-	-	0.1	µA
PWM CONTROLLER GATE DRIVERS						
	UGATE Source	VUAGTE=1V	-	0.6	-	A
	UGATE Sink	VUGATE=1V	-	7.3	-	Ω
	LGATE Source	VLGATE=1V	-	0.6	-	A
	LGATE Sink	VLGATE=1V	-	1.8	-	Ω
T_D	Dead Time		-	50	-	nS
PROTECTION						
I_{OCSET}	OCSET Sink Current	VOCSET=4.5V	34	40	46	µA
UV_{FB}	FB Under-Voltage Level	FB falling	-	0.5	-	V
	FB Under-Voltage Hysteresis		-	15	-	mV

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CC}=5V, V_{BOOT}=12V and T_A= 0~70 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7057			Unit
			Min.	Typ.	Max.	
SOFT-START AND SHUTDOWN						
T_{SS}	Soft-Start Interval		-	2	-	mS
	Shutdown Threshold	VOCSET Falling	-	1.25	-	V
	OCSET Shutdown Hysteresis		-	20	-	mV

Function Pin Description

BOOT (Pin 1)

This pin provides the supply voltage to the high side MOSFET driver. A voltage no greater than 13V can be connected to this pin as a supply to the driver. For driving logic level N-channel MOSEFT, a bootstrap circuit can be use to create a suitable driver's supply.

UGATE (Pin 2)

This pin provides gate drive for the high-side MOSFET.

GND (Pin 3)

Signal and power ground for the IC. All voltage levels are measured with respect to this pin. Tie this pin to the ground plane through the lowest impedance connection available.

LGATE (Pin 4)

This pin provides the gate drive signal for the low side MOSFET.

VCC (Pin 5)

This is the main bias supply for the controller and its low side MOSFET driver. Must be closely decoupled to GND (Pin 3). **DO NOT** apply a voltage greater than 5.5V to this pin.

FB (Pin 6)

This pin is the inverting input of the error amplifier and it receives the feedback voltage from an external resistive divider across the output (V_{OUT}). The output voltage is determined by:

$$V_{OUT} = 0.8V(1+\frac{R_{OUT}}{R_{GND}})$$

where ROUT is the resistor connected between VOUT and FB while RGND is the resistor connected from FB to GND.

OCSET (Pin 7)

This pin serves two functions: as a shutdown control and for setting the over current limit threshold. Pulling this pin below 1.25V shuts the controller down, forcing the UGATE and LGATE signals to be at 0V. A soft-start cycle will be initiated upon the release of this pin.

A resistor (R_{ocset}) connected between this pin and the drain of the high side MOSFET will determine the over current limit. An internally generated 40µA current source will flow through this resistor, creating a voltage drop. This voltage will be compared with the voltage across the high side MOSFET. The threshold of the over current limit is therefore given by:

$$I_{OI} = \frac{40uA \times R_{OCSET}}{R_{DS(ON)}}$$

An over current condition will cycle the soft-start function. After three consecutive cycles and if the fault condition persists, the controller will be shut down. To restart the controller, either recycle the V_{CC} supply or momentarily pull the OSCSET pin below 1.25V.

PHASE (Pin 8)

This pin is connected to the source of the high-side MOSFET and is used to monitor the voltage drop across the high-side MOSFET for over-current protection.

Block Diagram

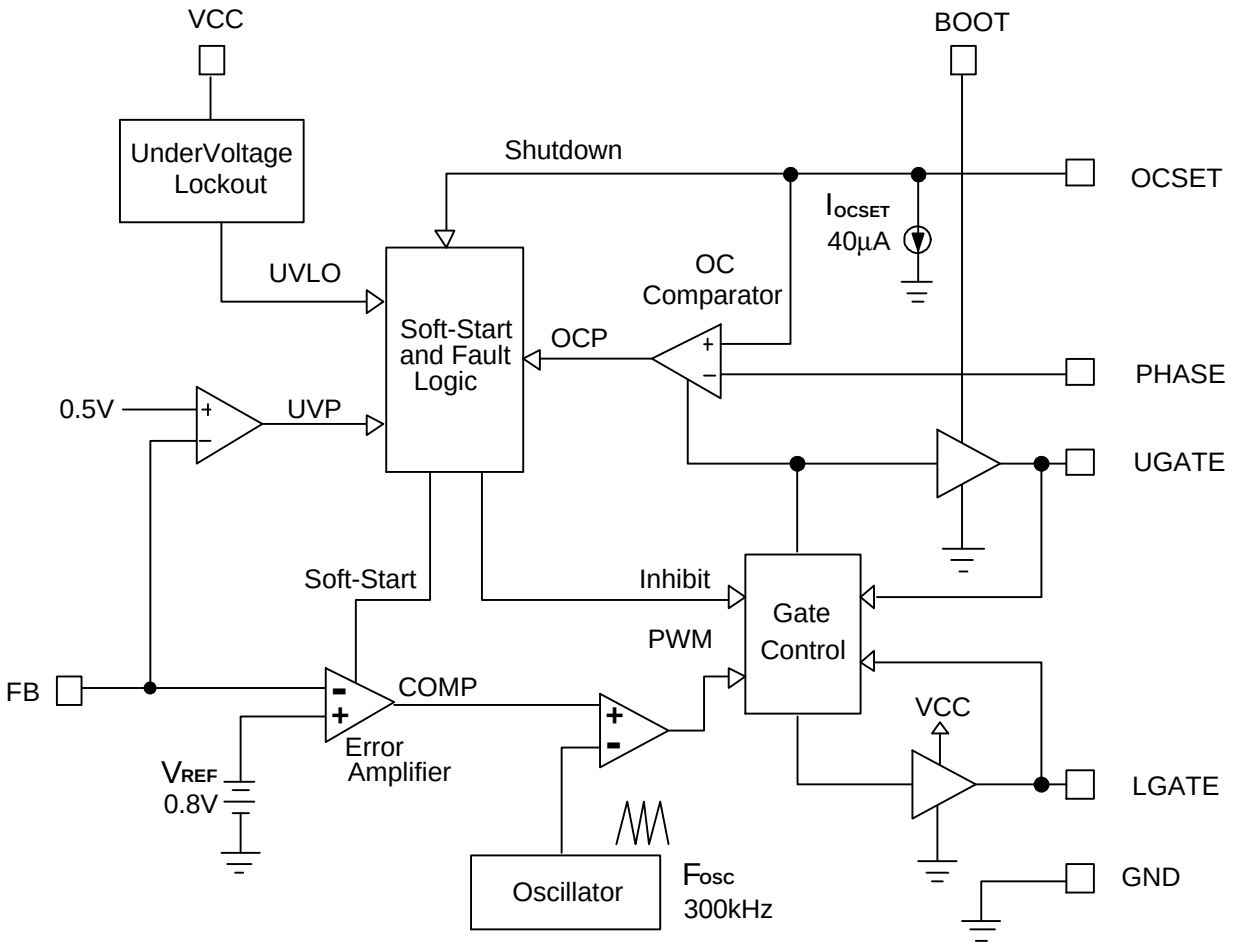
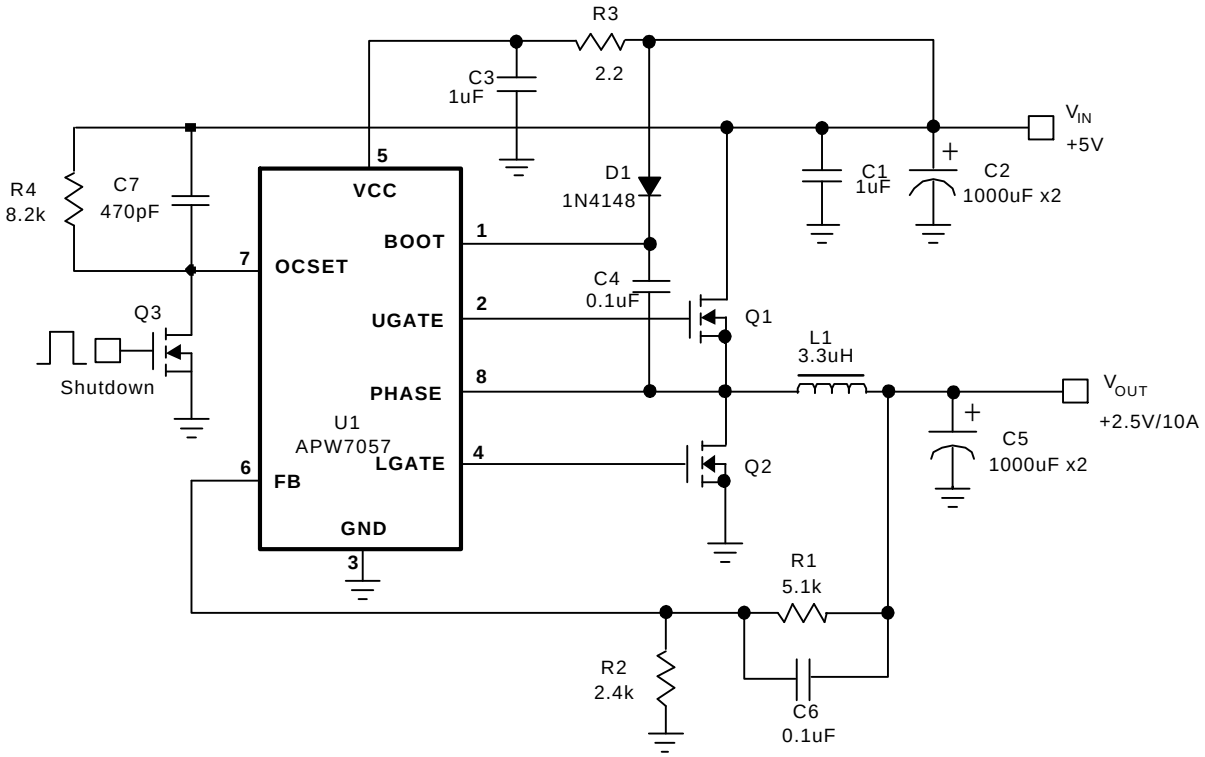


Figure 1.

Typical Application Circuit



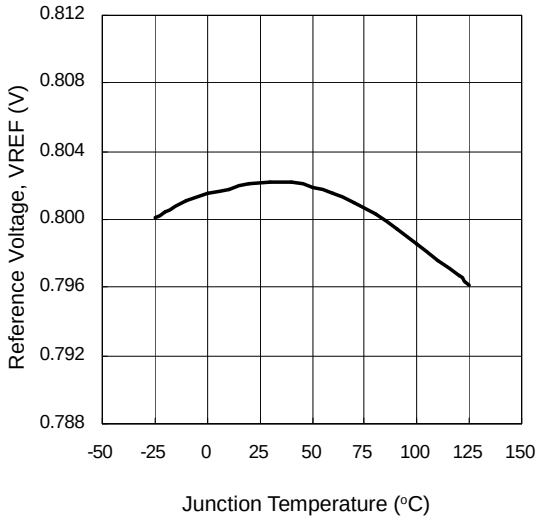
Q1: APM2014N UC
Q2: APM2014N UC
Q3: 2N7002

C2: 1000uF/10V, ESR = 25mΩ
C5: 1000uF/6.3V, ESR = 25mΩ

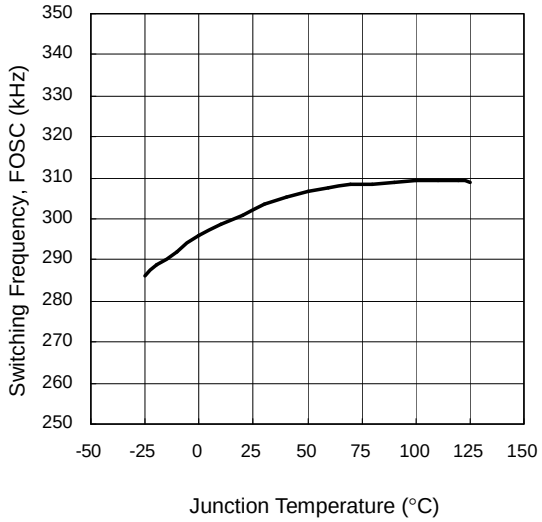
Figure 2.

Typical Operating Characteristics

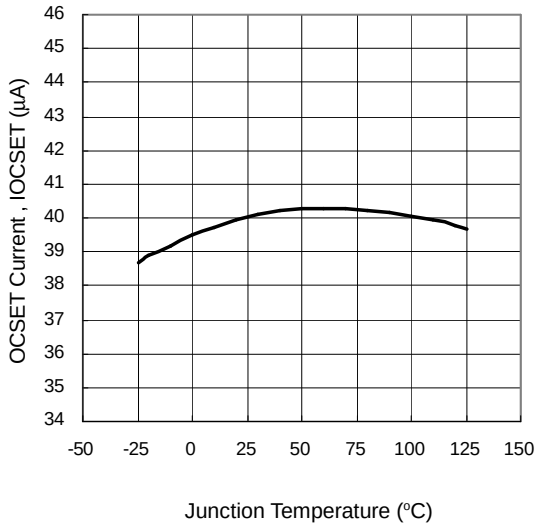
Reference Voltage vs. Junction Temperature



Switching Frequency vs. Junction Temperature



OCSET Current vs. Junction Temperature

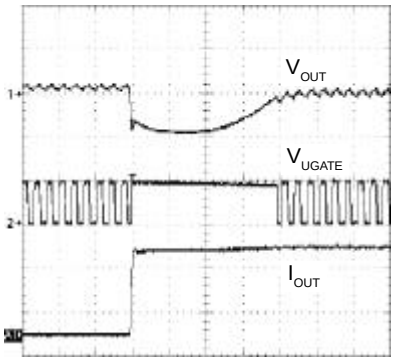


Operating Waveforms (Refer to the typical application circuit)

1. Load Transient Response : I_{OUT} = 0A -> 10A -> 0A

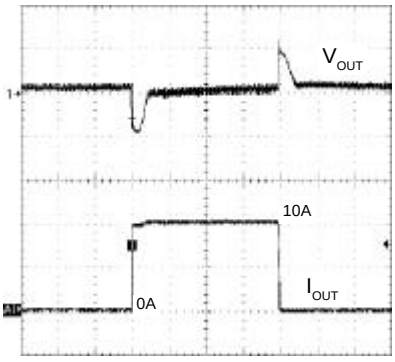
- I_{OUT} slew rate = ±10A/µS

I_{OUT} = 0A -> 10A



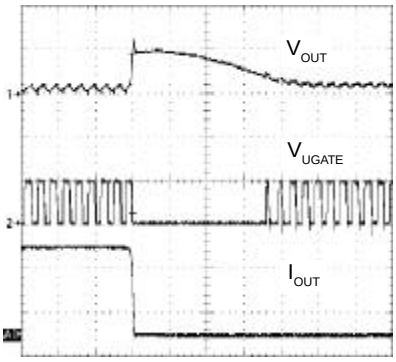
Ch1 : V_{OUT}, 100mV/Div, DC,
Offset = 2.50V
Ch2 : V_{UGATE}, 10V/Div, DC
Ax1 : I_{OUT}, 5A/Div
Time : 10µS/Div
BW = 20MHz

I_{OUT} = 0A -> 10A -> 0A



Ch1 : V_{OUT}, 100mV/Div, DC,
Offset = 2.50V
Ax1 : I_{OUT}, 5A/Div
Time : 100µS/Div
BW = 20MHz

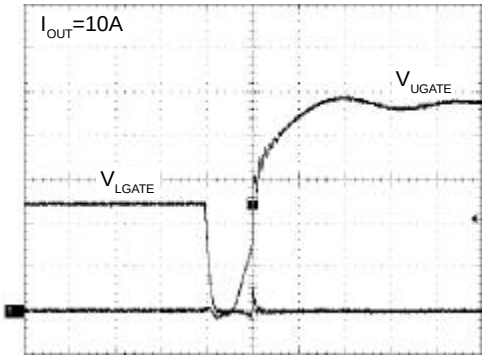
I_{OUT} = 10A -> 0A



Ch1 : V_{OUT}, 100mV/Div, DC,
Offset = 2.50V
Ch2 : V_{UGATE}, 10V/Div, DC
Ax1 : I_{OUT}, 5A/Div
Time : 10µS/Div
BW = 20MHz

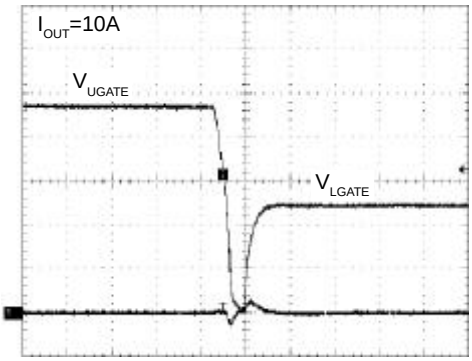
2. UGATE and LGATE

UGATE Rising



Ch1 : V_{UGATE}, 2V/Div, DC
Time : 125nS/Div
Ch2 : V_{LGATE}, 2V/Div, DC
BW = 500MHz

UGATE Falling



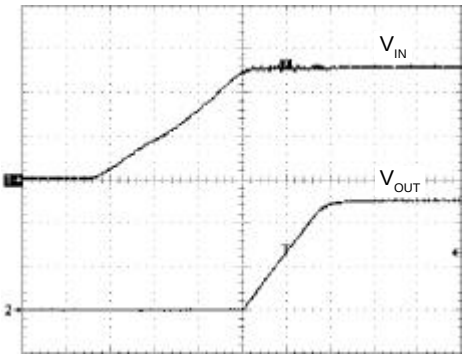
Ch1 : V_{UGATE}, 2V/Div, DC
Time : 125nS/Div
Ch2 : V_{LGATE}, 2V/Div, DC
BW = 500MHz

Operating Waveforms (Cont.)

(Refer to the typical application circuit)

3. Powering ON / OFF

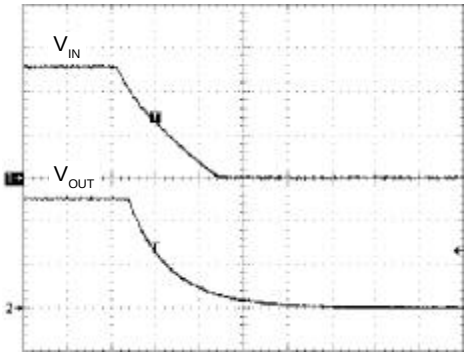
Soft-Start at Powering ON



Ch1 : V_{IN}, 2V/Div, DC
Time : 1mS/Div

Ch2 : V_{OUT}, 1V/Div, DC
BW = 20MHz

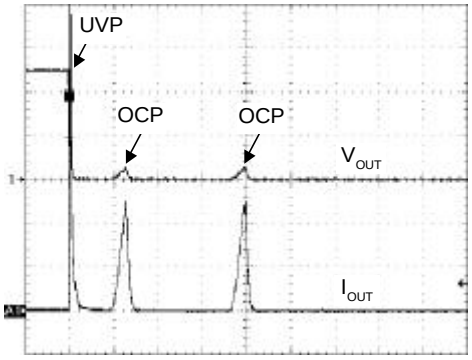
Powering OFF



Ch1 : V_{IN}, 2V/Div, DC
Time : 5mS/Div

Ch2 : V_{OUT}, 1V/Div, DC
BW = 20MHz

4. Short-Circuit Protection



Under-Voltage (UVP)
and Over-Current Protection (OCP)

Ch1 : V_{OUT}, 1V/Div, DC
Ax1 : I_{OUT}, 10A/Div
Time : 1mS/Div
BW = 20MHz

Application Information

Component Selection Guidelines

Output Capacitor Selection

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore, select high performance low ESR capacitors that are intended for switching regulator applications. In some applications, multiple capacitors have to be paralled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

For high frequency decoupling, a ceramic capacitor between 0.1µF to 1µF can be connected between V_{CC} and ground pin.

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

where Fs is the switching frequency of the regulator.

There is a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa.

The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement.The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$$P_{UPPER} = I_{out}^2 (1+ TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_S$$

$$P_{LOWER} = I_{out}^2 (1+ TC)(R_{DS(ON)})(1-D)$$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{sw} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET includes an additional transition loss. The switching internal, t_{sw}, is the function of the reverse transfer capacitance C_{RSS}. Figure 3 illustrates the switching waveform internal of the MOSFET.

Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedances should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. Figure 4 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together.

Application Information

Layout Consideration (Cont.)

Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- Decoupling capacitor C_{IN} provides the bulk capacitance and needs to be placed close to the IC since it will provide the MOSFET drivers transient current requirement.
- The ground return of C_{IN} must return to the combine C_{OUT} (-) terminal.
- Capacitor C_{BOOT} should be connected as close to the BOOT and PHASE pins as possible.
- Capacitor C_{HF} is to improve noise performance and a small 1µF ceramic capacitor will be sufficient.

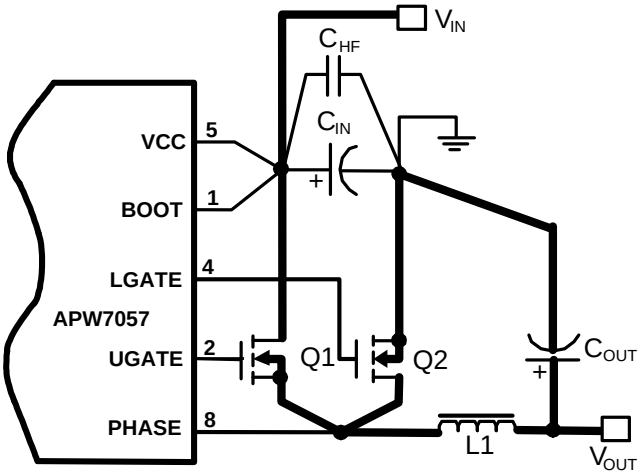


Figure 4. Recommended Layout Diagram

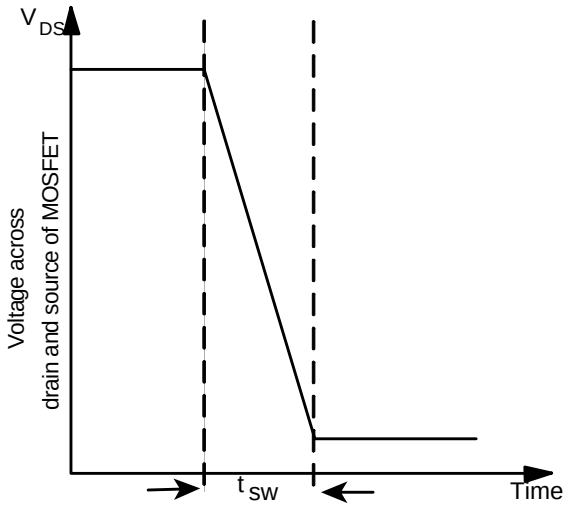
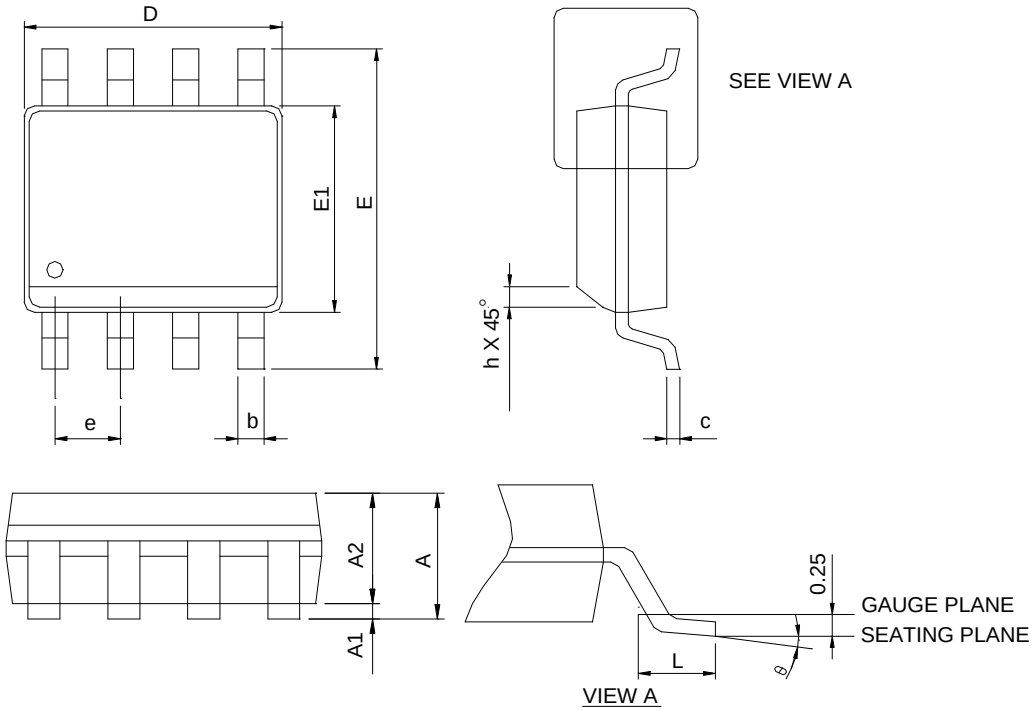


Figure 3. Switching waveform across MOSFET

Package Information

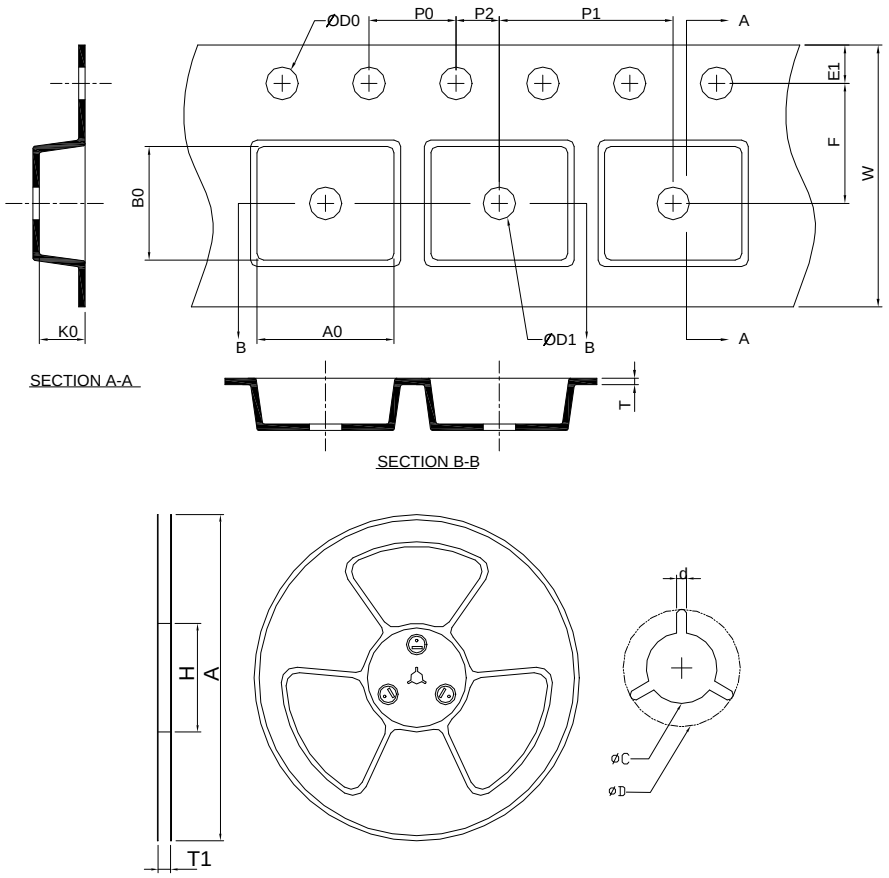
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



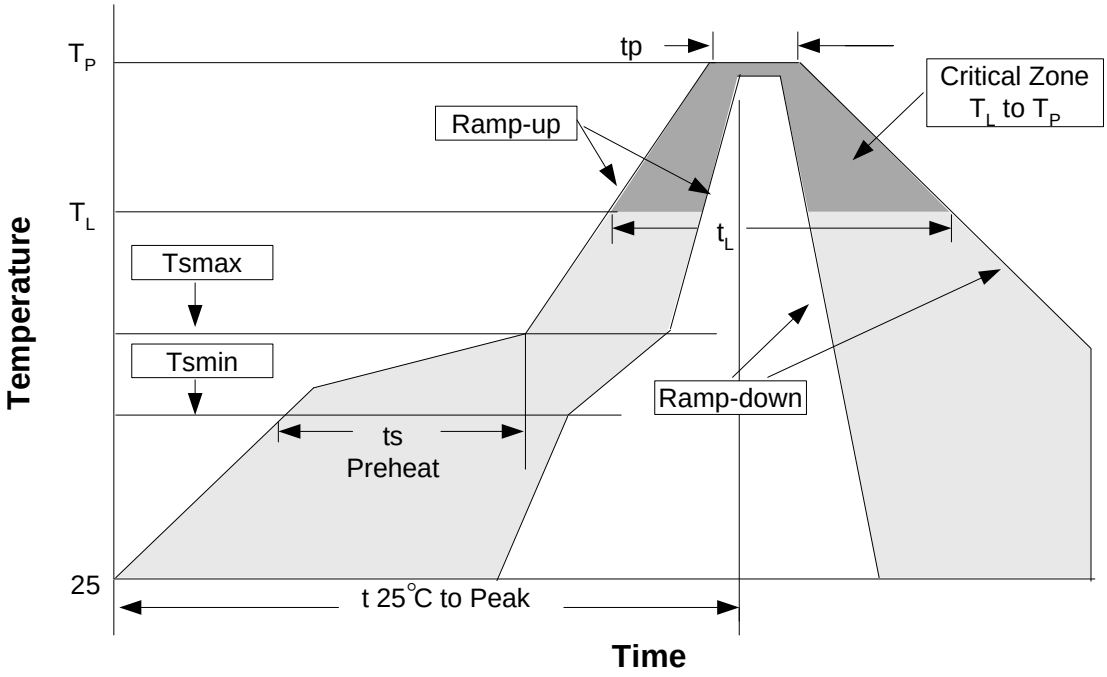
Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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