HFC0100

QUASI RESONANT CONTROLLER

The Future of Analog IC Technology

DESCRIPTION

The HFC0100 is a peak current mode controller with Green Mode Operation. Its high efficiency feature over the entire line and load range meets the stringent world-wide energy efficiency requirements.

The HFC01 00 integrate d with a high voltage current sou rce, its valley detector ensures minimum Drain-Source voltage switching (Quasi-Resonant oper ation). Whe n the outpu t power falls below a given level, the controller enters the burst mode.

The HFC0100 features variable protections like Thermal Sh utdown (TSD), Vcc Un der voltage Lockout (UVLO), Over Load Protection (OLP), Over Voltage Protection (OVP).

The HF C0100 is a vailable in th e 8-p in SOI C8 package.

FEATURES

- Universal Main Input Voltage (85~265VAC)
- Quasi-Resonant Operation
- Valley Switching for high efficiency and EMI
- Active Burst Mode for low standby powe r consumption
- Internal High Voltage Current Source
- High level of integration , allows a very low number external component count
- Maximum Frequency Limited
- Internal Soft Start
- Internal 250nS Leading Edge Blanking
- Thermal shutdown (auto resta rt with hysteresis)
- Vcc Under Voltage Lockout with Hysteresis (UVLO)
- Over Voltage Protection
- Over Load Protection.

APPLICATIONS

- Battery ch arger: cellular phone, digital camera, video camera, electrical shaver, emergency lighting system, etc
- Standby power supply: CRT-TV, Projection-TV, LCD-TV, PDP-TV, Desk top PC, Audio system, etc
- SMPS: Inc jet printer, DVD player/recorder, VCR, CD player, Set top box, Air conditioner, refrigerator, washing machine, dish washer, Adapter for NB, etc

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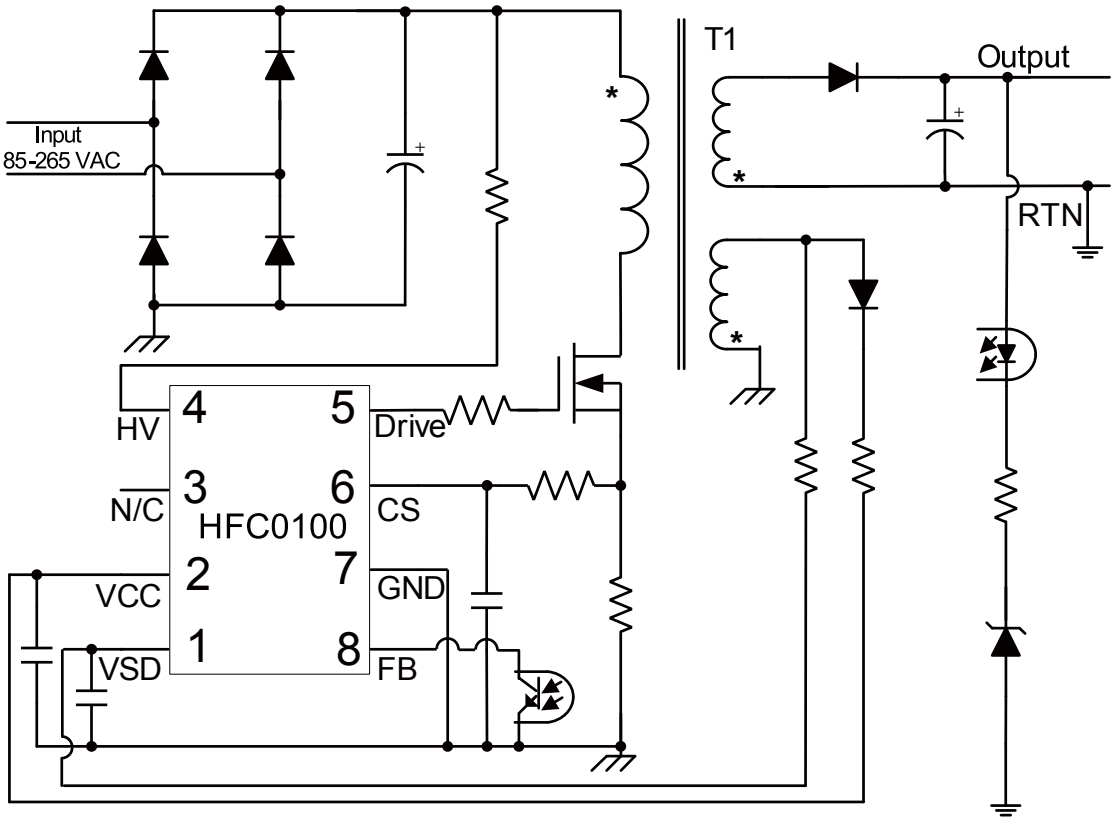
TYPICAL APPLICATION

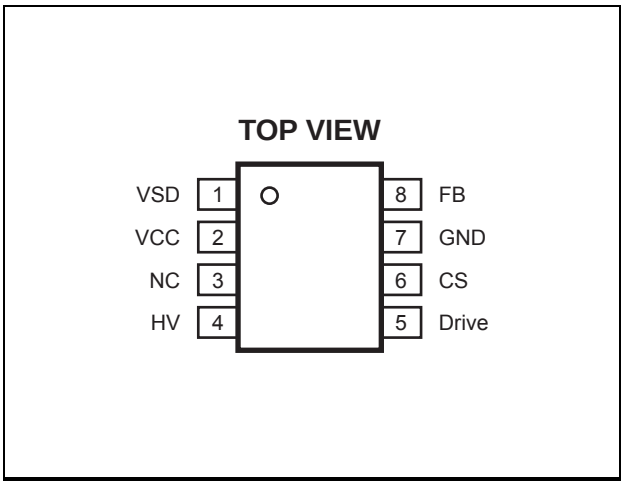


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
HFC0100HS	SOIC8	HFC100	-40°C to +125°C

*For Tape & Reel, add suffix –Z (e.g. HFC0100HS–Z);
For RoHS compliant packaging, add suffix –LF (e.g. HFC0100HS–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

HV Break Down Voltage ..... -0.7V to 700V
Vcc, DRV to GND .....-0.3V to 22V
FB, CS, VSD to GND .....-0.3V to 7V
Continuous Power Dissipation…(T_A = +25°C) (2)
……....1.3W
Junction Temperature .....150°C
Thermal Shut Down .....150°C
Thermal Shut Down Hysteresis .....50°C
Lead Temperature .....260°C
Storage Temperature ..... -60°C to +150°C
ESD Capability Human Body Model (All Pins except HV) 2.0kV
ESD Capability Machine Model 200V

Recommended Operation Conditions (3)

Operating Vcc range .....8V to 20V
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8 .....96 ..... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERICS

For typical value T_J=25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-up Current Source (Pin HV)						
Charging current from Pin HV	I_{charge}	Vcc=6V;V_{HV}=400V	1.4	2	2.6	mA
Leakage current from Pin HV	I_{leak}	With auxiliary supply; V_{HV}=400V, Vcc=13V	--	20	--	μA
Break Down Voltage	V_{BR}		700	--	--	V
Supply Voltage Management (Pin Vcc)						
Vcc Upper Level at which the Intern al High Voltage Current Source Stops	V_{CCH}		10.6	11.8	13	V
Vcc Lower Level at which the Internal High Voltage Current Source Triggers	V_{CCL}		7.2	8	8.8	V
Vcc Re -charge Level at which the protection occurs	Vccp		--	5.5	--	V
Internal IC Consumption, 1nF Load on Drive Pin,	Icc1	Fs=100kHz, Vcc=12V	-- 2.0		--	mA
Internal IC Consumption, Latch off phase,	Icc2 VCC=6V		--	450	--	μA
Feedback Management (Pin FB)						
Internal Pull Up Resistor	R_{FB}		--	10	--	kΩ
Internal Pull Up Voltage	Vup		--	4.5	--	V
FB Pin to Current Limit Division Ratio	I_{div}		--	3	--	--
Internal Soft-Start Time	Tss		--	2.4	--	mS
FB Decrea sing Level at which the controller enter the Burst Mode	V_{BURL}		--	0.5	--	V
FB Increa sing Level at which the controller leave the Burst Mode	V_{BURH}		--	0.7	--	V
Over Load Set Point	V_{OLP}		--	3.7	--	V
Valley Switching Management (Pin VSD)						
Valley Switching Threshold Voltage	V_{VSD}		40	55	70	mV
Valley Switching Hysteresis	V_{hys}		--	10	--	mV
Pin VSD Clamp Voltage	V_{VSDH}	High State; Ipin2=3.0mA	7 7.5 8			V
	V_{VSDL}	Low State; Ipin2=-2.0mA	-0.8 -0.65		-0.5	
Valley Switching Propagation Delay	T_{VSD}	Pull down from 2V to -100mV	120 160		200	nS
Minimum Off Time	T_{min}		6.6	7.8	9	μS
Re-start time After Las t Valley detec t Transition	$T_{restart}$		--	4.6	--	μS
OVP Sampling Delay	T_{OVPS}		--	3.5	--	μS
Pin VSD OVP reference level	V_{OVP}		--	6	--	V
Internal Impedance	Rint		--	24	--	kΩ
Current Sampling Management (Pin CS)						
Leading Edge Blanking	T_{LEB}		--	250	--	nS
Driving Signal (Pin DRIVE)						
Sourcing Resistor	R_H		--	17	--	Ω
Sinking Resistor	R_L		--	7	--	Ω

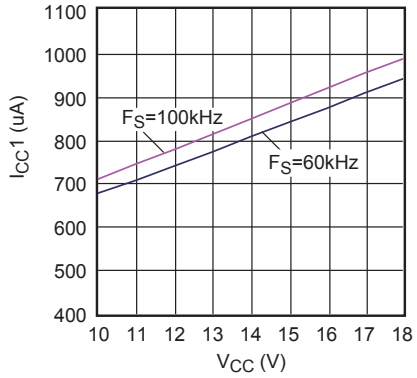
PIN FUNCTIONS

Pin #	Name	Description
1	VSD	Input from the auxiliary flyback signal, it ensures discontinuous operation and valley switching. It also offers a fixed OVP detection.
2	VCC	Supply voltage Pin. This pin is connected to an external bulk capacitor of typically 22uf and a ceramic capacitor of typically 0.1uF.
3	N/C	This Pin ensures adequate creepage distance.
4	HV	Input for the start up current unit.
5	Drive	Output of the driving signal.
6	CS	Input of the current sense.
7	GND	Ground.
8	FB	The Pin sets the peak current limit, by connecting an optocoupler to this Pin. A feedback voltage of 3.7V will trigger an over load protection, and a feedback voltage of 0.5V will trigger a burst mode operation.

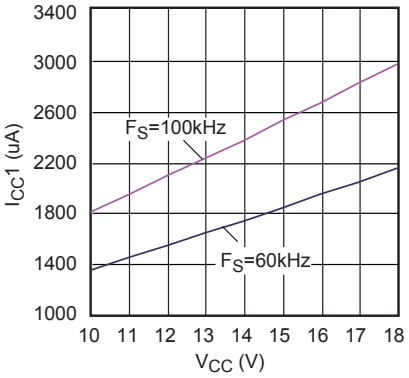
TYPICAL PERFORMANCE CHARACTERISTICS

T_A=25℃

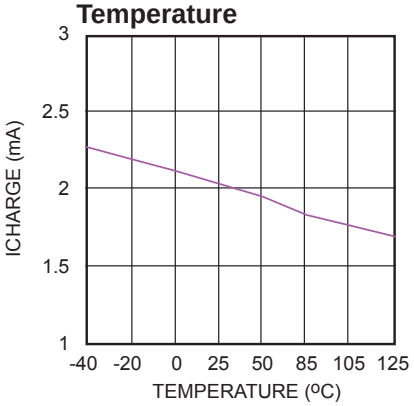
IC Consumption Vs Vcc (No Output Load)



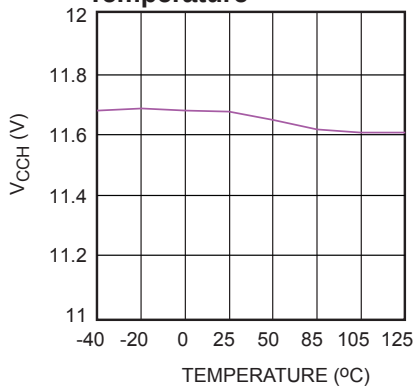
IC Consumption Vs Vcc (1nF Output Load)



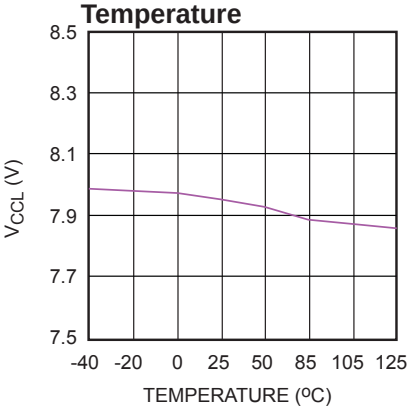
Charging Current From Pin HV (Vcc=6V, VHV=400V) Vs Temperature



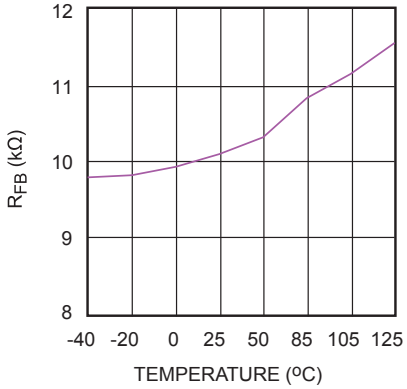
Vcc Upper Level at which the Internal High Voltage Current Source Stops Vs Temperature



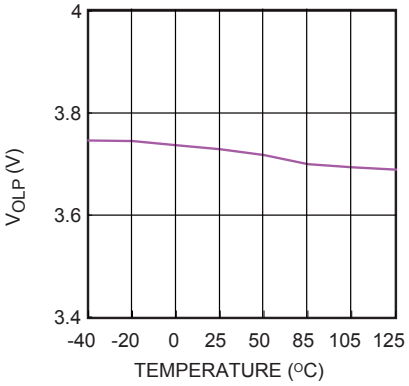
Vcc Lower Level at which the Internal High Voltage Current Source Triggers Vs Temperature



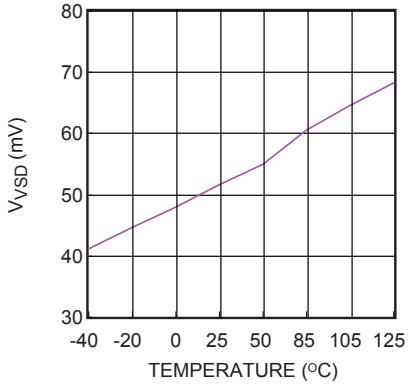
Pin FB Internal Pull Up Resistor Vs Temperature



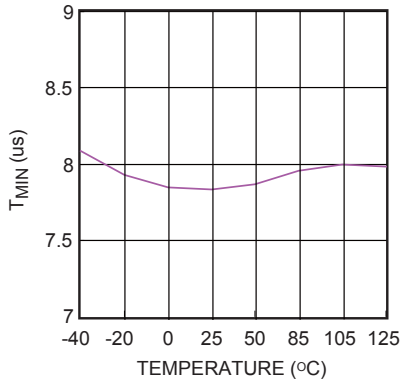
Over Load Set Point Vs Temperature



Valley Switching Threshold Voltage Vs Temperature



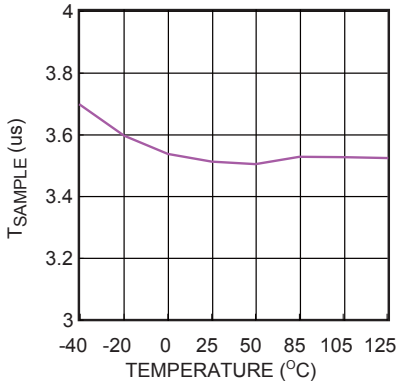
Minimum Off Time Vs Temperature



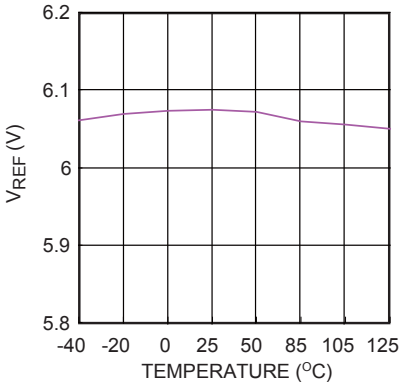
TYPICAL PERFORMANCE CHARACTERISTICS *(continues)*

T_A=25℃

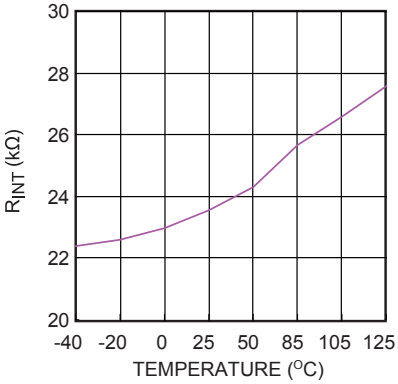
OVP Sampling Delay Vs Temperature



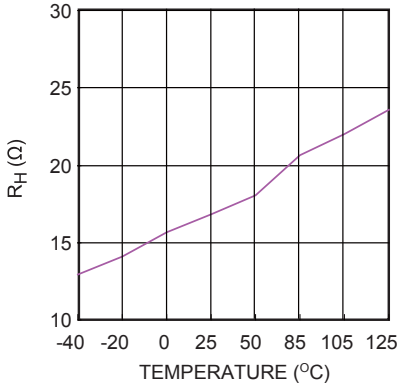
Pin VSD OVP reference level Vs Temperature



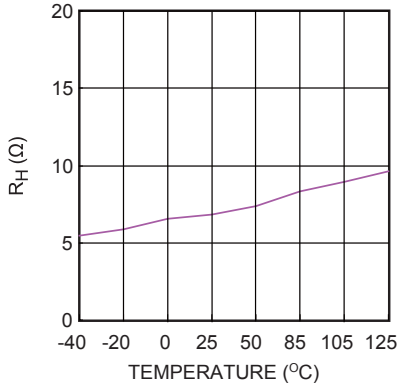
Pin VSD Internal Impedance Vs Temperature



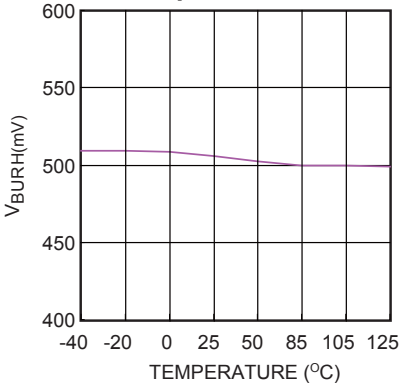
Sourcing Resistor Vs Temperature



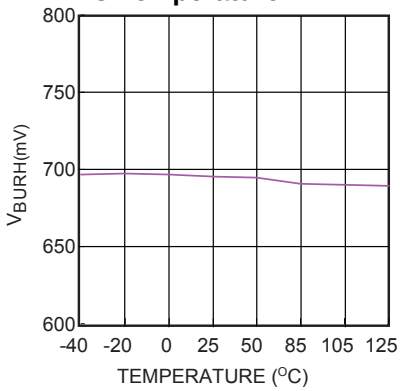
Sinking Resistor Vs Temperature



FB Decreasing Level at which the controller enter the Burst Mode Vs Temperature



FB Increasing Level at which the controller leave the Burst Mode Vs Temperature



BLOCK DIAGRAME

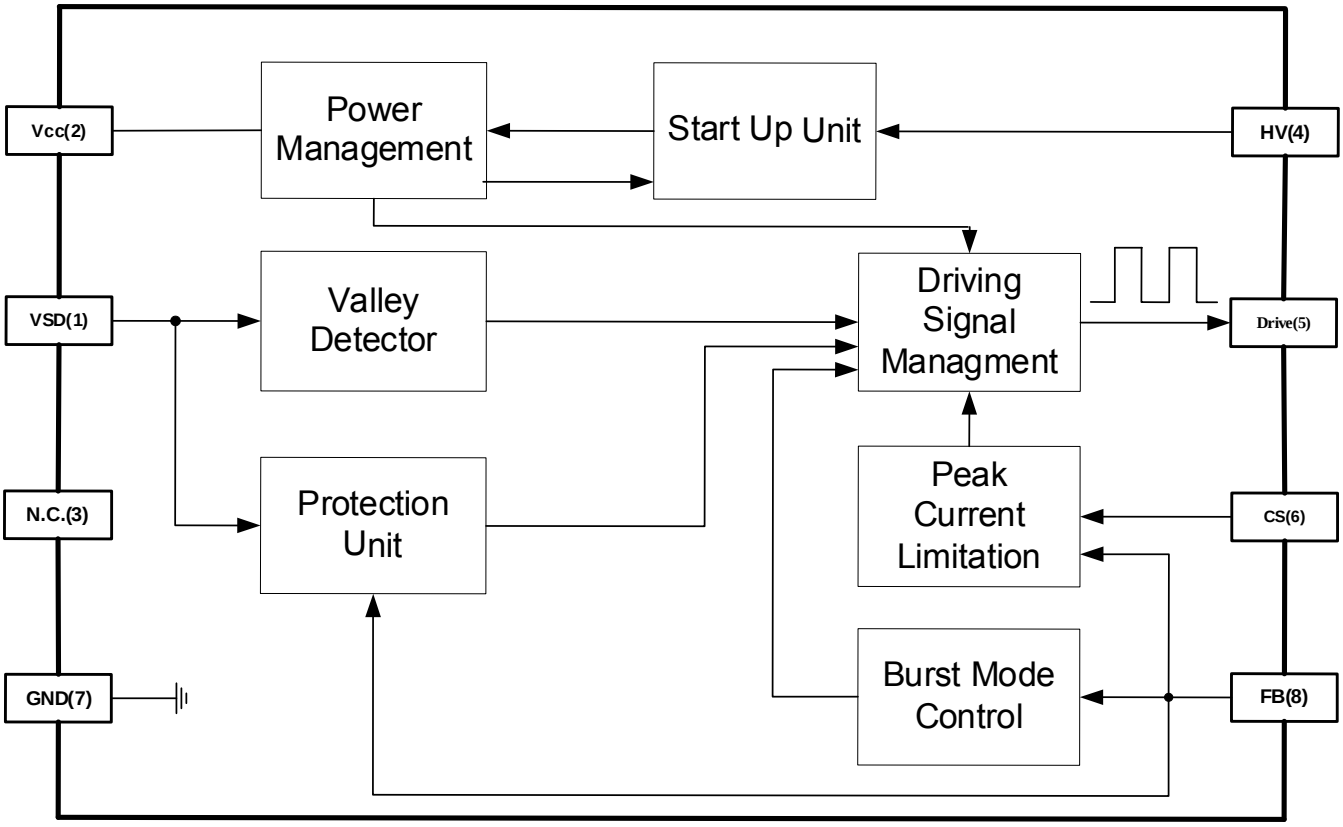


Figure 1— Block Diagram

OPERATION

The HFC0100 incorp orates all t he necessa ry features needed to a reliable Switch Mode Power Supply. Its valley det ector ensur es minimu m Drain-Source voltage switching (Q uasi-Resonant operation). When the o utput power falls be low a given level, the regulato r enters the burst mode. An internal minimu m off time limiter prevents the free running frequency to exceed 150kHz.

Start-Up

Initially, the IC is self su pplying from the internal high voltag e current source unit which drawn from the HV pin.

The IC starts switchin g and the internal hig h voltage current source unit is stopped as soon as the voltage on Pin Vcc reaches t he threshold V_{CCH}—11.8V.

Before the supply is ta ken over by the auxiliar y winding of the transfor mer, the Vcc capa citor supplies HFC0100 to maintain Vcc.

Quasi-Resonant Operation

The HFC0100 opera tes in Discontinuous Conduction Mode (DCM). The valley detector ensures minimum Drain-Source voltage switching (Quasi-Resonant operation)

As a result, there are virtually no primary s witch turn on losses and no secondary diode recovery losses. It ensures the reduction of the EMI noise.

Figure2 shows the valley detector unit.

When the voltage:

$$(V_{DS} - V_{in}) \times \frac{N_{aux}}{N_{pri}} \times \frac{24k\Omega}{4k\Omega + R_{VSD}} \quad 55mV$$

V_{DS} —Drain Source Voltage of the primary FET

V_{IN}—Input Voltage

N_{aux} —Auxiliary Winding Turns of the transformer

N_{pri} —Primary Winding Turns of the transformer

The valley detector se nds out a valley signal to turn on the primary FET.

Figure3 shows a typi cal drain source voltage waveform with valley switching.

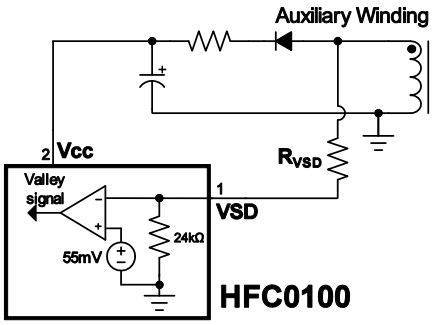


Figure 2—Valley Detector

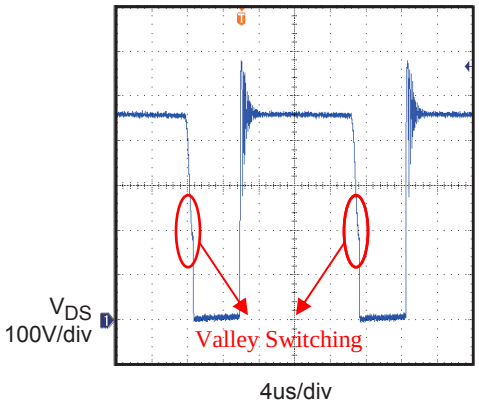


Figure 3—Valley Switching

To ensure the switching frequency below the EN55022 start limit---150kHz, HFC0100 employs an internal minimum off time limiter---7.8μS, shows as figure 4.

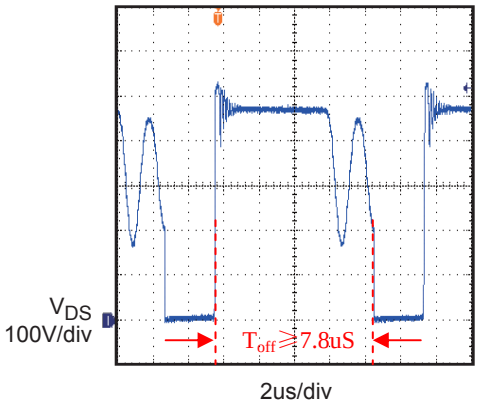


Figure 4—Minimum Off Time Limit

V_{CC} Under-Voltage Lock-out

When the Vcc below the UVLO threshold-8V, the HFC0100 stops switching and the internal high voltage current source unit re-starts, the Vcc external bulk capacitor is re-charged by it.

Figure 5 shows the typical waveform with Vcc under voltage lock out.

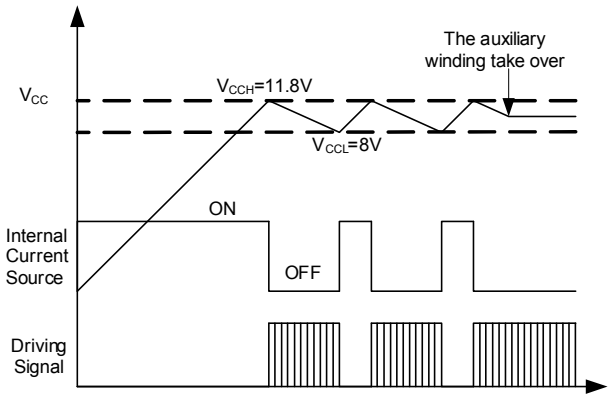


Figure 5—Vcc Under-Voltage Lock Out

Over-Voltage Protection (OVP)

The positive plateau of auxiliary winding voltage is proportional to the output voltage, the OVP use the auxiliary winding voltage instead of directly monitoring the output voltage.

The Figure 6 shows the OVP sample unit.

If the voltage:

$$V_O \times \frac{N_{aux}}{N_{SEC}} \times \frac{24k\Omega}{24k\Omega + R_{VSD}} > 6V$$

V_O—Output voltage

N_{aux}—Auxiliary Winding Turns of the transformer

N_{SEC}—Secondary Winding Turns of the transformer

The OVP circuit is triggered, and the HFC0100 stops the switching cycle and goes into latched fault condition. The controller stays fully latched in this position until the Vcc is decreased down to 3V, e.g. when the user unplugs the power supply from the main supply and re-plugs it.

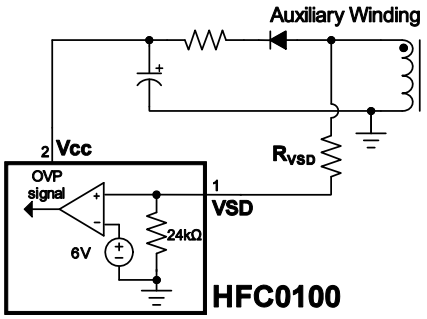


Figure 6—OVP Sample Unit

To avoid the mis-trigger due to the oscillation of the leakage inductance and the parasitic capacitance, the OVP sampling has a T_{OVPS} blanking, typical 3.5μS, shows as Figure 7.

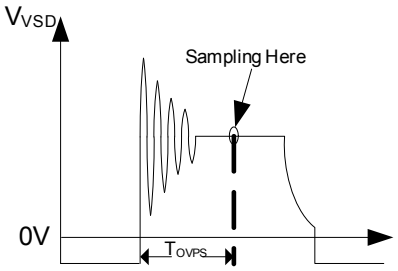


Figure 7

Over Load Protection (OLP)

The maximum output power is limited by the maximum switching frequency and maximum primary peak current. If the output consumes more than the maximum output power, the output voltage is drawn below the set point, this reduces the current through the optocoupler LED, which also reduces the transistor current, thus increases the FB voltage.

By continuously monitoring the Pin FB voltage, when the feedback voltage exceeds the threshold V_{OLP}—3.7V, it shuts off the switching cycle. The HFC0100 enters a safe low power operation that prevents from any lethal thermal or stress damage. As soon as the default disappears, the power supply resumes operation.

During the start up or load transient, the FB voltage will be high enough temporarily to mis-trigger the OLP, to prevent this undesired protection, OLP circuit is designed to be triggered after Vcc is decreased below 8.5V.

Burst Operation

To minimize the power dissipation in no load or light load, the HFC0100 enters the burst mode operation. As the load decreases, the FB voltage decreases,, the HFC0100 stops the switching cycle when the FB voltage drops below the threshold V_{BURL}—0.5V. And the output voltage starts to drop at a rate dependent on the load. This causes the FB voltage to rise again. Once the FB voltage exceeds the threshold V_{BURH}—0.7V, switching resumes. The FB voltage then falls and rises repeatedly. The burst mode operation alternately enables and disables switching cycle of the MOSFET thereby reducing switching loss in the no load or light load conditions.

Figure 8 shows the typical FB and Drive waveform during the burst mode.

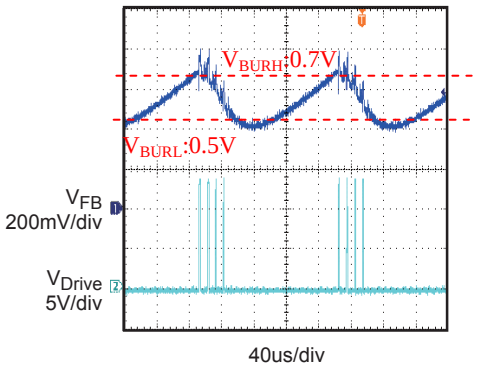


Figure 8—Burst Mode

Thermal Shutdown (TSD)

To prevents from any lethal thermal damage. The HFC0100 shuts down switching cycle when the inner temperature exceeds 150DegC. As soon as the inner temperature drops below 100DegC, the power supply resumes operation.

Soft-Start

To reduce the stress on primary MOSFET and secondary diode during start up, to smoothly establish the output voltage, the HFC0100 has an internal soft-start circuit that increases the current comparator inverting input voltage, together with the MOSFET current, slowly after it starts up. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors.

Current Limit Setting

The switch current is sensed by the resistor series between the Source of the FET and the ground. And the current limit is determined by the FB signal, $V_{Limit} = \frac{V_{FB}}{I_{div}} = \frac{V_{FB}}{3}$. To limit the maximum output power, the current limit is clamped at 1V when V_{FB} is bigger than 3.3V.

Leading Edge Blanking

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading edge blanking (LEB) unit is employed between the CS Pin and the current comparator input. During the blanking time, the path, CS Pin to the current comparator input, is blocked. Figure 9 shows the leading edge blanking.

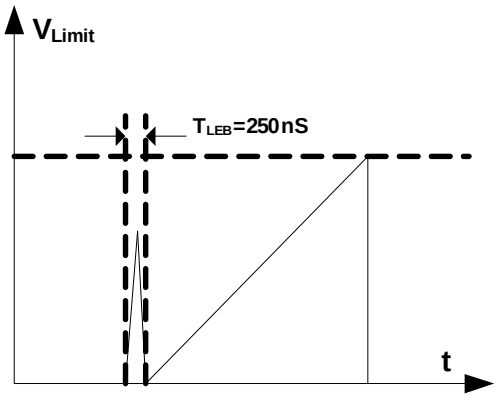


Figure 9—Leading Edge Blanking

Over Power Compensation

In the case of current sensing, shows as figure 10, the turn off of the FET is delayed due to the propagation delay of the control circuit, the delay time is the inherent characteristic of the control circuit, so T_{delay} can be seen fixed. This delay will cause an overshoot of the peak current. △I2 is bigger than △I1 due to the bigger rising ratio(the higher input voltage, the bigger rising ratio).

The propagation delay is done by means of the feedforward resistor, shown as Figure 1 1. Through this method, a dding one o ffset voltage at CS pin (the higher input voltage, the big ger offset voltage.).

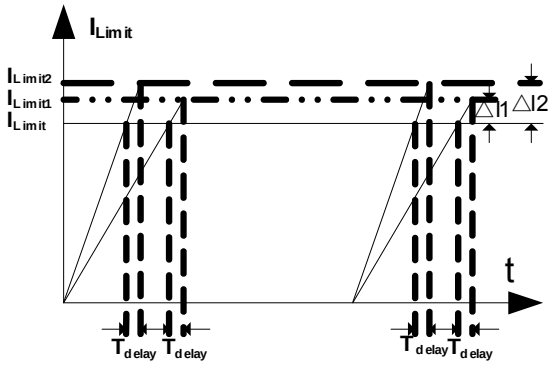


Figure 10—Propagation delay of the current limit

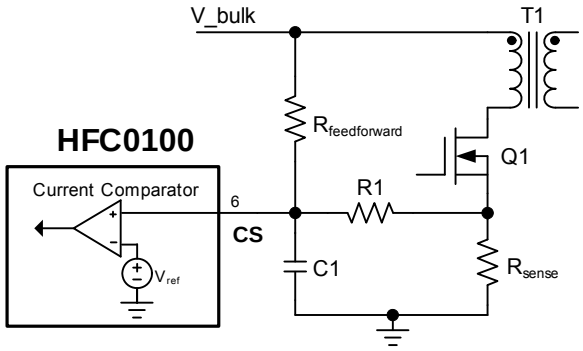


Figure 11—Over Power Compensation

Figure 12 shows the HFC0100 control flow chart.

Figure 13 shows the H FC0100 evolution of th e signals in presence of faults

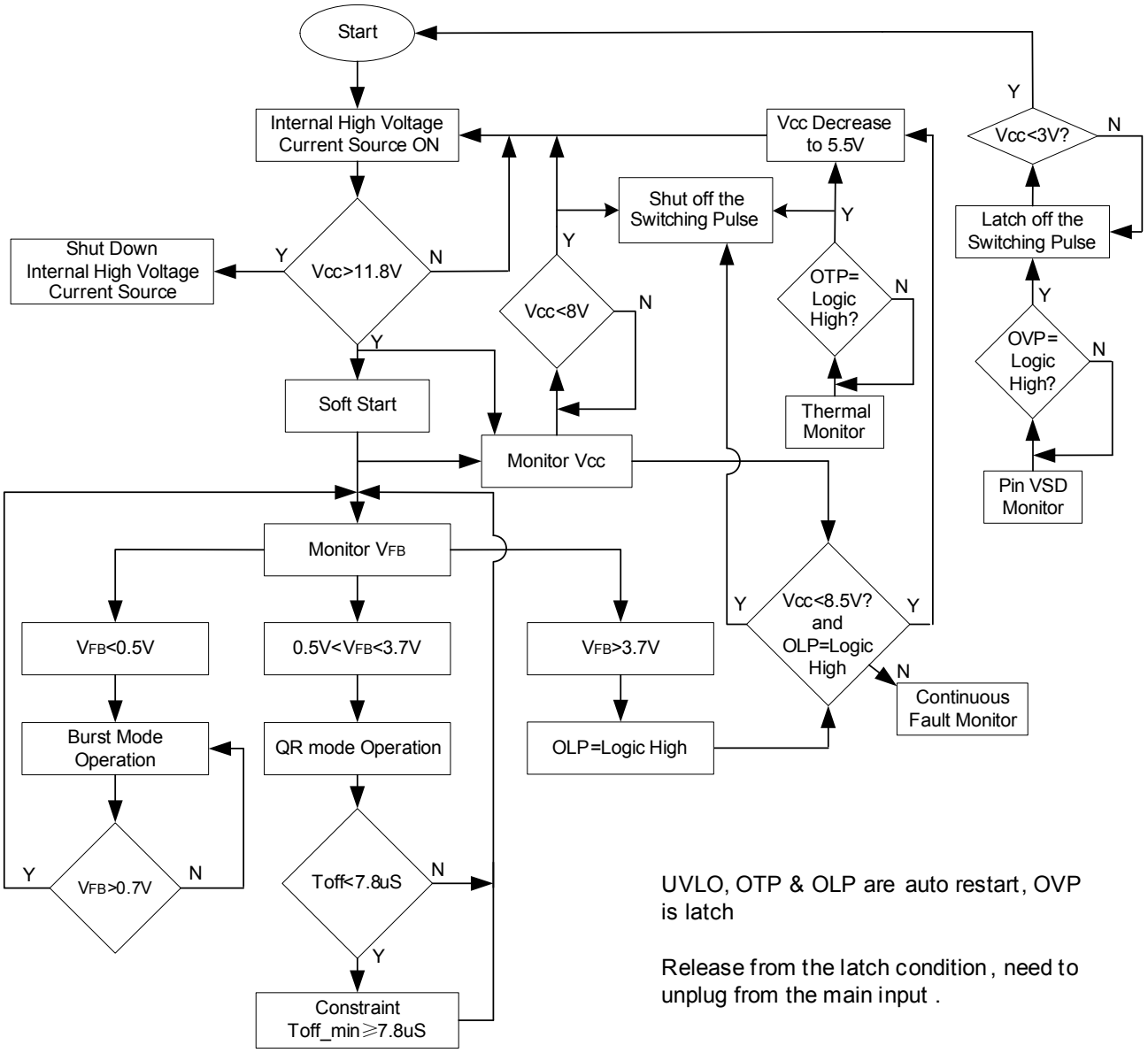


Figure 12—Control Flow Chart

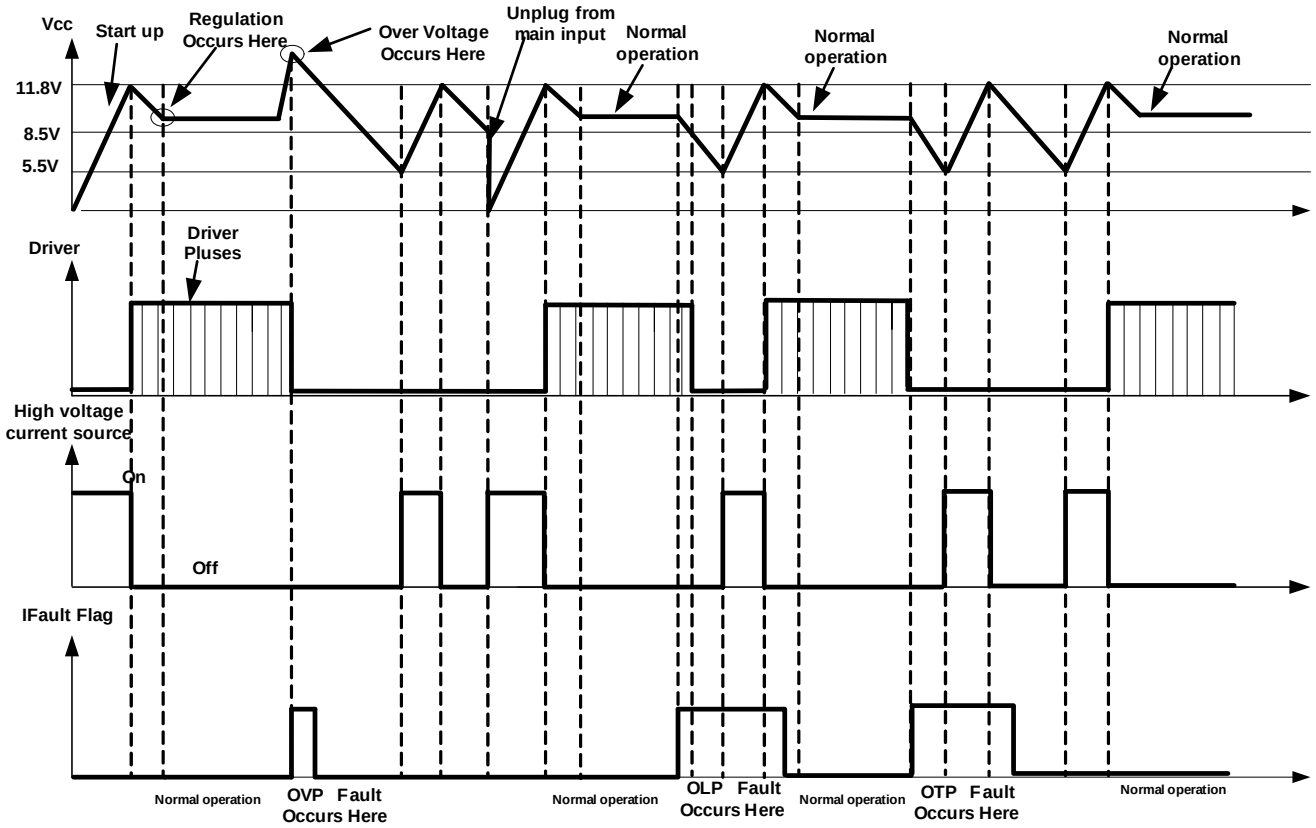
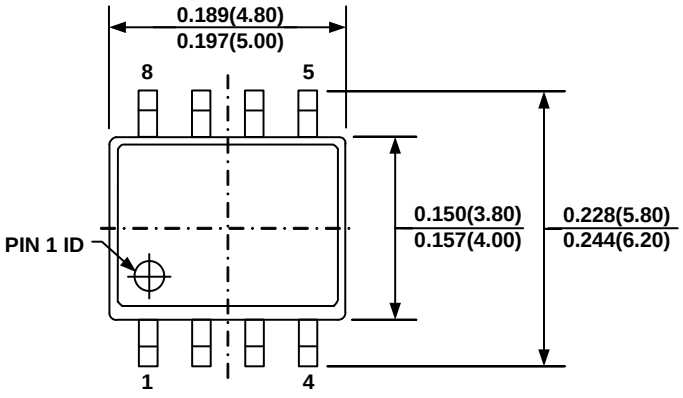


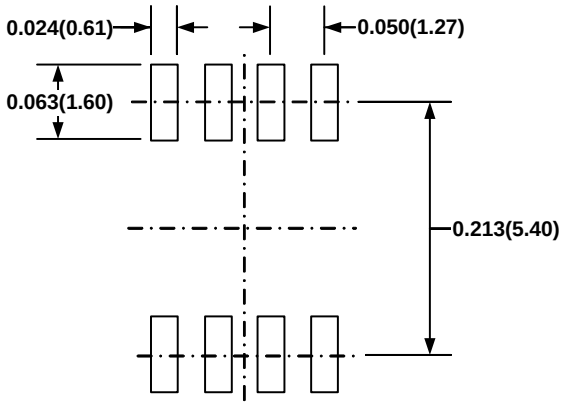
Figure 13—Evolution of the Signals in Presence of Faults

PACKAGE INFORMATION

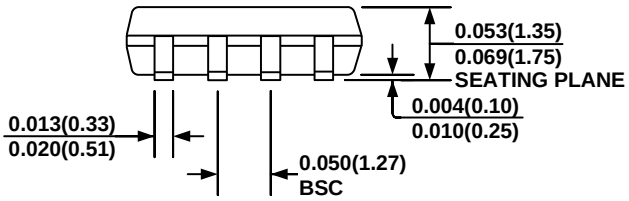
SOIC8



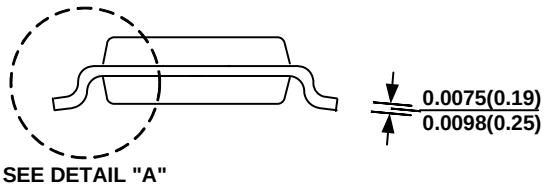
TOP VIEW



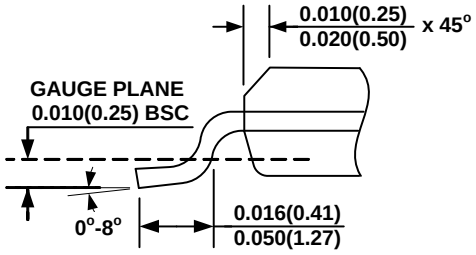
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.