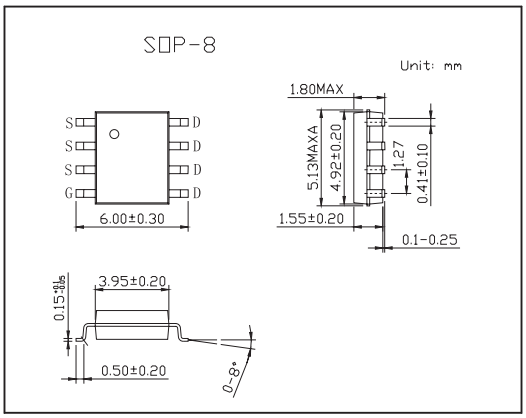
TY Semicondutor®

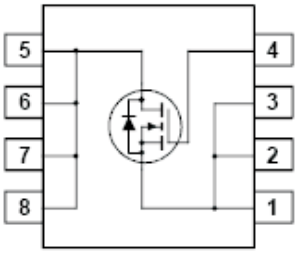
Product specification

KDS4470



■ Features

- 12.5 A, 40 V. $R_{DS(ON)}$ = 9mΩ @ V_{GS} = 10 V
- Low gate charge (45 nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	40	V
Gate to Source Voltage	V_{GS}	+30/-20	V
Drain Current Continuous (Note 1a)	I_D	12.5	A
Drain Current Pulsed		50	A
Power dissipation (Note 1a)	P_D	2.5	W
Power dissipation (Note 1b)		1.4	
Power dissipation (Note 1c)		1.2	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction to Ambient (Note 1c)	$R_{\theta JA}$	125	℃/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	25	℃/W

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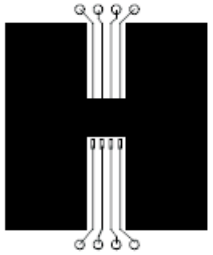
■ Electrical Characteristics Ta = 25℃

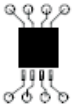
Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Avalanche Energy	E_{AS}	Single Pulse,V_{DD}=40V,I_D=12.5A(Not 2)			370	mJ
Drain-Source Avalanche Current	I_{AS}	(Not 2)			12.5	A
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 250 μA	40			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		42		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2	3.9	5	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		-8		mV/℃
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 12.5 A		6	9	mΩ
		V_{GS} = 10 V, I_D =12.5 A,T_J = 125℃		9	14	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 5 V	25			A
Forward Transconductance	g_{FS}	V_{DS} = 10V, I_D = 12.5 A		45		S
Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V,f = 1.0 MHz		2659		pF
Output Capacitance	C_{oss}			605		pF
Reverse Transfer Capacitance	C_{rss}			298		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, I_D = 1 A,V_{GS} = 10 V, R_{GEN} = 6 Ω (Note 2)		14	25	ns
Turn-On Rise Time	tr			12	22	ns
Turn-Off Delay Time	$t_{d(off)}$			37	59	ns
Turn-Off Fall Time	tf			29	46	ns
Total Gate Charge	Q_g	V_{DS} = 20 V, I_D = 12.5 A,V_{GS} = 10 V (Note 2)		45	63	nC
Gate-Source Charge	Q_{gs}			27		nC
Gate-Drain Charge	Q_{gd}			5		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				2.1	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.1 A (Not 2)		0.7	1.2	V
Diode Reverse Recovery Time	trr	I_F = 12.5 A, di_F/dt = 100 A/μs		33		nS
Diode Reverse Recovery Charge	Qrr			39		nC

Notes:

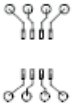
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%