1. INTRODUCTION

1.1. SUMMARY

The Rockwell C40 and L39 Microcontrollers (MCUs) are complete 8-bit microcontrollers fabricated on a single chip using CMOS silicon gate process. This MCU complements an industry standard line of R6500 and R65C00 microprocessors, as well as R6500*/, R65CXX, C19, C29, and C39 microcomputers, and their compatible peripheral devices. This MCU family has a wide range of controller applications where high 8-bit performance, minimal chip count and low power consumption are required.

The basic C40 MCU features include an enhanced 6502 Central Processing Unit (CPU), 8k bytes of internal mask programmable read only memory (ROM), 1024 bytes of internal random access memory (RAM), two 16-bit counter/timers, two 17-bit precision timing generators, an asynchronous/synchronous USART port, a 16550A interface with FIFO and DMA handshake support, a 16-bit cyclic redundancy check (CRC), a 16-bit address/8-bit data expansion bus, 8 bank select registers for flexible memory banking control, and up to 40 general purpose input/output ports. Thirty two I/O lines can be assigned to special purpose functions under software control.

The C40 also provides improved 16550A interface operation and incorporates three internal resistors to eliminate three previously required external resistors.

In addition to the C40 enhancements, the L39 MCU provides lower voltage and power operation, a Stop Mode, and expanded internal RAM. Low voltage and power mask options include 5V power and I/O with 5V core (5/5), 5V power and I/O with 3.3V core (5/3), and 3.3V power and I/O with 3.3V core (3/3).

1.2. FEATURES

- Single-chip microcomputer
  - Enhanced R6502 CPU
  - 8k (8192) bytes internal read-only memory (ROM)
  - 1024 bytes (C40) or 1470 bytes (L39) internal random access memory (RAM)
  - Two 16-bit counter/timers
  - Two 17-bit precision time generators
  - Universal asynchronous/synchronous receiver transmitter (USART)
  - Host bus for 16550A interface or scratchpad RAM interface with 16-byte FIFO and DMA
  - Eight levels of prioritized, vectored interrupts
  - High speed operation

    C40: Up to 10 MHz

    L39: Up to 15 MHz (3/3), 16.5 MHz (5/3) or 20.5 MHz (5/5)
  - Low power sleep mode
  - Ultra-low power stop mode (L39 only)
- Enhanced R6502 CPU
  - 12 new bit manipulation and branching instructions to shorten code and speed up execution
  - 21 new arithmetic processing instructions to optimize arithmetic processing
  - 10 new direct threaded code instructions to support high level languages that compile linked machine instructions
  - R6502 instruction compatible except "(indirect,X)" addressing mode changed to "(Indirect)" and "(Indirect),Y" addressing mode changed to "(Indirect),X"
- General purpose input/output (GPIO), output (GPO), or input (GPI) lines
  - 28 GPIO lines with data latches and direction registers: Ports A, C, D (0-3), and E
  - 8 output only lines with data latches: Port B
  - 4 input only lines with data latches: Port D (4-7)
  - 32 I/O lines can be assigned to special purpose functions under software control
- Two identical 16-bit programmable counter/timers with latches
  - Four modes: Interval Timer, Pulse Generation, Pulse Width Measurement, Event Counter
  - Selectable divide-by-32 prescaler
  - Timer interrupt can be vectored to either ROM or page 1 RAM
  - I/O port interface
- Two 17-bit precision time generators (PTGs) with latches
  - Increment/decrement capability with counter option (clear accumulator on overflow)
  - Interrupt enables

- Selectable Host Bus for 16550A or scratchpad RAM interface
  - 16550A interface (application software dependent)
    - 6 bytes for 16550A registers
    - 7 bytes for dual port scratch pad RAM
    - 1 byte for dual port general purpose RAM
    - 1 byte for dual port handshake
    - 1 byte for receiver and transmitter FIFO interface (16 byte deep FIFO)
    - 2 bytes for FIFO status
    - 1 byte for GP FIFO status
    - DMA interface
  - General purpose dual port RAM interface
    - 13 bytes for dual port scratch pad RAM
    - 1 byte for dual port handshake
    - 1 byte for FIFO interface (16 byte deep FIFO)
    - 2 bytes for FIFO status
    - 1 byte for GP FIFO status
    - DMA interface
- USART Serial I/O
  - Common asynchronous/synchronous features
    - Full double buffering
    - Serial in and serial out individually enabled
    - Interrupt enables for receiver buffer full and transmitter buffer empty
    - Echo modes
    - Timer B or PTGA/PTGB timing
    - Speed recognition
  - Asynchronous features
    - 5-, 6-, 7-, or 8-bit characters
    - Even, odd, stuff or no parity bit generation and detection
    - 1, 1-1/2 or 2 stop bit generation with 3/4 or 7/8 stop bit control
    - False start bit detection
    - Interrupt enables
    - Line break generation and detection
  - Synchronous features
    - Transmit data (TXD) serial input timing – internal, external TXCLK, or external TXREF
    - Received data (RXD) serial output timing – internal or external RXCLK
    - 5-, 6-, 7-, or 8-bit characters
    - Automatic word sync on first 1 to 0 transition
    - Interrupt enables for serial input clock (TXCLK) and serial output clock (RXCLK)

- Expansion Bus
  - Built-in memory banking allows up to 512k bytes of external memory to be addressed
  - Eight Bank Select Registers independently control 8k-byte memory banks
  - Each BSR defines address translation (A13-A15), A16 control, and chip select (ES0-ES3)
- Eight levels of prioritized, vectored interrupts
  - RESP (highest priority)
  - Non-mask interrupt (NMI)
  - Six prioritized interrupt requests (IRQ1-IRQ6)

    Six IRQ ROM vectors

    Two software selectable Timer IRQ page 1 RAM vectors

  Internal clock with crystal or clock input
  - Internal divide-by-1 input frequency divider
  - Input Frequency

    C40:1 MHz to 10 MHz

    L39: 1 MHz to 15 MHz (3/3), 16.5 MHz (5/3), or 20.5 MHz (5/5) MHz
  - Sleep mode, software enabled,

    Low power dissipation

    Normal operation resumption within 2 clock cycles upon wake up condition
  - Stop mode, software enabled (L39 only))

    Ultra-low power dissipation

    Normal operation resumption within 12 clock cycles after power on stabilization upon wake up condition
  - Flexible wake up conditions from Sleep or Stop mode

    Awakened by a low on NMIP

    Awakened by a high detected on PA0, software enabled

    Awakened by a low detected on PA2, software enabled

    Awakened by a low detected PD4, software enabled

    Awakened by a low detected PD5 software enabled

    Awakened by a low detected on PD4 or on PD5, software enabled
- Available in plastic leaded chip carrier (PLCC) or low profile plastic quad flat pack (PQFP) packages
  - 84-pin PLCC
  - 80-pin PQFP
- Flexible power supply

  +5 V ±5%

  +3.3 V ±0.3V (L39 only)

1.3. MCU FEATURE COMPARISON

The feature differences between the MCUs are summarized in Table 1-1.

Table 1-1. MCU Feature Comparison

Feature	C2900	C3900	C4000	L3900	L3902	Units	Ref.
Power Supply	+5	+5	+5	+5/+3.3	+5/+3.3	VDC	4.2
Crystal speed divisor	2	1	1	1	1		3.3
Maxiimum clock frequency	10	10	10	15, 16.5, or 20.5	15, 16.5, or 20.5	MHz	3.3
ROM	8k	8k	8k	8k	8k	Bytes	3.6
Slow external clock firmware in internal ROM	No	No	Yes	Yes	Yes		3.6.2
RAM	1024	1024	1024	1470	1470	Bytes	3.7
Page 0 RAM	128	128	192	192	192	Bytes	3.7
Page 1-3 RAM	768	768	768	768	768	Bytes	3.7
Page 4 RAM	128	128	64	256	256	Bytes	3.7
Page 5 RAM	0	0	0	254	254	Bytes	3.7
64-byte RAM on page 1 addressable on page 0	Yes	Yes	No	No	No		3.9.6
CRC Locations	0480-0481	0480-0481	05FE-05FF	05FE-05FF	05FE-05FF		Fig. 3-2b
Bytes GP Scratchpad RAM	15	13	13	13	13	Bytes	3.14.2
16-byte FIFO	No	Yes	Yes	Yes	Yes		3.14.2, 3.14.3
Host interface	16450	16550A	16550A	16550A	16550A		3.14.3
16550 interface Timer B & PTGB Override	No	No	Yes	Yes	Yes		3.14.3
Six FIFO IRQ3 interrupts added to 16550 interface	No	Yes	Yes	Yes	Yes		Table 3-5
DMA handshake with RDYand ACK lines	No	Yes	Yes	Yes	Yes		3.14.3, 3.14.14
Internal pull-up resistors provided on PA3 and PA4	NA	No	Yes	No	Yes		Table 2-1
Enable RXD on PA6 when RXD is selected (SM7 = 1); overrides RXRDY on PA6 in 16550 mode (FCR0 = 1)	No	No	Yes	Yes	Yes		3.12
In 16550 mode (FCR0 = 1), disable HTACKP on PA3 and HRACKP on PA4 when RXD mode is selected (SM7 = 1) or SYNC mode is selected (SM4 = 1)	No	No	Yes	No	Yes		3.12
USART PTG divide by 3 option	No	No	Yes	Yes	Yes		3.12.8
USART PTGA source option for SINC	No	No	Yes	Yes	Yes		3.12.4
Low power mode	Sleep	Sleep	Sleep	Sleep/Stop	Sleep/Stop		3.4
Data bus (D0-D7) receivers off during Sleep/Stop	No	No	Yes	Yes	Yes		Table 2-1
Wake-up interrupts in low power mode	3	5	5	5	5		3.16.1
BRK vector	IRQ6	NMI	NMI	NMI	NMI		3.5.2

1.4. MCU DESIGN CHANGES FROM THE C39 MCU

MCU changes effecting input/output operation are summarized below.

1.4.1. Design Changes Incorporated in the C40 MCU

A. Common to the C40, L3900, and L3902

1. **Slow External Clock Internal Firmware Added.** Firmware was added to internal masked ROM to support 8 MHz applications.
2. **Software Selectable 64-byte RAM Segments Deleted.** The ability to select 64-byte segments of page 1 addressable on page 0 was deleted. 64 bytes are permanently reassigned to page 0 (now 192 bytes).
3. **LSR Flag Setting Synchronized.** The 16550 Line Status Register (LSR) error flag setting was synchronized with the data in RX FIFO to prevent erroneous operation (loss of valid data and acceptance of erroneous data) by communications software that interprets the error status flags.
4. **USART Timer Improved.** An option to select the divide by 3 function on the USART timing source was added and an option to select the PTGA as the USART timing source for SINC was added.
5. **Enable RXD on PA6 in 16550 Mode Added** The ability to enable RXD on PA6 when RXD is selected (SMR7 = 1) regardless of other modes, was added.

B. Common to the C40 and L3902

1. **Internal PA3 and PA4 Pull-up Resistors Added.** Internal Pull-up resistors were added to the PA3 and PA4 ports to eliminate the need for external pull-up resistors.
2. **Disable HTACKP and HRACKP in 16550 Mode Added.** When 16550 mode is selected (FCR0 = 1), the ability to disable HTACKP on PA3 and HRACKP on PA4 when RXD mode is selected (SMR7 = 1) or SYNC mode is selected (SMR4 = 1) was added.
3. **Internal XTLO 100 Ohm Series Resistor Added.** An internal 100 ohm series resistor was added to the XTLO signal to eliminate the need for an external 100 ohm series resistor to improve oscillator start up with fast rise time power supplies. In application designs already providing an external 100 ohm resistor, the external resistor may be left in the circuit (providing 200 ohms total) with no adverse effect.
4. **FIFO Operation Improved.**
   a. The ability of the host to read the receive buffer during the first interval after the MCU writes to an empty RX FIFO was added.
   b. A problem that can occur when the host does not read the 16450 buffer between the first and second baud interval after the MCU writes to an empty receiver FIFO was corrected.
   c. Clearing of the RX FIFO and the TX FIFO whenever the host changes the state of the FIFO Enable bit in the FIFO Control Register (FCR0) was added.

1.4.2. Design Changes Incorporated in the L3900 MCU

A. Common to the C40, L3900, and L3902

Same As 1.4.1 Item A.

B. Common to the L3900 and L3902

1. **3.3 V Operation Option Added.** The ability to operate the MCU on 3.3 V I/O and 3.3 V core (3/3) was added (mask option).
2. **5 V Low Power Operation Option Added.** The ability to operate the MCU with a 5 V I/O and a 3.3 V core (5/3) was added for lower power operation in addition to the 5 V I/O and 5 V core (5/5) (mask option).
3. **Maximum Clock Rate Raised.** The maximum clock frequency was raised to 20.5 MHz (5/5), 16.5 MHz (5/3), or 15 MHz (3/3).
4. **Power Consumption Reduced.** Circuits were improved to reduce power consumption.
5. **Stop Mode Added.** Stop mode was added with ultra-low power consumption.
6. **Internal RAM Enlarged.** The internal RAM was enlarged from 1024 bytes to 1470 bytes.
7. **Data Bus Receivers Disabled in Low Power Modes.** Circuitry was added to disable external memory bus data receivers in low power mode (Sleep and Stop).

1.4.3. Design Changes Incorporated in the L3902 MCU

A. Common to the C40, L3900, and L3902

Same as 1.4.1 Item A.

B. Common to the C40 and L3902

Same as 1.4.1 Item B.

C. Common to the L3900 and L3902

Same as 1.4.2 Item B.

D. Unique to the L3902

1. **16550 Interface Operation Improved.**
   a. The Interrupt Identifier Register (IIR) operation was changed to automatically clear the Receiver Buffer Full (Data Available) interrupt when the RX FIFO trigger level control is changed from a value lower than the RX FIFO contents to a value greater than the RX FIFO contents.
   b. The IIR operation was changed to cause the Receiver Buffer Full and Character Timeout interrupts to respond to changes to the receiver timeout event without first reading the RX FIFO.
2. **Internal ROM Read Added.** The ability to read internal ROM from address $FE00-$FFFF when TSTP pin is low was added.

1.5. REFERENCES

1. C39R (C40) Microcontroller PO1 Specification, Rev. NC, January 19, 1994.
2. L39 Microcontroller PO1 Specification, Rev. NC, February 21, 1994.