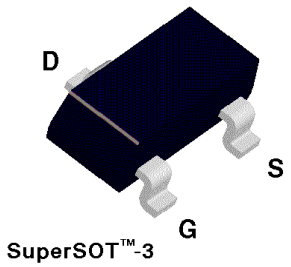
NDS352P

General Description

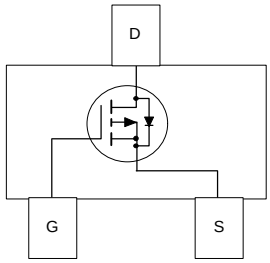
These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -0.85A, -20V. $R_{DS(ON)}$ = 0.5Ω @ V_{GS} = -4.5V.
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface mount package.



SuperSOT™-3



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS352P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		±12	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	±0.85	A
	- Pulsed		±10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-5	µA
		T_J =125°C			-20	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.8	-1.6	-2.5	V
		T_J =125°C	-0.5	-1.3	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -0.85 A		0.46	0.5	Ω
		T_J =125°C		0.59	0.7	
		V_{GS} = -10 V, I_D = -1 A			0.35	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-2			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -0.85 A		1.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		125		pF
C_{oss}	Output Capacitance			140		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GS} = -10 V, R_{GEN} = 50 Ω		8	15	ns
t_r	Turn - On Rise Time			19	30	ns
$t_{d(off)}$	Turn - Off Delay Time			64	90	ns
t_f	Turn - Off Fall Time			61	90	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -0.85 A, V_{GS} = -5 V		2.2	4	nC
Q_{gs}	Gate-Source Charge				1	nC
Q_{gd}	Gate-Drain Charge				2	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.85 A (Note 2)		-0.92	-1.2	V

Notes:

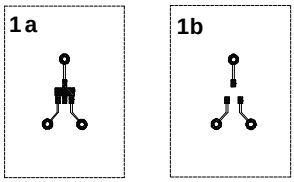
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz cpper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz cpper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.