Dual N-Channel 20 V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY				
	V_{DS}	$R_{DS(on)}$ (Ω)	I_D (A)[a, f]	Q_g (Typ.)
Channel-1	20	0.022 at V_{GS} = 10 V	8	8
		0.025 at V_{GS} = 4.5 V	8	
Channel-2	20	0.015 at V_{GS} = 10 V	8	17
		0.019 at V_{GS} = 4.5 V	8	

SCHOTTKY PRODUCT SUMMARY		
V_{DS} (V)	V_{SD} (V) Diode Forward Voltage	I_F (A)[a]
20	0.43 V at 1 A	4

FEATURES

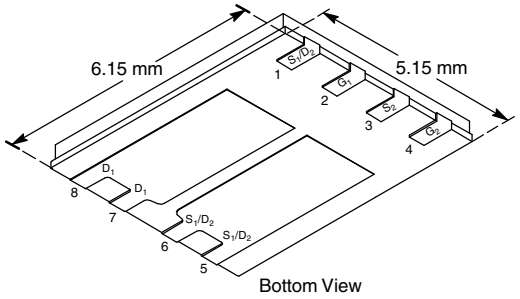
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

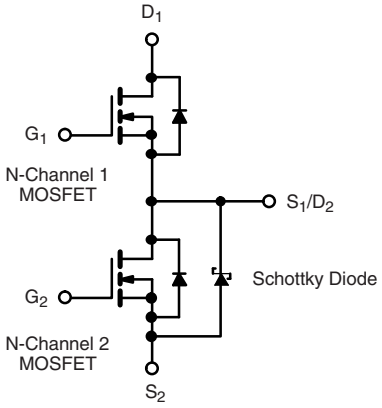
- Synchronous Buck Converter
  - Game Machines
  - Notebook Computers

PowerPAK SO-8



Bottom View

Ordering Information:
Si7980DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage		V_{DS}	20	20	V
Gate-Source Voltage		V_{GS}	± 16	± 16	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	8[f]	8[f]	A
	T_C = 70 °C		8[f]	8[f]	
	T_A = 25 °C		8.8[b, c]	11[b, c]	
	T_A = 70 °C		7.1[b, c]	9[b, c]	
Pulsed Drain Current		I_{DM}	30	30	
Source-Drain Current Diode Current	T_C = 25 °C	I_S	8[f]	8[f]	
	T_A = 25 °C		2.8[b, c]	2.8[b, c]	
Pulsed Source-Drain Current		I_{SM}	30	30	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	15	15	
Single Pulse Avalanche Energy		E_{AS}	11.2	11.2	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	19.8	21.9	W
	T_C = 70 °C		12.6	14	
	T_A = 25 °C		3.1[b, c]	3.4[b, c]	
	T_A = 70 °C		2[b, c]	2.2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[d, e]			260		

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Package limited.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Channel-1 Typ.	Channel-1 Max.	Channel-2 Typ.	Channel-2 Max.	Unit
Maximum Junction-to-Ambient[a, b]	t ≤ 10 s	R_{thJA}	32	40	30	36	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	5	6.3	4.5	5.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions		Min.	Typ.[c]	Max.	Unit
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	Ch-1	20			V
		V_{GS} = 0 V, I_D = 1 mA	Ch-2	20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	Ch-1		22		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	Ch-1		- 5		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	1		2.5	V
		V_{DS} = V_{GS}, I_D = 1 mA	Ch-2	1.4		2.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 16 V	Ch-1			100	nA
		V_{DS} = 0 V, V_{GS} = ± 16 V	Ch-2			100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	Ch-1			0.001	mA
		V_{DS} = 20 V, V_{GS} = 0 V	Ch-2		0.05	0.50	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 100 °C	Ch-1			0.025	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 100 °C	Ch-2		3	15	
On-State Drain Current[d]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	Ch-1	10			A
		V_{DS} = 5 V, V_{GS} = 10 V	Ch-2	10			
Drain-Source On-State Resistance[d]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	Ch-1		0.018	0.022	Ω
		V_{GS} = 10 V, I_D = 5 A	Ch-2		0.012	0.015	
		V_{GS} = 4.5 V, I_D = 4 A	Ch-1		0.020	0.025	
		V_{GS} = 4.5 V, I_D = 4 A	Ch-2		0.015	0.019	
Forward Transconductance[d]	g_{fs}	V_{DS} = 15 V, I_D = 5 A	Ch-1		40		S
		V_{DS} = 15 V, I_D = 5 A	Ch-2		47		
Dynamic[c]							
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	Ch-1		1010		pF
			Ch-2		1370		
Output Capacitance	C_{oss}		Ch-1		220		
		Channel-2 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	Ch-2		320		
Reverse Transfer Capacitance	C_{rss}		Ch-1		100		
			Ch-2		120		

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. Maximum under steady state conditions is 88 °C/W (channel-1) and 83 °C/W (channel-2).
c. Guaranteed by design, not subject to production testing.
d. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

For technical questions, contact: pmostechsupport@vishay.com
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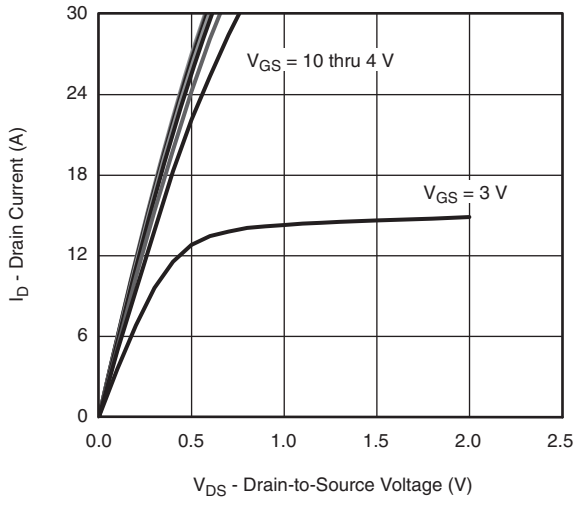
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.[a]**	**Max.**	**Unit**
Dynamic[a]							
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 5 A	Ch-1		17.5	27	nC
		V_{DS} = 10 V, V_{GS} = 10 V, I_D = 5 A	Ch-2		22.5	34	
		Channel-1 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 5 A	Ch-1		8	12	
			Ch-2		10.3	16	
Gate-Source Charge	Q_{gs}		Ch-1		2.5		
		Channel-2 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 5 A	Ch-2		3.4		
Gate-Drain Charge	Q_{gd}		Ch-1		2.1		
			Ch-2		2.6		
Gate Resistance	R_g	f = 1 MHz	Ch-1	0.2	1.1	2.2	Ω
			Ch-2	0.2	1.3	2.6	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1		9	18	ns
			Ch-2		13	25	
Rise Time	t_r		Ch-1		16	30	
			Ch-2		16	30	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1		20	35	
			Ch-2		24	45	
Fall Time	t_f		Ch-1		9	18	
			Ch-2		8	16	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1		15	30	
			Ch-2		18	35	
Rise Time	t_r		Ch-1		18	35	
			Ch-2		18	35	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1		20	40	
			Ch-2		25	45	
Fall Time	t_f		Ch-1		12	24	
			Ch-2		10	20	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	Ch-1			8	A
			Ch-2			8	
Pulse Diode Forward Current[a]	I_{SM}		Ch-1			30	
			Ch-2			30	
Body Diode Voltage	V_{SD}	I_S = 2 A	Ch-1		0.73	1.1	V
		I_S = 1 A	Ch-2		0.37	0.43	
Body Diode Reverse Recovery Time	t_{rr}	Channel-1 I_F = 5 A, dI/dt = 100 A/µs, T_J = 25 °C	Ch-1		16	32	ns
			Ch-2		20	40	
Body Diode Reverse Recovery Charge	Q_{rr}		Ch-1		8	16	nC
			Ch-2		10	20	
Reverse Recovery Fall Time	t_a	Channel-2 I_F = 5 A, dI/dt = 100 A/µs, T_J = 25 °C	Ch-1		8		ns
			Ch-2		9		
Reverse Recovery Rise Time	t_b		Ch-1		8		
			Ch-2		11		

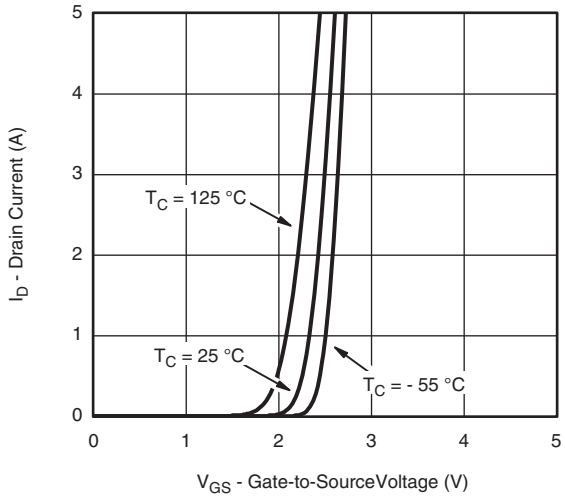
Note:
a. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

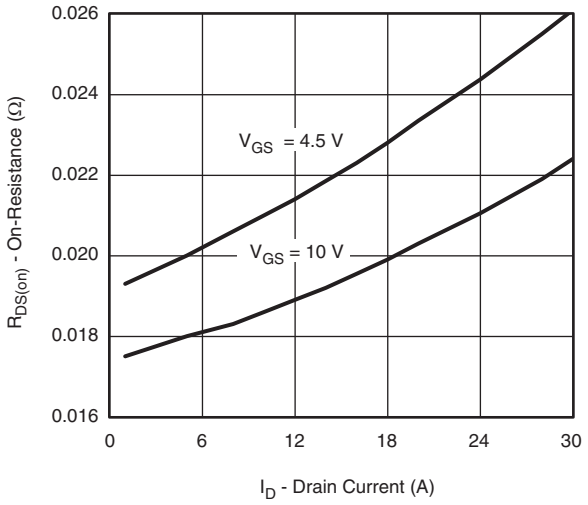
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



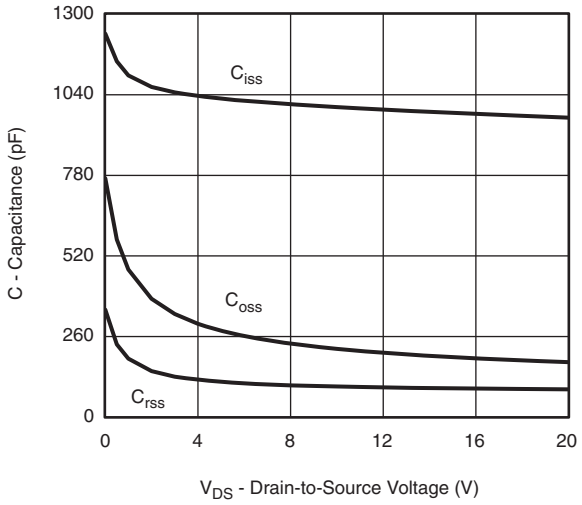
Output Characteristics



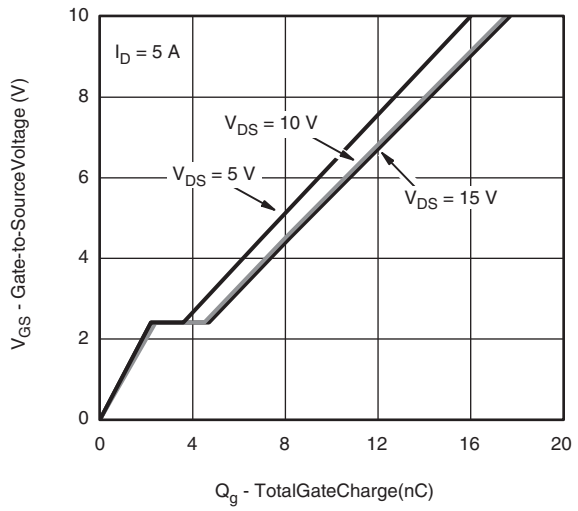
Transfer Characteristics



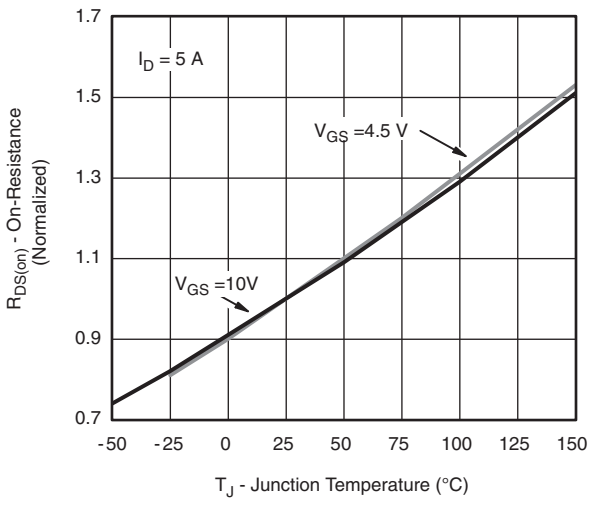
On-Resistance vs. Drain Current



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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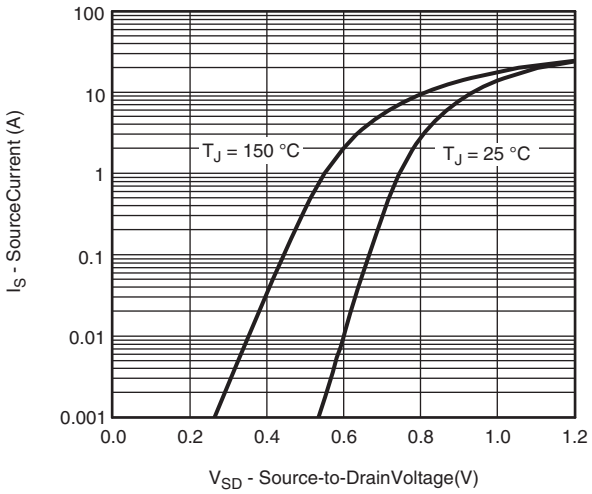
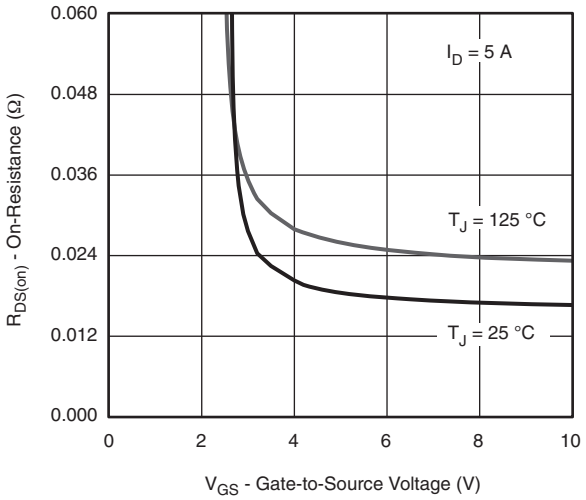
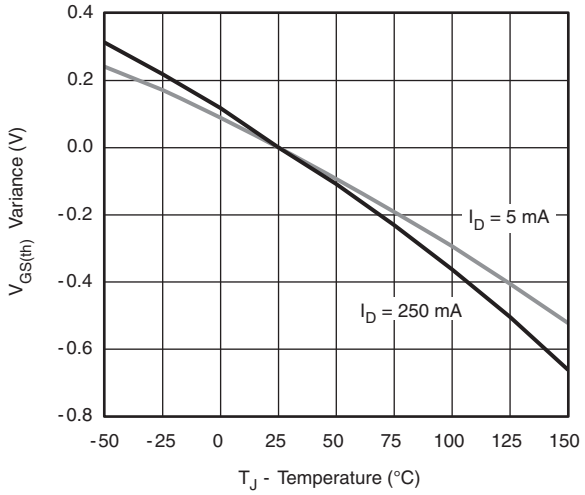


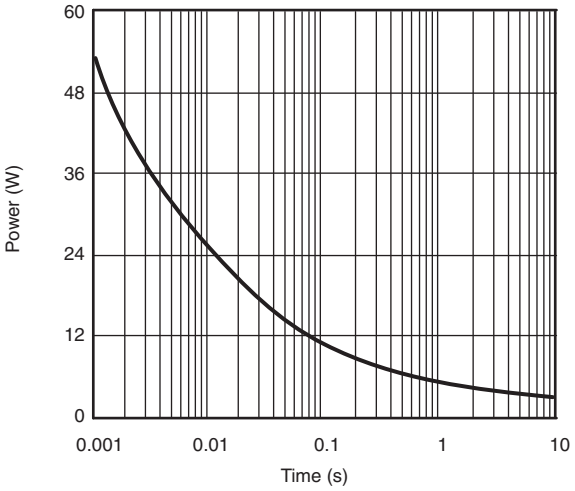
Source-Drain Diode Forward Voltage



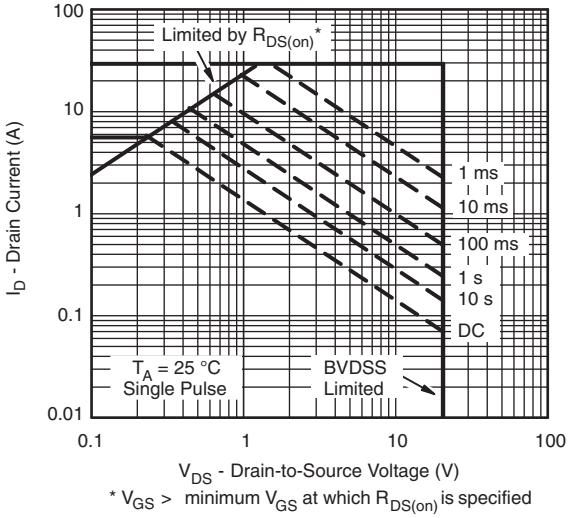
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

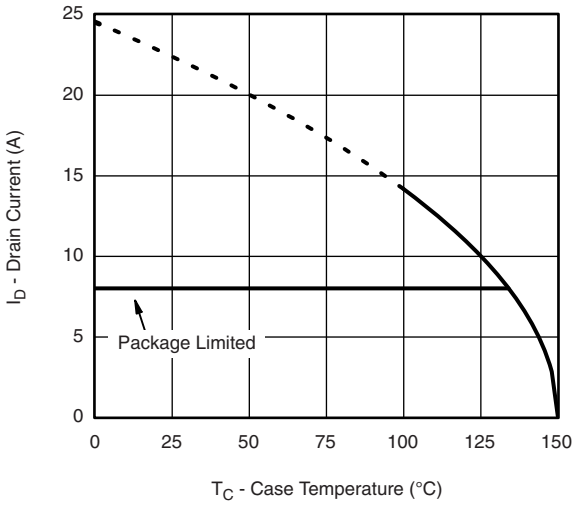


Single Pulse Power, Junction-to-Ambient

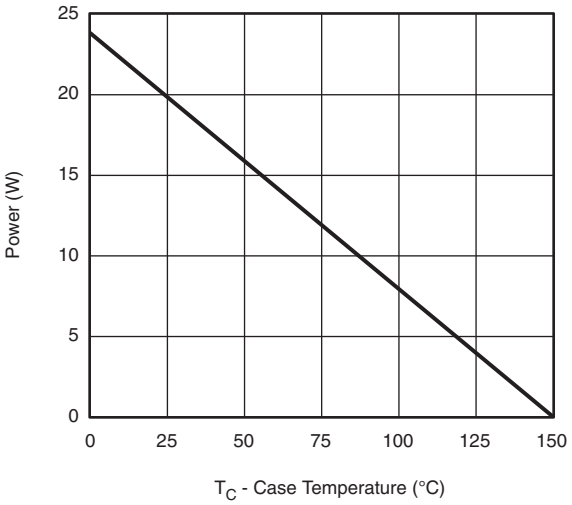


Safe Operating Area, Junction-to-Ambient

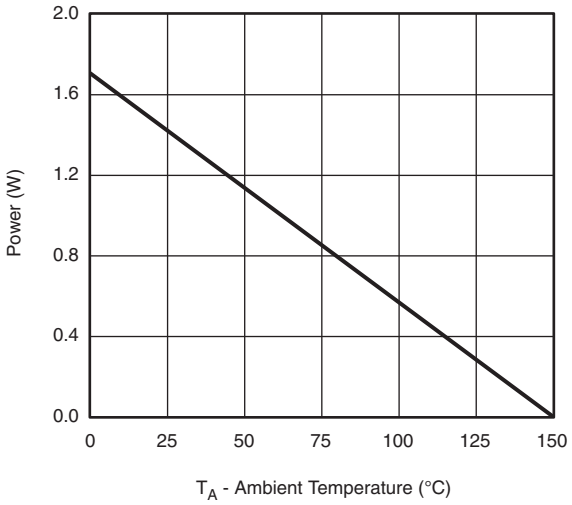
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power Derating, Junction-to-Case



Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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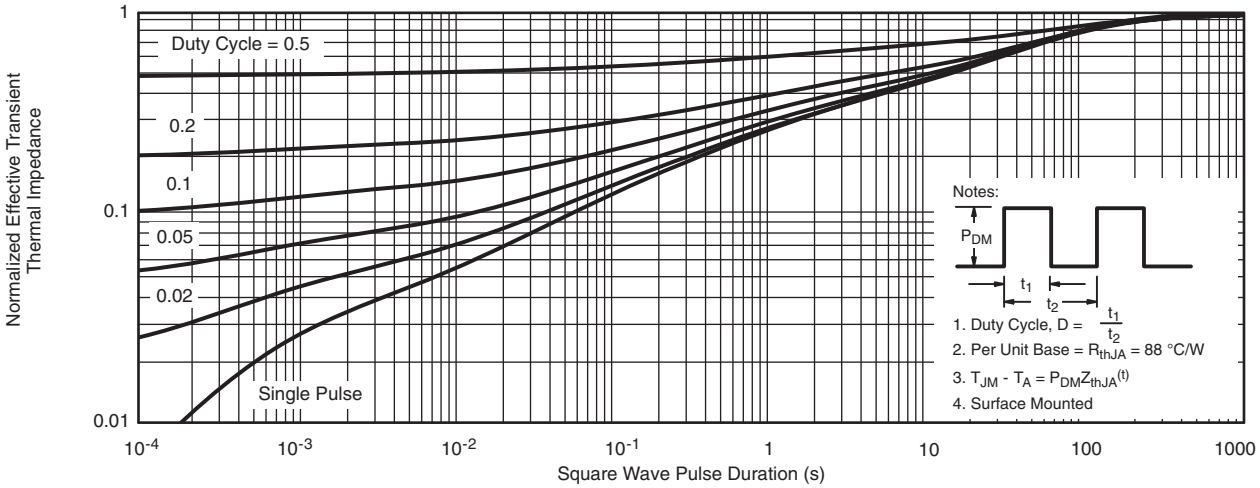
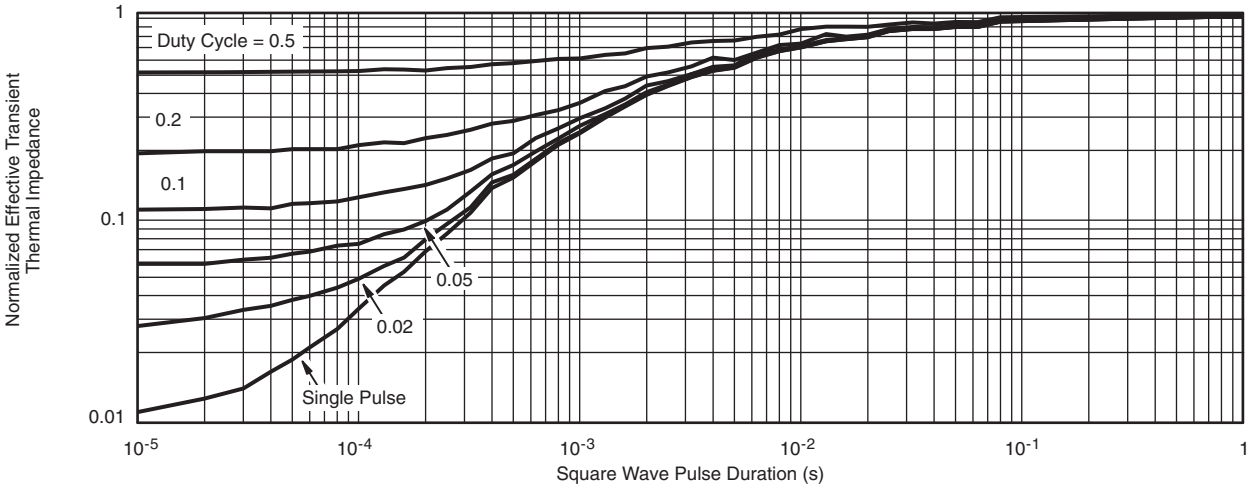
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

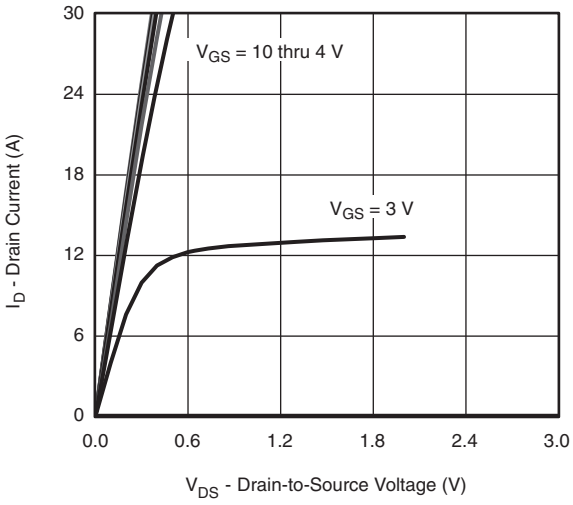


Normalized Thermal Transient Impedance, Junction-to-Ambient

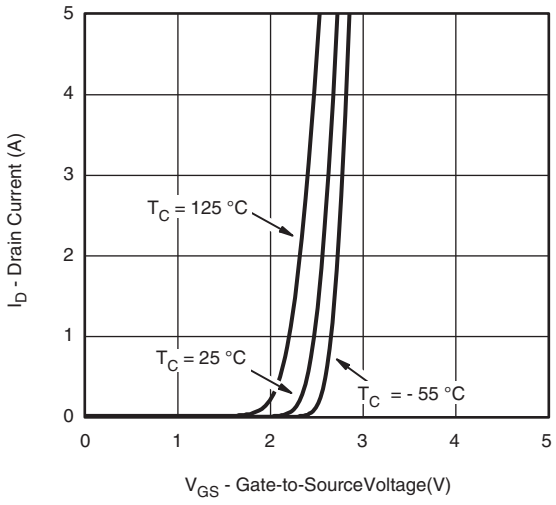


Normalized Thermal Transient Impedance, Junction-to-Case

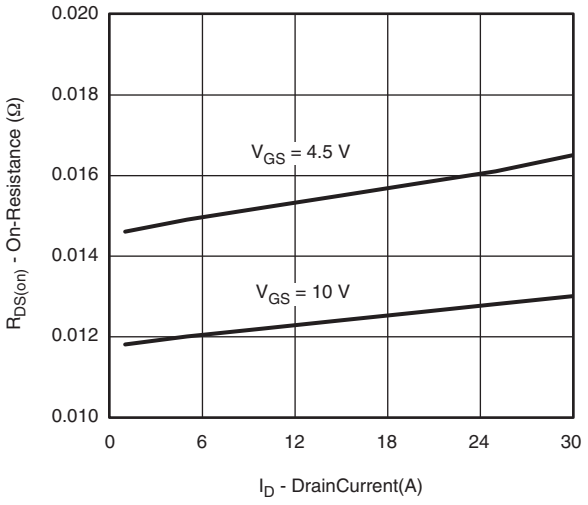
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



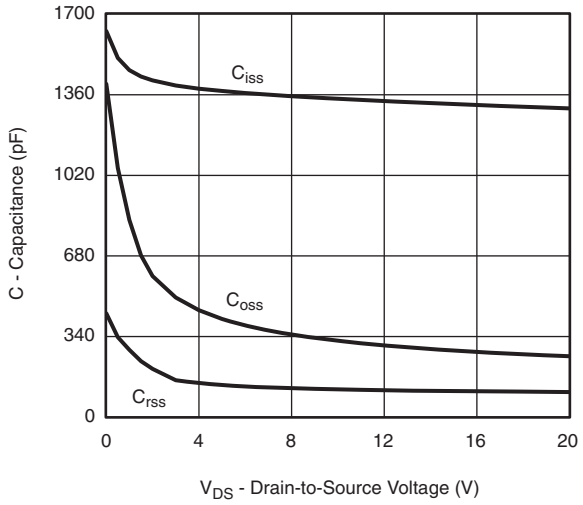
Output Characteristics



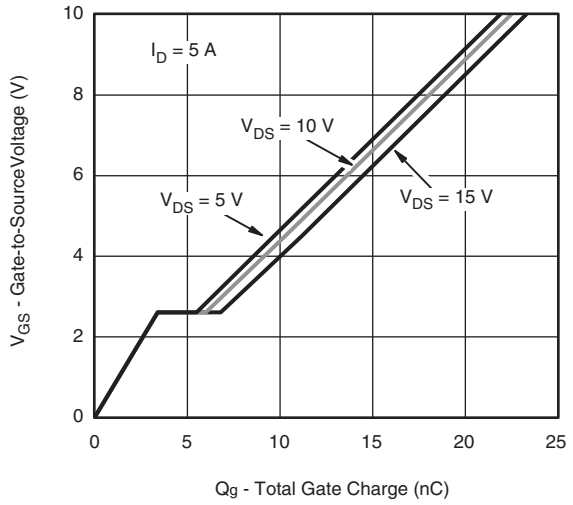
Transfer Characteristics



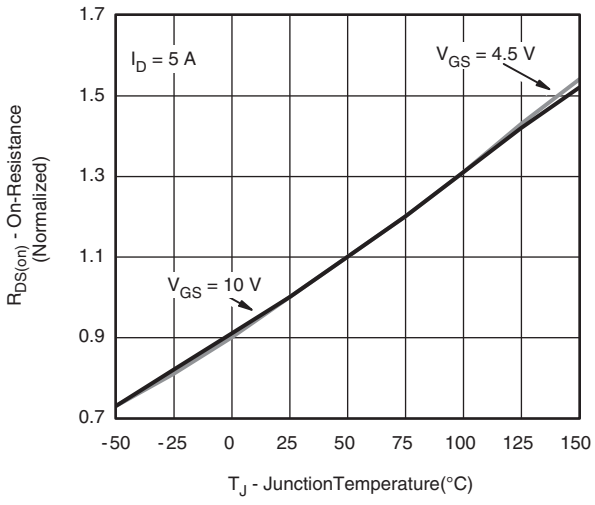
On-Resistance vs. Drain Current



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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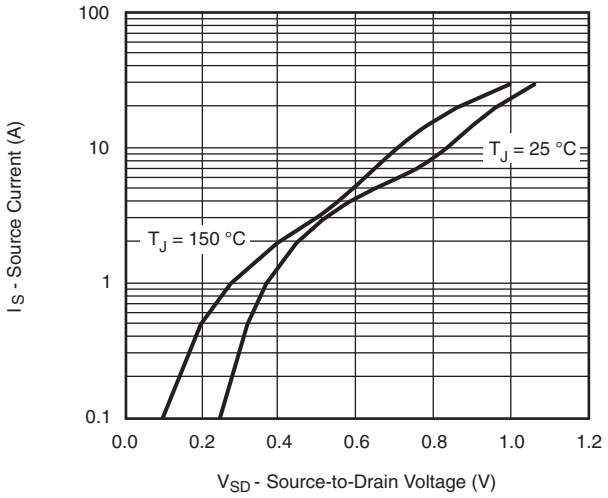
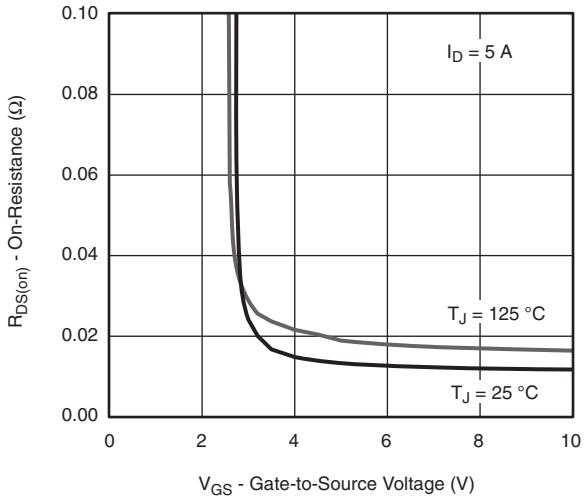
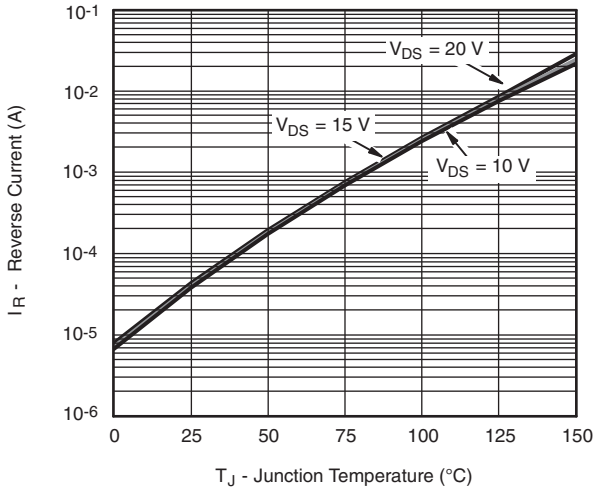
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



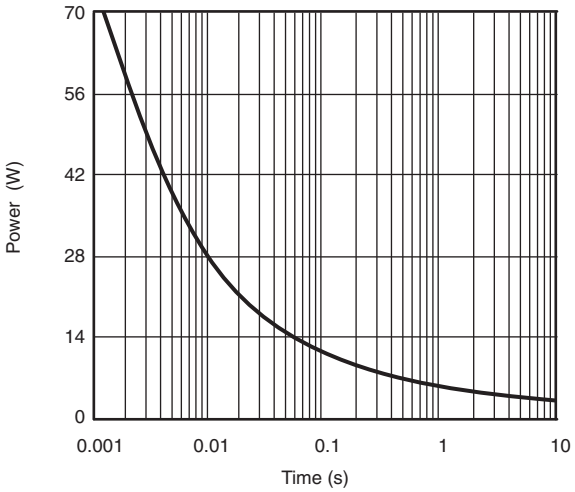
Source-Drain Diode Forward Voltage



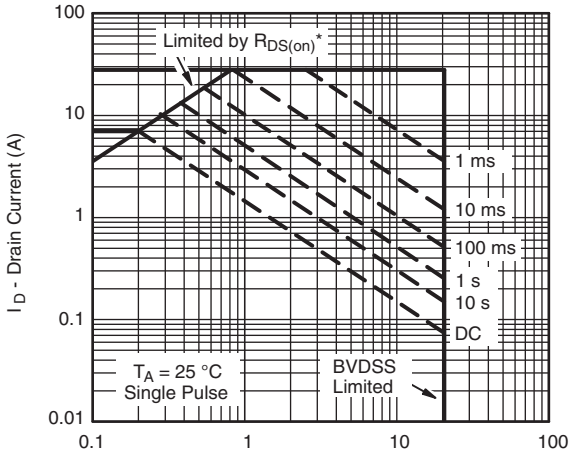
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)



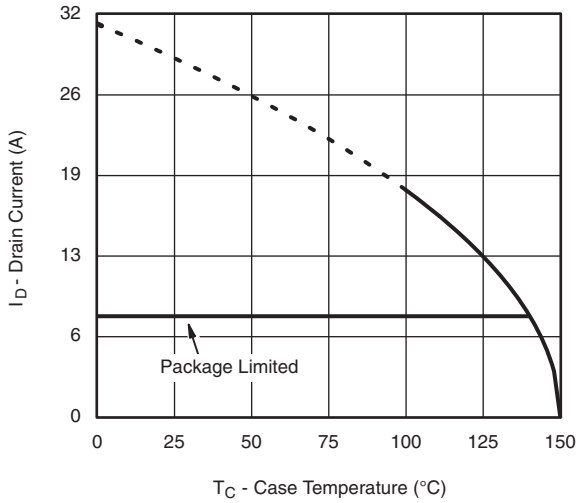
Single Pulse Power, Junction-to-Ambient



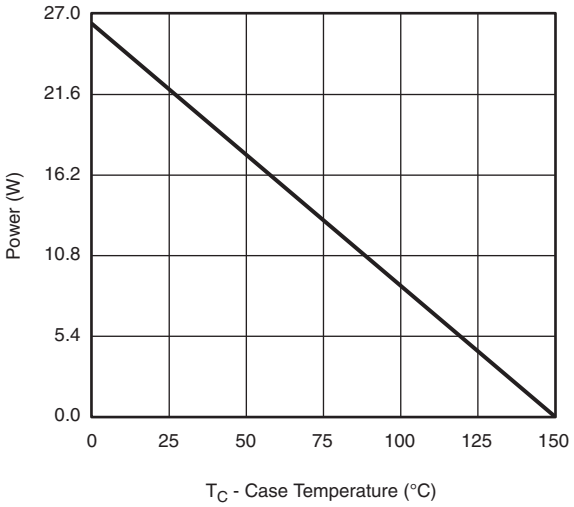
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

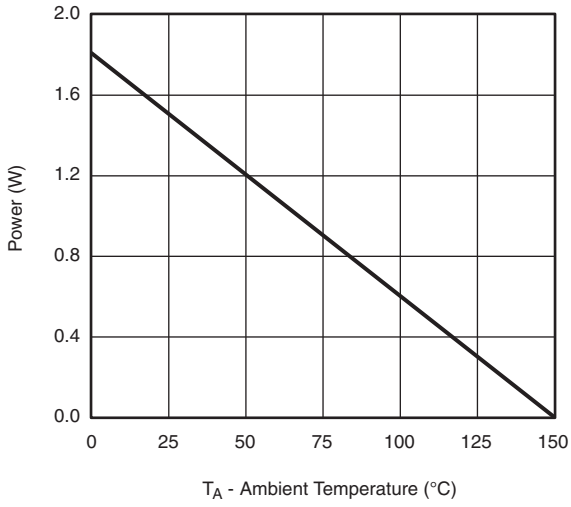
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power Derating, Junction-to-Case

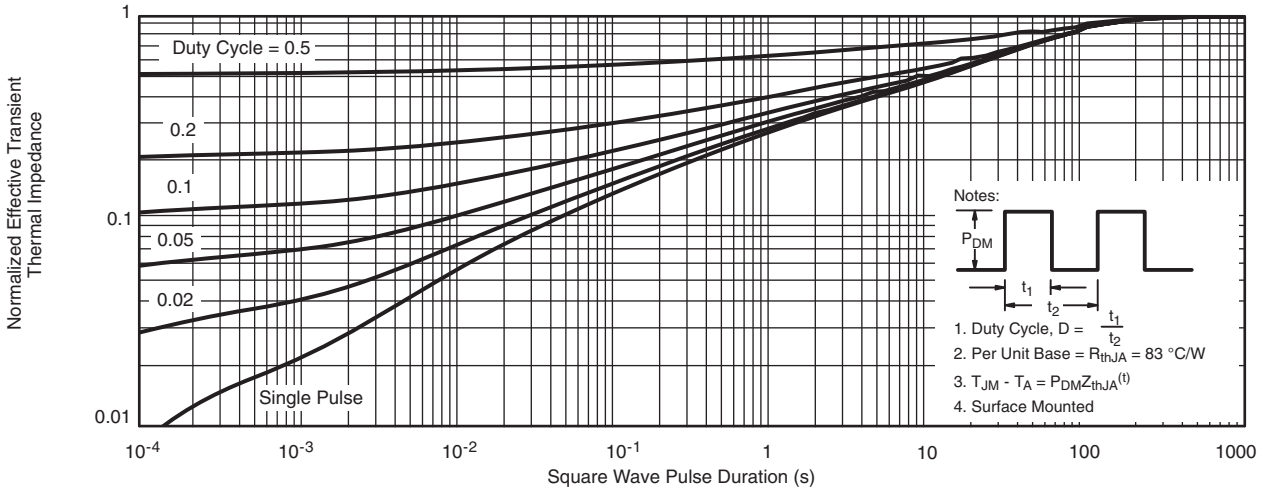


Power Derating, Junction-to-Ambient

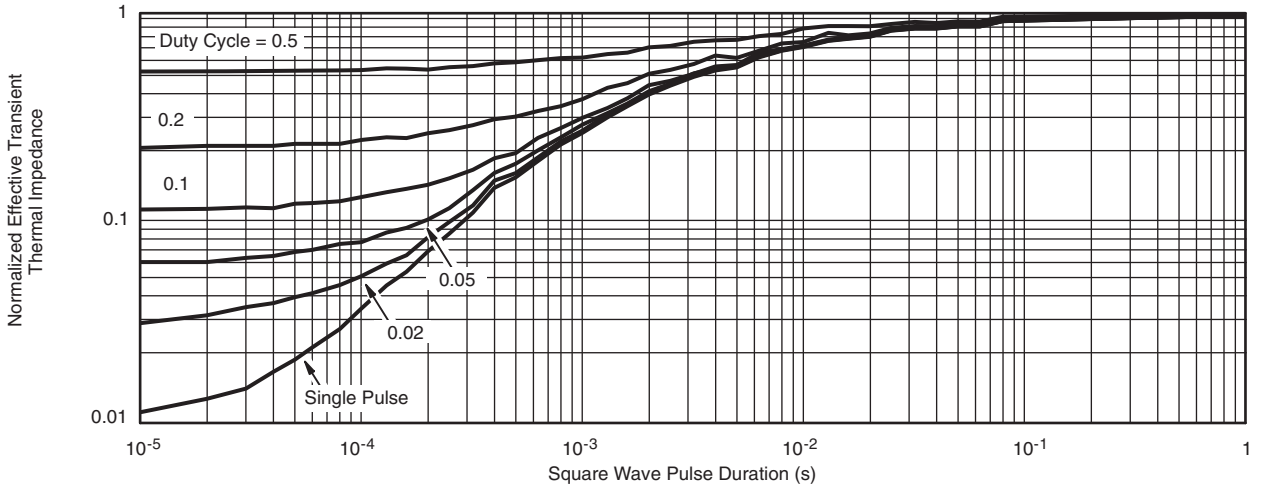
* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

For technical questions, contact: pmostechsupport@vishay.com
Document Number: 68391
S13-0631-Rev. D, 25-Mar-13

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



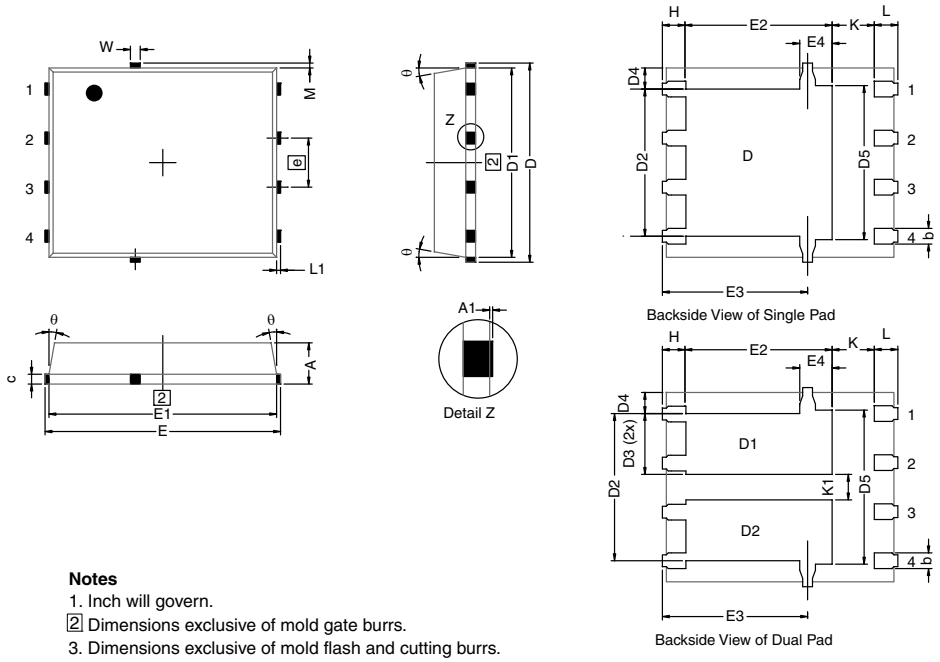
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68391.

PowerPAK® SO-8, (Single/Dual)

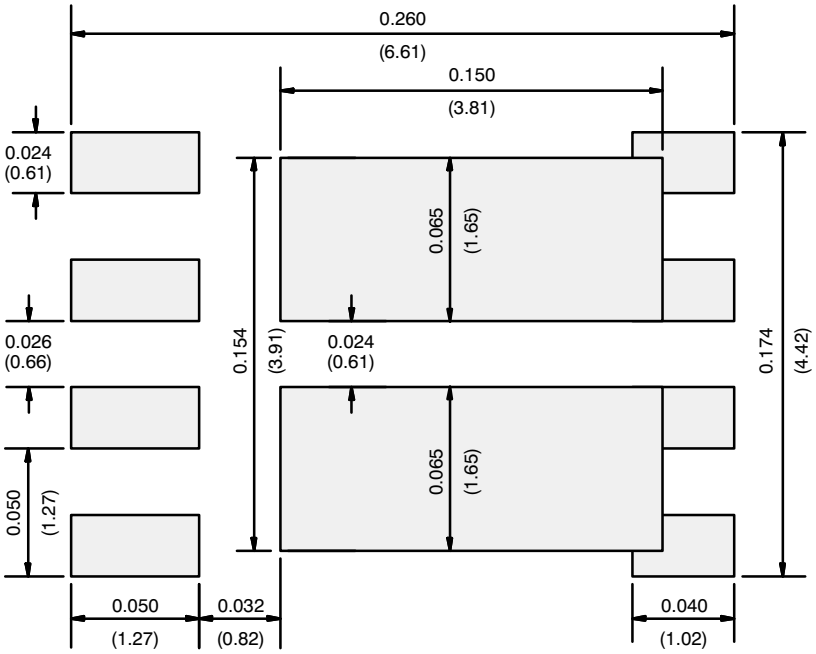


Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4		0.57 typ.			0.0225 typ.	
D5		3.98 typ.			0.157 typ.	
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)		0.58 typ.			0.023 typ.	
E4 (for other product)		0.75 typ.			0.030 typ.	
e		1.27 BSC			0.050 BSC	
K (for AL product)		1.45 typ.			0.057 typ.	
K (for other product)		1.27 typ.			0.050 typ.	
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M		0.125 typ.			0.005 typ.	
ECN: C13-0702-Rev. K, 20-May-13 DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Dual



Recommended Minimum Pads
Dimensions in Inches/(mm)

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