

# 3/6-Port DS3/E3/STS-1 Integrated Line Termination Device for Transport

# M29323/6-"Line-Card-on-a-Chip"

The M29323/6 provides a complete physical-layer solution for flexible DS3/E3/STS-1 clear channel services. The M29323/6 aggressively drives down cost for existing solutions and as well as reduces PCB real-estate and power.

Each port of the M29323/6 operates independently allowing for a mix of DS3, E3 or STS-1 on the same device. This enables ADMs/OEDs and MSPPs to deploy a single line card that supports the simultaneous mapping for SDH or SONET transport of both DS3 and E3.

The M29323/6 includes 3/6 independent DS3/E3/STS-1 line interface units (LIUs) with built-in digital jitter attenuators (DJAT), 6/12 DS3/E3 framers and 3/6 STS-1 framers. Each port is capable of supporting DS3/E3/STS-1 mapped/demapped signals to/from SONET/SDH.

The M29323/6 line side interfaces support electrical DS3/E3/STS-1, requiring only the addition of transformers and passive termination. The M29323/6 system interface supports STS-12/STM-4 for the SONET/SDH traffic via a standard 8-bit, 77 MHz TDM telecom bus. Thus, a channelized OC-12/STM-4 or OC-3/STM-1 can be broken down to DS3/E3/STS-1 streams by the M29323/6 on a channel-bychannel basis.

The M29323/6 requires only one 19.44 MHz reference clock (passive crystal) or 77.76/155.52 MHz SONET reference clock for generating all the necessary internal line rate clocks. The generated clocks are also available through an output pin.

# **KEY FEATURES**

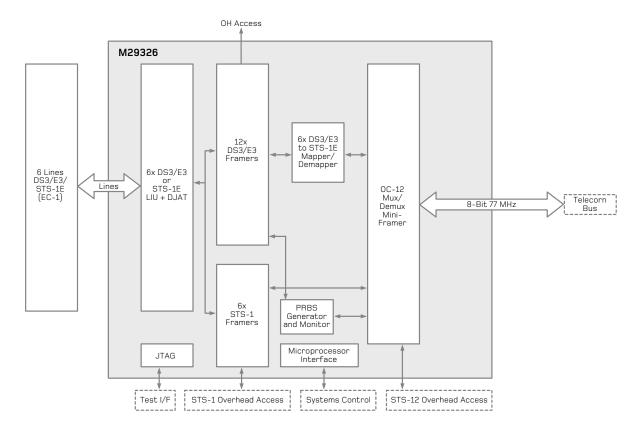
- High integration LIUs with DJAT, DS3/E3 framers/mappers, STS-1 framers/mappers, STS-12/STM-4 framer
- Flexibility mix DS3, E3 and STS-1 on one device
- Easy implementation TAP software + high integration = faster time-to-market
- Parallel 8-bit, 77.76 MHz TDM telecom bus
- Embedded CLADs for supported line rates
- Pattern generator/detector for BERT
- Comprehensive loopbacks

In addition, the M29323/6 supports pseudo-random bit sequence (PRBS) testing and a full set of loopback functions at different functional blocks.

Using the telecom application package (TAP) software to abstract the physical registers, developers can easily implement the M29323/6 solution, reducing design time.

The M29323/6 are offered in a 27mm FCBGA package.





M29326 Functional Block Diagram

## **Product Features**

- 3/6 DS3/E3/STS-1 LIUs with jitter attenuation/desynchronization
- -Adaptive receive equalizer enables > 1800 ft of cable reach
- Programmable transmit pulse mask configuration
- Dynamic loop bandwidth to comply with all standard intrinsic and output jitter requirements
- 6/12 DS3/E3 framers support DS3-M13, DS3-M23, DS3 C-bit parity E3-G.751, E3-G.832
- 3/6 DS3/E3 mappers/demappers supporting DS3/VC-3/AU-3; DS3/TUG-3/AU-4; E3/VC-3/AU-3; E3/TUG-3/AU-4

- 3/6 STS-1 SONET/SDH framers support transport overhead access; includes monitor and generator
- STS-12/STM-4 SONET/SDH TDM supporting mapping/demapping of 12 STS-1E or AU-3 into/from STS 12/STM-4 frame
- Pointer processing
- Overhead insertion and extraction
- Parallel 77.76 MHz x 8-bit Telecom bus interface
- Synchronous 16-bit microprocessor interface bus at 30-77 MHz bus rate
- Glueless connection to Motorola MPC860

- Local (source) and remote (line) capability at various internal points in the device
- PRBS detector and generator supporting framed and unframed modes
- JTAG (IEEE 1149.1) boundary scan
- Single rail 1.8 V core supply with 3.3 V LvTTL I/O, 1.8V LVDS I/O
- Embedded CLADs internally generating the DS3, E3, STS-1 clocks
- -40C to +85C operation

### **Applications**

- · SONET/SDH ADM/OED
- MSPP
- Optical ADM
- DCS
- NGDLC
- Class V voice switch

#### **Ordering Information**

- M29323-12P
- M29326-12P

### www.mindspeed.com/salesoffices

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