SONY

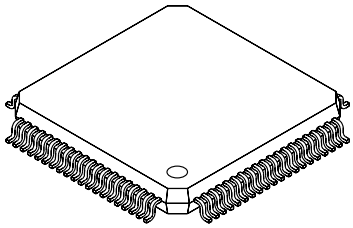
CXD1945R

IEEE 1394 3-port 100/200Mbps Cable Transceiver/Arbiter

Description

The CXD1945R is a physical layer IC conforming to IEEE 1394-1995 that supports transfer speeds of 200/100Mbit/s. This chip has three ports for 1394 cable interface, an interface to a Link layer IC, received packet data regeneration repeat, and arbitration/bus initialization logic. The CXD1945R supports IEEE 1394 protocol physical layer functions.

80 pin LQFP (Plastic)



Features

- Low voltage amplitude differential transceiver conforming to IEEE 1394-1995
- Supports 196.603Mbit/s and 98.304Mbit/s data rates
- Active line detection function for when a port is connected to an active node
- Automatic shutdown function for inactive ports to save power
- Bus initialization and arbitration state machine logic
- Resynchronization of received data to local clock
- Link-On packet recognition
- DS Link encoding/decoding
- Built-in 196.603MHz PLL
- Cable Power Status detects drops in the power supply from the cable
- Link Power Status detects the Link layer IC power status
- Supports Configuration Manager Capable and Power Class definition pins
- 3-port independent TpBias

Applications

Digital camera, digital VCR, digital audio, electronic musical instruments, scanner, printer, various storage devices

Absolute Maximum Ratings

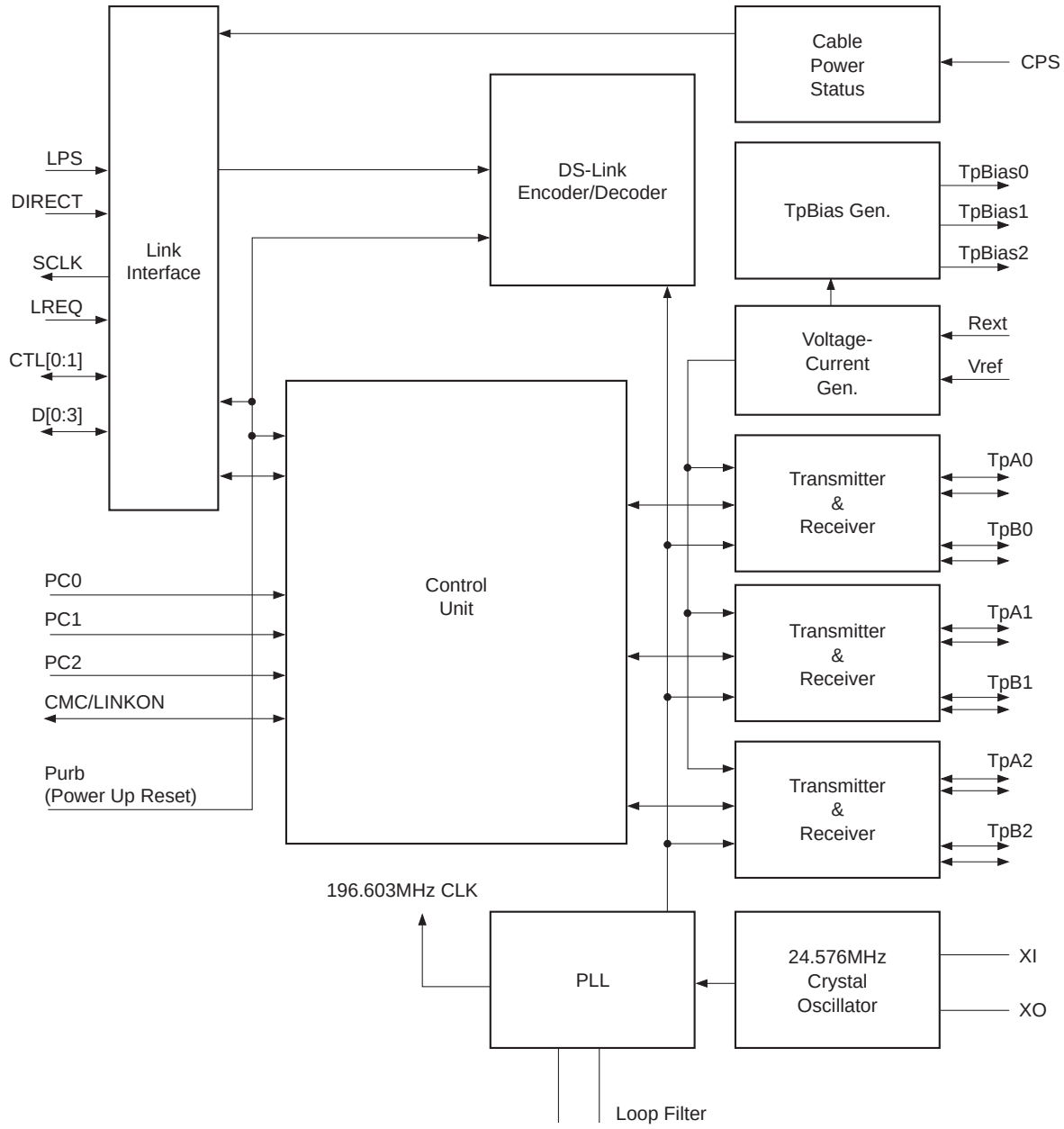
• Supply voltage	V_{DD}	–0.5 to +5.0	V
• Input voltage	V_{IN}	–0.5 to V_{DD} + 0.5	V
• Output voltage	V_{OUT}	–0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

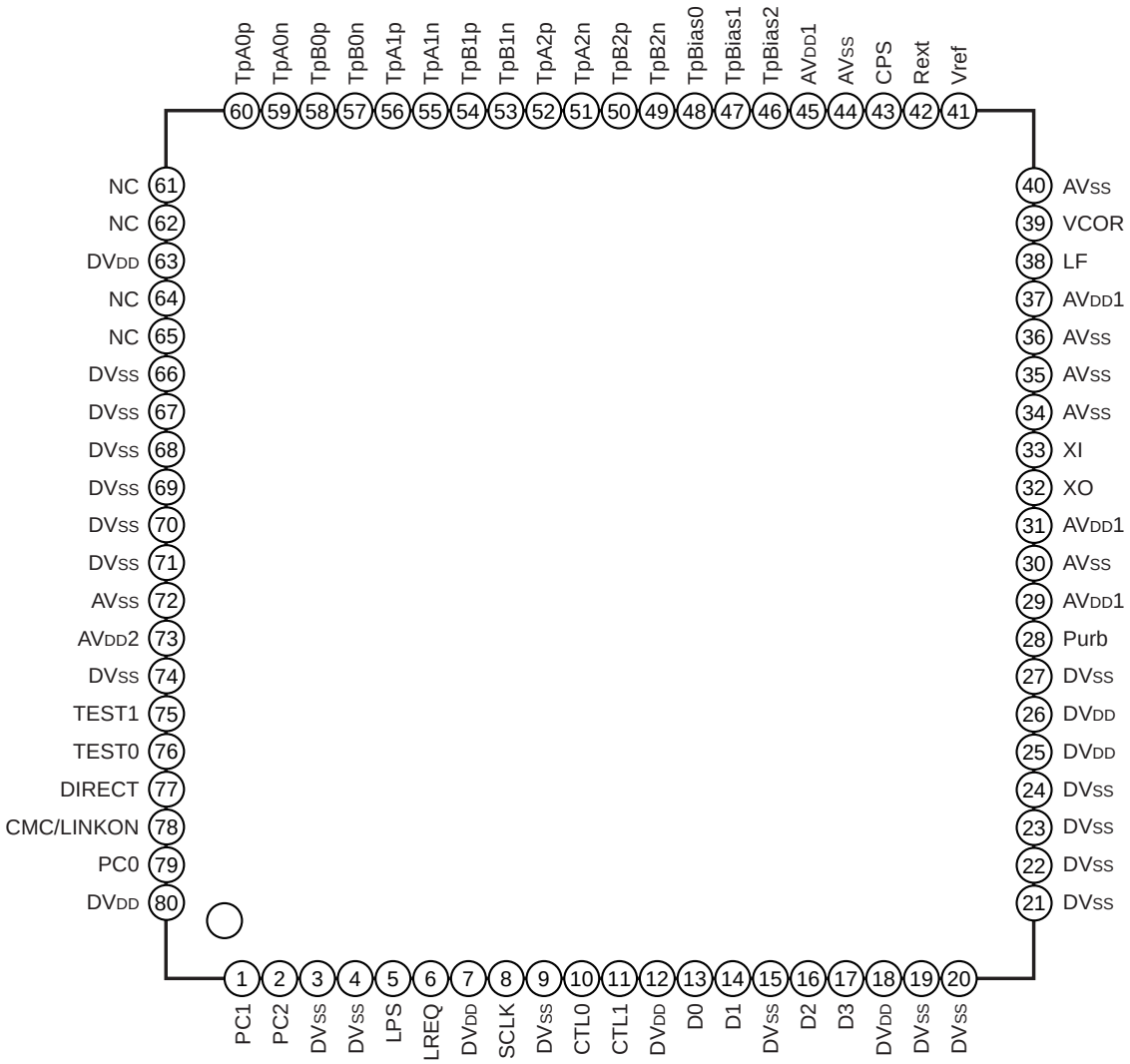
• Supply voltage	V_{DD}	3.0 to 3.6	V
• Input voltage	V_{IN}	0 to V_{DD}	V
• Output voltage	V_{OUT}	0 to V_{DD}	V
• Ambient temperature	T_A	0 to +70	°C

E98643-PS

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
79, 1, 2	PC[0:2]	I	Power Class [0:2] The POWER_CLASS field of the Self-ID packet reflects the status of this pin during the Self-ID period. Connect to DV_{SS} or DV_{DD} depending on the setting.
3, 4, 9, 15, 19 to 24, 27, 66 to 71, 74	DV_{SS}		Digital ground.
5	LPS	I	Link Power Status. Monitors the Link power ON/OFF status. Link power OFF is detected if this pin is low for 2.56µs. Link power ON is detected if this pin is high for 80ns. (See 3-1-2.)
6	LREQ	I	Link request. The Link reads/writes the PHY register and performs bus requests via this pin. (See 3-1-3.)
7, 12, 18, 25, 26, 63, 80	DV_{DD}		Digital power supply.
8	SCLK	O	49.152MHz Link system clock. The PHY-Link interface and cable interface are synchronized to SCLK.
10, 11	CTL[0:1]	I/O	PHY-Link interface control signal. (See 3-1-3.)
13, 14, 16, 17	D[0:3]	I/O	PHY-Link interface data signal. (See 3-1-3.)
28	Purb	I	External capacitor connection for Power Up Reset. Connect to DV_{SS} via 0.1µF. The reset period is a minimum 15ms. The internal reset state machines are all initialized during the reset period. (See 3-4.)
29, 31, 37, 45	$AV_{DD}1$		Analog power supply 1. Power supply for all blocks other than the cable interface driver.
30, 34 to 36, 40, 44, 72	AV_{SS}		Analog ground.
32, 33	XO, XI	I/O	Crystal connection. Crystal oscillator connection. The oscillator output frequency must be 24.576MHz ±100ppm. Use a crystal with an accuracy of 50ppm when a 10pF load is connected. (See 3-3.)
38	LF	O	External loop filter connection.
39	VOCR	I	
41	Vref	I	External reference resistor connection. Connect to AV_{SS} via 18kΩ + 510Ω (±1%) external resistors and 0.01µF.
42	Rext	I	External reference resistor connection. Connect to AV_{SS} via 11kΩ + 620Ω (±1%) external resistors.

Pin No.	Symbol	I/O	Description
43	CPS	I	Cable Power Status detection. Connect to Cable Power (Vp) via 220kΩ (±5%). When not used, connect to $AV_{DD}1$. (See 3-2-3.)
48 to 46	TpBias[0:2]	O	Cable bias output. Connect to AV_{SS} via 0.33µF.
57, 53, 49	TpB[0:2]n	I/O	Arbitration/Speed Signal/Data output. Arbitration/Strobe input. Reverse phase I/O.
58, 54, 50	TpB[0:2]p	I/O	Arbitration/Speed Signal/Data output. Arbitration/Strobe input. Forward phase I/O.
59, 55, 51	TpA[0:2]n	I/O	Arbitration/Strobe output. Arbitration/Speed Signal/Data input. Reverse phase I/O.
60, 56, 52	TpA[0:2]p	I/O	Arbitration/Strobe output. Arbitration/Speed Signal/Data input. Forward phase I/O.
61, 62, 64, 65	NC		No connected. Leave open or connect to ground (DV_{SS}).
73	$AV_{DD}2$		Analog power supply 2. Power supply for cable interface driver.
76, 75	TEST[0:1]	I	Test mode control. Connect to DV_{DD}.
77	DIRECT	I	PHY-Link interface operating mode setting. Connect to DV_{DD}. The CXD1945R supports only DC connection.
78	CMC/ LINKON	I/O	Configuration Manager Capable setting/Link-On signal output. The CONTENDER field of the Self-ID packet reflects the status of this pin during the Self-ID period, and then this pin functions as the Link-On output after that. Link-On is a 6.144MHz, duty 50% AC signal. (See 3-1-4.)

Electrical Characteristics

1. DC Characteristics

Electrical characteristics under the Recommended Operating Conditions (unless otherwise specified)

Link Interface

(V_{SS} = 0V)

Symbol	Item	Pin	Conditions	Min.	Typ.	Max.	Unit
V_{T+}	Input Schmitt rise threshold value	LREQ, CTL[0:1], D[0:3]		$V_{DD}/2 + 0.2$		$V_{DD}/2 + 1.0$	V
V_{T-}	Input Schmitt fall threshold value	LREQ, CTL[0:1], D[0:3]		$V_{DD}/2 – 1.0$		$V_{DD}/2 – 0.2$	V
V_{IH}	High level input voltage	LPS, TEST[0:1], DIRECT, PC[0:2], CMC/LINKON		$V_{DD} – 1.0$			V
V_{IL}	Low level input voltage	LPS, TEST[0:1], DIRECT, PC[0:2], CMC/LINKON				1.0	V
I_{IH}	High level input current	LREQ, CTL[0:1], D[0:3]	$V_{IH} = V_{DD}$	–10			µA
		LPS, TEST[0:1], DIRECT, PC[0:2], CMC/LINKON	$V_{IH} = V_{DD}$	–10			
I_{IL}	Low level input current	LREQ, CTL[0:1], D[0:3]	$V_{IL} = V_{SS}$			10.0	µA
		LPS, TEST[0:1], DIRECT, PC[0:2], CMC/LINKON	$V_{IL} = V_{SS}$			10.0	
V_{OH}	High level output voltage	SCLK, CTL[0:1], D[0:3]	I_{OH} = –10mA	$V_{DD} – 0.5$			V
		CMC/LINKON	I_{OH} = –6mA	$V_{DD} – 0.5$			
V_{OL}	Low level output voltage	SCLK, CTL[0:1], D[0:3]	I_{OL} = 10mA			0.5	V
		CMC/LINKON	I_{OL} = 6mA			0.5	
I_{DD}	Dynamic current consumption		V_{DD} = 3.3V		128.0		mA

Cable Interface

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{OD}	Differential output amplitude	Load 55Ω	175		265	mV
V_{TPBIAS}	TpBias output voltage	Source 3mA, Sync 1.3mA	1.72		1.92	V
I_{CM}	Tp common mode current	Driver disabled (Z state) Drivers other than the speed signal enabled	–25		5	µA
			–0.18		0.18	mA
I_{SPD}	TpB200Mbit speed signal		2.76		4.6	mA
Z_{DIFFZ}	Differential input impedance	Driver disabled (Z state)	21.0			kΩ
					6.9	pF
Z_{DIFFEN}	Differential input impedance	Driver enabled	3.4			kΩ
					6.9	pF
C_{CM}	Common mode input capacitance	Tp pins shorted Z state drivers			27.6	pF
$V_{T\ NoConn}$	Inactive line threshold voltage	TPB common mode voltage	0.64		0.96	V
$V_{T\ Cpwd}$	CPS threshold voltage	Vp pins (R = 220kΩ)	6.0		7.6	V

2. AC Characteristics

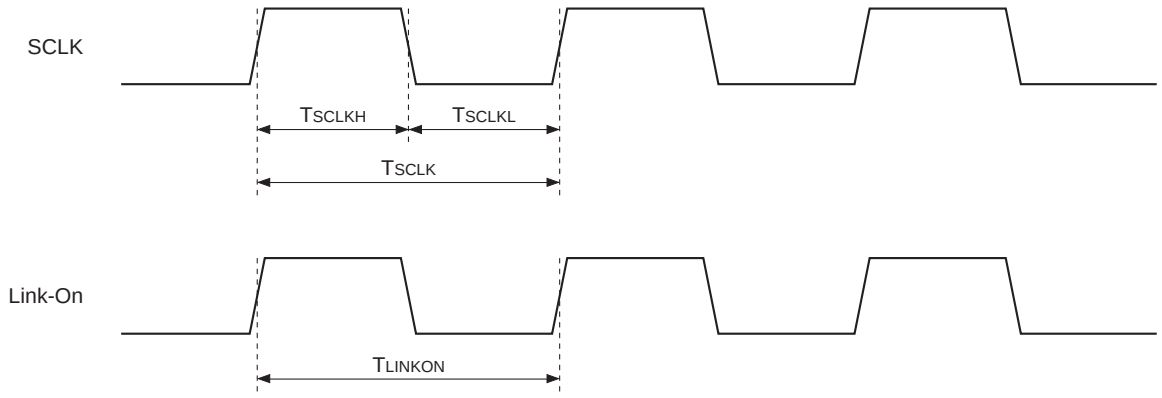
Link Interface

Symbol	Item	DC connection			Unit
		Min.	Typ.	Max.	
T_{SU}	D, CTL and LREQ setup time	5			ns
T_{H}	D, CTL and LREQ hold time	1			ns
T_{D}	D and CTL output timing time	0		7	ns
T_{SCLK}	SCLK cycle time	20			ns
T_{SCLKH}	SCLK high level time	8		12	ns
T_{SCLKL}	SCLK low level time	8		12	ns
T_{LINKON}	Link-On cycle time	160			ns

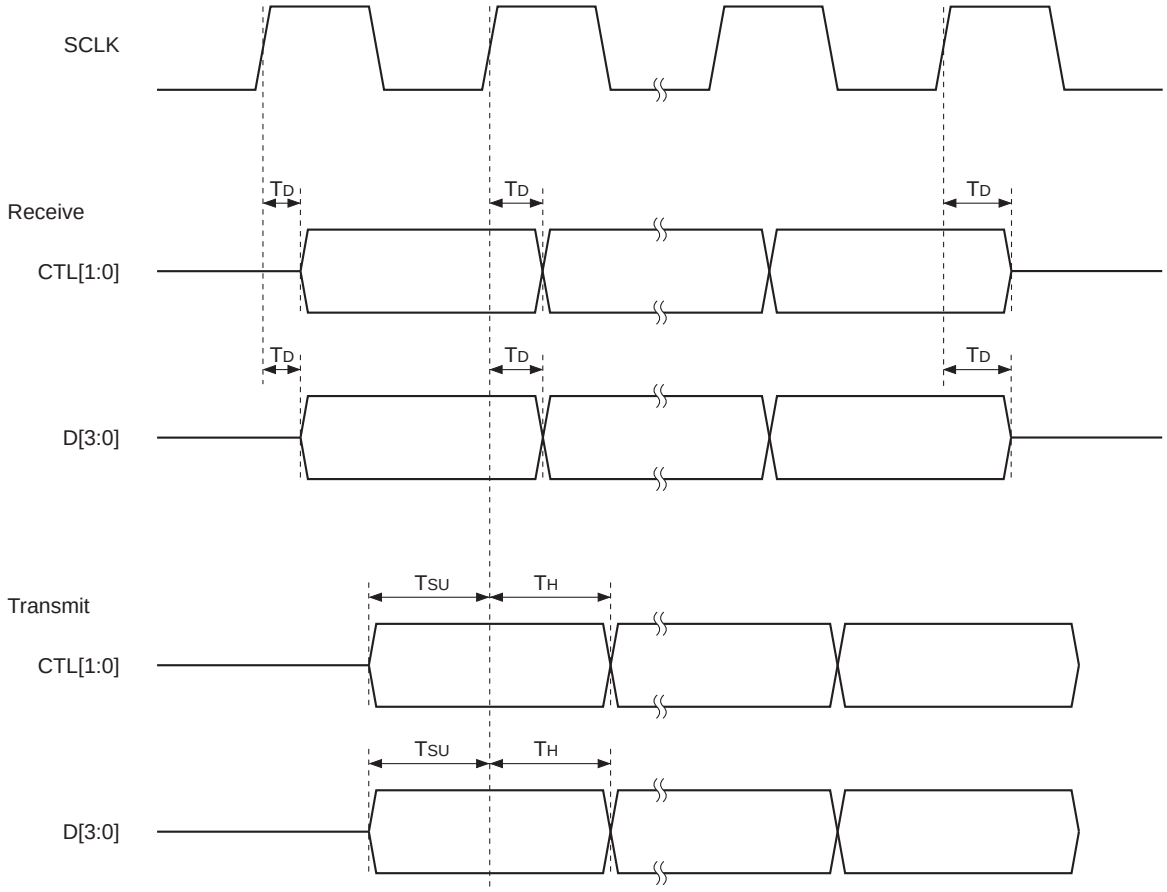
Twisted Pair Interface

Symbol	Item	Conditions	Min.	Max.	Unit
$T_{TJITTER}$	TpA and TpB transfer jitter			±0.25	ns
T_{TSKEW}	Skew between TpA strobe and TpB data transfer			±0.15	ns
T_{TRF}	TpA and TpB transfer rise and fall	From 10% to 90%, via 55Ω and 10pF		2.2	ns

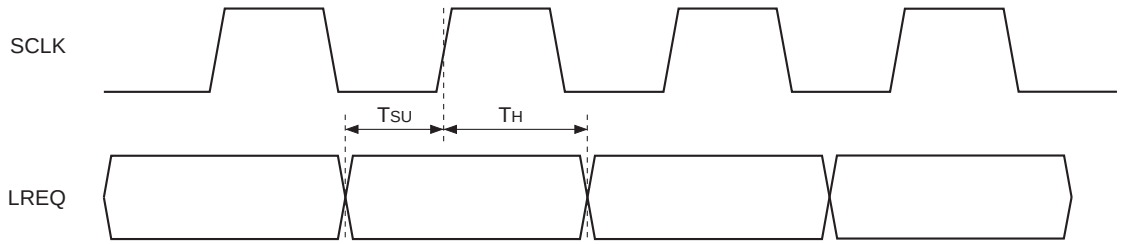
Link Interface AC Characteristics (SCLK, Link-On)



Link Interface AC Characteristics (CTL, D)



Link Interface AC Characteristics (LREQ)



[1] Control Register

1-1. Register Access Method

Normally the CXD1945R registers are accessed from the Link layer IC. See "3-1-3-1. LREQ" for the detailed access method.

1-2. Register Contents

1-2-1. Register0

Address 00h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00h	Physical ID						R	CPS

bits 7 to 2: Physical ID: Physical Node ID (R – initial value: 00h)
Indicates the ID of this node determined during the Self-ID period.
These bits are initialized by a bus reset and determined when the Self-ID packet is transmitted during the Self-ID period.
The register address "00h" including these bits is automatically output to the Link interface as the status transmission after transmitting the Self-ID packet.

bit 1: R: root indicator (R – initial value: 0h)
Indicates that this node is the root when "1".
This bit is initialized by a bus reset and determined during the Tree-ID period.

bit 0: CPS: Cable Power Status (R – initial value: CPS pin setting)
Reflects the CPS pin value to indicate the cable power status. Indicates that power is supplied from the cable when "1".

1-2-2. Register1

Address 01h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
01h	RHB	IBR	GC					

bit 7: RHB: Root Hold Bit (R/W – initial value: 0h)
Requests that this node become the root at the next bus reset when "1".
This bit is also automatically set by PHY configuration packet transmit/receive.

bit 6: IBR: Indicates Bus Reset (R/W – initial value: 0h)
Bus reset is initiated immediately when set to "1".
This bit is initialized by a bus reset.

bits 5 to 0: GC: Gap Count (R/W – initial value: 3Fh)
This is the Gap Count value.
These bits are also automatically set by PHY configuration packet transmit/receive.
After these bits are set, the value is held by the first bus reset, but initialized by the next bus reset.

1-2-3. Register2

Address 02h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
02h	SPD		Reserved		NP			

bits 7 to 6: SPD: Speed (R – initial value: 01b)
Indicates the maximum transfer speed supported by the CXD1945R. "01b" is read.

bits 5 to 4: Reserved (R – initial value: 0h)
Normally "0" (00b) is read.

bits 3 to 0: NP: Number of Ports (R – initial value: 3h)
Indicates the number of ports possessed by the CXD1945R. Normally "3" (0011b) is read.

1-2-4. Register3

Address 03h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
03h	AStat0		BStat0		Ch0	Con0	Reserved	

bits 7 to 6: AStat0: Status of TpA0 (R – initial value: 0h)
Indicates the TpA0 status. The meanings of the values are as follows.
11b: Z
01b: 1
10b: 0
00b: invalid

bits 5 to 4: BStat0: Status of TpB0 (R – initial value: 0h)
Indicates the TpB0 status. The meanings of the values are as follows.
11b: Z
01b: 1
10b: 0
00b: invalid

bit 3: Ch0: Child (R – initial value: 0h)
Indicates that port 0 is a child when "1", or a parent when "0".
This bit is initialized by a bus reset and determined during the Tree-ID period.

bit 2: Con0: Connected (R – initial value: 0h)
Indicates that port 0 is connected to an opposing node when "1".
The CXD1945R has a built-in connection debounce circuit, so bus reset is initiated after waiting for the 341ms period from the time cable connection is detected until the connection stabilizes. Bus reset is initiated immediately when cable disconnection is detected.
This bit is determined during the bus reset period.

bits 1 to 0: Reserved (R – initial value: 0h)
Reserved.

1-2-5. Register4

Address 04h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
04h	AStat1		BStat1		Ch1	Con1	Reserved	

bits 7 to 6: AStat1: Status of TpA1 (R – initial value: 0h)
Indicates the TpA1 status. The meanings of the values are as follows.
11b: Z
01b: 1
10b: 0
00b: invalid

bits 5 to 4: BStat1: Status of TpB1 (R – initial value: 0h)
Indicates the TpB1 status. The meanings of the values are as follows.
11b: Z
01b: 1
10b: 0
00b: invalid

bit 3: Ch1: Child (R – initial value: 0h)
Indicates that port 1 is a child when "1", or a parent when "0".
This bit is initialized by a bus reset and determined during the Tree-ID period.

bit 2: Con1: Connected (R – initial value: 0h)
Indicates that port 1 is connected to an opposing node when "1".
The CXD1945R has a built-in connection debounce circuit, so bus reset is initiated after waiting for the 341ms period from the time cable connection is detected until the connection stabilizes. Bus reset is initiated immediately when cable disconnection is detected.
This bit is determined during the bus reset period.

bits 1 to 0: Reserved (R – initial value: 0h)
Reserved.

1-2-6. Register5

Address 05h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
05h	AStat2		BStat2		Ch2	Con2	Reserved	

bits 7 to 6: AStat2: Status of TpA2 (R – initial value: 0h)
Indicates the TpA2 status. The meanings of the values are as follows.
11b: Z
01b: 1
10b: 0
00b: invalid

bits 5 to 4: BStat2: Status of TpB2 (R – initial value: 0h)
Indicates the TpB2 status. The meanings of the values are as follows.
11b: Z
01b: 1
10b: 0
00b: invalid

bit 3: Ch2: Child (R – initial value: 0h)
Indicates that port 2 is a child when "1", or a parent when "0".
This bit is initialized by a bus reset and determined during the Tree-ID period.

bit 2: Con2: Connected (R – initial value: 0h)
Indicates that port 2 is connected to an opposing node when "1".
The CXD1945R has a built-in connection debounce circuit, so bus reset is initiated after waiting for the 341ms period from the time cable connection is detected until the connection stabilizes. Bus reset is initiated immediately when cable disconnection is detected.
This bit is determined during the bus reset period.

bits 1 to 0: Reserved (R – initial value: 0h)
Reserved.

1-2-7. Register6

Address 06h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
06h	LoopInt	CPStatInt	CPStat	IDidit	Reserved			

bit 7: LoopInt: Loop Interrupt (R/W – initial value: 0h)
Indicates that the bus forms a Loop when "1".
This bit is cleared by a hardware reset or by writing "0".

bit 6: CPStatInt: Cable Power Status Interrupt (R/W – initial value: 0h)
Indicates that the power supplied from the cable has dropped when "1".
This bit is cleared by a hardware reset or by writing "0".

bit 5: CPStat: Cable Power Status (R/W – initial value: CPS pin setting)
Reflects the CPS pin value to indicate the cable power status. Indicates that power is supplied from the cable when "1".
This bit has the same contents as the CPS bit (address "00h" bit 0).

bit 4: IDidIt: Indicates Bus Reset initiated (R/W – initial value: 0h)
Indicates that this node initiated the previous bus reset when "1".
This bit is the same as the i (initiated_reset) field of the Self-ID packet.
This bit is determined during bus reset.

bits 3 to 0: Reserved (R – initial value: 0h)
Normally "0000b" is read.

1-2-8. Register7

Address 07h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
07h	Reserved							

bits 7 to 0: Reserved (R – initial value: 0h)
Reserved.

1-2-9. Register8

Address 08h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
08h	Reserved							

bits 7 to 0: Reserved (R – initial value: 0h)
Reserved.

1-2-10. Register9

Address 09h

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
09h	Reserved							ISBR

bits 7 to 1: Reserved (R – initial value: 0h)
Reserved.

bit0: ISBR: Initiate Short (Arbitrated) Bus Reset (R/W – initial value: 0h)
An arbitration short bus reset is initiated when this bit is set to "1".
This bit is initialized by a bus reset.

1-3. List of Registers

Address	7	6	5	4	3	2	1	0
00h	Physical ID						R	CPS
01h	RHB	IBR	GC					
02h	SPD		Reserved		NP			
03h	AStat0		BStat0		Ch0	Con0	Reserved	
04h	AStat1		BStat1		Ch1	Con1	Reserved	
05h	AStat2		BStat2		Ch2	Con2	Reserved	
06h	LoopInt	CPStatInt	CPStat	IDidit	Reserved			
07h	Reserved							
08h	Reserved							
09h	Reserved							ISBR

Table 1-1. List of Registers

[2] Data Format

2-1. Self-ID Packet

The Self-ID packet output by the CXD1945R is comprised of 2 quadlets, and follows the format shown in Fig. 2-1.

1	0	phy_ID		0	L	gap_cnt	sp	del	c	pwr	p0	p1	p2	i	m
logical inverse of first quadlet															

Fig. 2-1. Self-ID Packet Format

phy_ID: physical_ID field
This is the physical_ID of the CXD1945R.

L: Link_active field
Reflects the LPS pin status during Self-ID packet transmit.

gap_cnt: gap_count field
Reflects the PHY register1 GC value.

sp: PHY_SPEED field
00 = 98.304Mbps
01 = 98.304 and 196.608Mbps
10 = 98.304, 196.608 and 393.216Mbps
11 = Reserved
Available speeds are saved. Fixed to "01" for the CXD1945R.

del: PHY_DELAY field
00 = 144ns or less (to 14/BASE_RATE)
01 to 11 = Reserved
The repeater worst case delay time is saved. Fixed to "00" for the CXD1945R.

C: CONTENDER field. CMC/LINKON pin setting.
Reflects the CMC/LINKON pin setting.

pwr: POWER_CLASS field
Reflects the PC[2:0] pin setting. Defined as follows for IEEE 1394-1995.
000 = The node does not require power supply.
001 = The node has its own power supply and can feed a minimum of 15W.
010 = The node has its own power supply and can feed a minimum of 30W.
011 = The node has its own power supply and can feed a minimum of 45W.
100 = The node consumes a maximum of 1W of power from the cable.
101 = The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 2W to enable the Link and upper layers.
110 = The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 5W to enable the Link and upper layers.
111 = The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 9W to enable the Link and upper layers.

p0 to p2: Port status field

11 = Connected to the child node.

10 = Connected to the parent node.

01 = Not connected to another PHY.

00 = This PHY is not offered.

Indicates the port status.

i: initiated_reset field

Indicates that this node issued the present bus reset.

m: more_packets field

This field is set to "1" when transmitting multiple Self-ID packets, but it is fixed to "0" for the CXD1945R.

[3] Description of Functions

3-1. Link Chip Interface

3-1-1. Connection Method

3-1-1-1. DC Connection

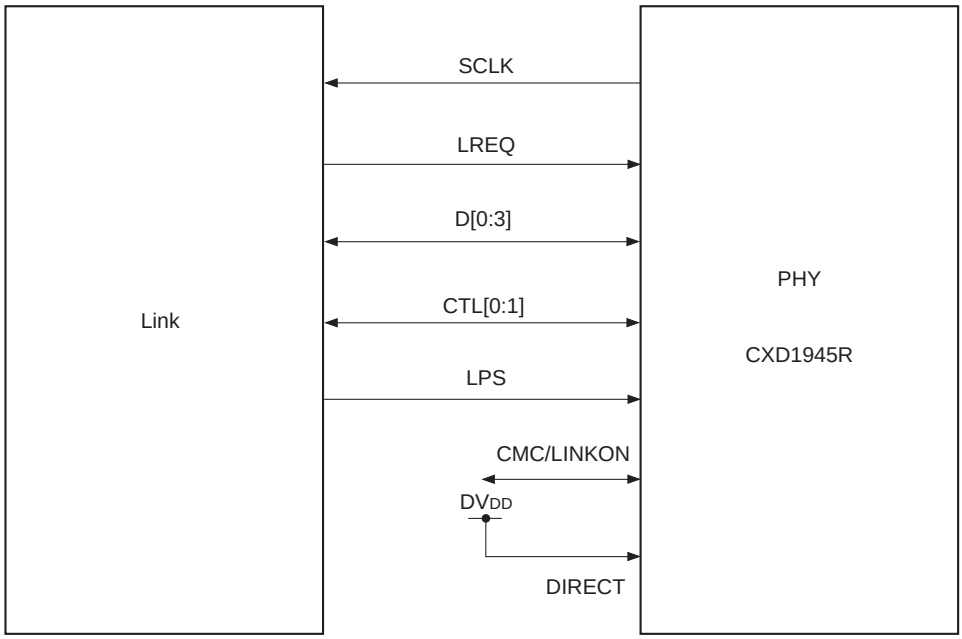


Fig. 3-1. CXD1945R – Link Chip Connection Diagram (DC Connection)

3-1-2. LPS (Link Power Status)

The LPS pin is the input signal for monitoring the power ON/OFF status of the Link connected to the CXD1945R. If the LPS pin is continuously high for a period of 80ns or more, the CXD1945R recognizes that the Link power is ON, activates the PHY-Link interface and outputs SCLK, D and CTL to the Link.
Conversely, if the LPS pin is continuously low for 2.56µs or more, the CXD1945R recognizes that the Link power is OFF, deactivates the PHY-Link interface and stops SCLK, D and CTL output to the Link (Hi-Z). Therefore, packet receive and status output to the Link are not performed during this period, and information is not output after the PHY-Link interface is activated next.
The CXD1945R operates as a repeater during this period.
The L bit in the Self-ID packet is set to "0" during this period.
In addition, if a Link-On packet addressed to this node is received during this period, the Link-On signal is output to the CMC/LINKON pin.
If LPS is set high during Link-On signal output, Link-On signal output stops.
The LPS, SCLK, D and CTL timing is shown in Fig. 3-2.

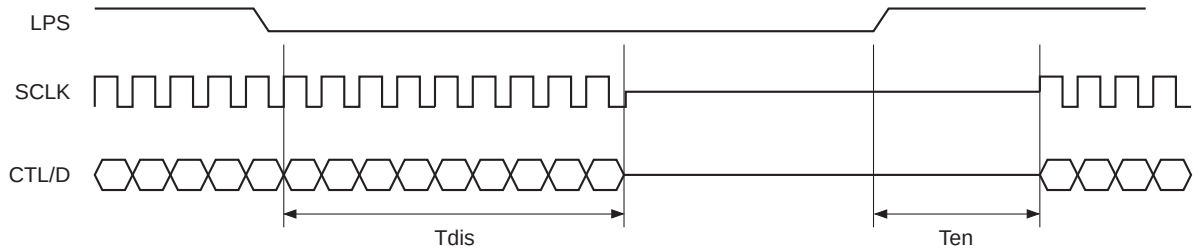


Fig. 3-2. LPS Timing

Symbol	Description	Min.	Max.	Unit
Tdis	Time from when LPS goes low until SCLK, D and CTL go to Hi-Z	2.58	2.6	µs
Ten	Time from when LPS goes low until SCLK, D and CTL become active	61	102	ns

Table 3-1. LPS Timing Constants

3-1-3. Link Interface (LREQ, CTL[0:1], D[0:3])

The PHY-Link interface of the CXD1945R conforms to IEEE Std 1394-1995 Annex J.
The PHY-Link interface performs four operations: request using LREQ, and status transmit, packet transfer and packet receive using CTL. Operations using CTL (operations other than request) are first controlled by PHY.
When the CXD1945R receives a packet, it initiates packet receive operation on a priority basis.
The CTL states and their meanings are given in Tables 3-2 and 3-3.

CTL[0:1]	Name	Description
00b	Idle	Idle status, with no operations. (default mode)
01b	Status	The PHY chip is transferring status information.
10b	Receive	The PHY chip is transferring the received packet contents.
11b	Grant	The PHY chip has granted the PHY-Link interface to the Link chip in order to receive a packet.

Table 3-2. PHY Chip Control Mode 1

After the Link has been granted control of the PHY-Link bus by Grant above, operation switches to the modes shown in Table 3-3.

CTL[0:1]	Name	Description
00b	Idle	The Link chip has completed transfer and released the interface.
01b	Hold	• The Link chip is holding the interface until the data is established for transfer. • The Link chip is requesting another packet transmission, without performing arbitration.
10b	Transmit	The Link chip is transferring the transmit packet data to the PHY chip.
11b	Reserved	Reserved

Table 3-3. PHY Chip Control Mode 2

3-1-3-1. LREQ

The Link chip inputs a serial signal synchronized to SCLK to the LREQ pin in order to access the PHY register or to request packet transmit. This serial signal contains the request type, transfer packet speed, and read/write command information.
The length of the LREQ serial signal differs according to the request type; it is 7 bits for a bus request, 9 bits for a register read request, and 17 bits for a register write request.
This serial signal must transmit a "0" at the end as the stop bit.

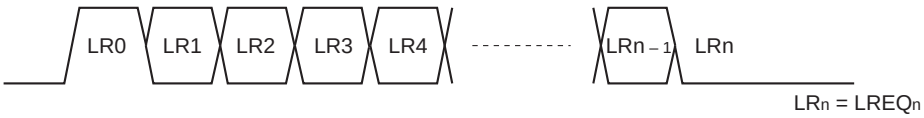


Fig. 3-3. LREQ Stream

Packet transfer requests are performed with a 7-bit length format as shown in Table 3-4.

bit	Name	Description
0	Start Bit	Indicates the start of transfer. Always transfer "1".
1 to 3	Request Type	Indicates the request type shown in Table 3-8.
4 to 5	Request Speed	Indicates the transfer speed of the PHY chip.
6	Stop Bit	Indicates the end of transfer. Always transfer "0".

Table 3-4. Request Format

LREQ[4:5]	Data Rate
00	100Mbps
01	200Mbps

Table 3-5. Speed Format

PHY chip register read requests are performed with a 9-bit length format as shown in Table 3-6. Register write requests are performed with a 17-bit length format as shown in Table 3-7.

bit	Name	Description
0	Start Bit	Indicates the start of transfer. Always transfer "1".
1 to 3	Request Type	Indicates the request type shown in Table 3-8.
4 to 7	Address	Indicates the PHY chip register address to be read.
8	Stop Bit	Indicates the end of transfer. Always transfer "0".

Table 3-6. Read Register Format

bit	Name	Description
0	Start Bit	Indicates the start of transfer. Always transfer "1".
1 to 3	Request Type	Indicates the request type shown in Table 3-8.
4 to 7	Address	Indicates the PHY chip register address to be written.
8 to 15	Data	Indicates the PHY chip register data to be written.
16	Stop	Indicates the end of transfer. Always transfer "0".

Table 3-7. Write Register Format

LREQ[1:3]	Name	Description
000	ImmReq	Immediate request
001	IsoReq	Isochronous request
010	PriReq	Priority request
011	FairReq	Fair request
100	RdReg	Read contents of set register
101	WrReg	Write to set register
110, 111	Reserved	Reserved

Table 3-8. Request Type

Fair requests and priority requests must begin issuing LREQ at least 1 SCLK or more after CTL becomes Idle. If CTL becomes Receive either during or after the Link issues these requests, the CXD1945R cancels the requests. Therefore, the Link must reissue these requests when CTL becomes idle next.

The Cycle Master Link issues PriReq in order to transfer the Cycle Start packet.

The Link issues IsoReq in order to transmit an isochronous packet. IsoReq must be issued either during transmit or receive of the Cycle Start packet or an isochronous packet.

The CXD1945R clears IsoReq only when it wins at arbitration and transmits Grant to the Link, detects a subaction gap, or when a bus reset occurs.

The Link issues ImmReq during packet receive in order to transmit an Ack packet. The Link must confirm the destination_ID of the received packet, and after confirming that the packet is addressed to this node, must issue ImmReq immediately in order to satisfy ACK_RESPONSE_TIME. The CXD1945R acquires the bus and returns Grant to the Link immediately after completing packet receive. If the Link discovers a CRC error, the Link must not return any data to that Grant.

When a register write request is received, the CXD1945R immediately writes the data for that address.

When a register read request is received, the CXD1945R outputs the data at that address to the Link as a status transmission. If this output is interrupted by packet receive, the CXD1945R repeats the status output from the first bit until the status output is completed.

When the CXD1945R receives a bus request (FairReq, PriReq, IsoReq, ImmReq), further bus requests are ignored until the received request is canceled by packet receive, packet transmit, subaction gap (only for IsoReq, ImmReq), etc.

If the CXD1945R receives the next register read request before the present register read request is completed, this operation is unstable.

All bus requests are cleared by a bus reset.

3-1-3-2. Status Output

The CXD1945R outputs the information shown in Table 3-9 to the Link interface as the status output. The CXD1945R asserts "01b" to the CTL pin and outputs the information to the D[0:1] pins. The CTL pin outputs "01b" during the status output period.

The CXD1945R normally outputs only the first 4 bits required by the Link state machines as the status output. (Arbitration Reset Gap, Subaction Gap, Bus Reset, PHY interrupt)

However, when a register read request is received from the Link, all of the status information is output as the return value. Also, when the CXD1945R finishes sending its own Self-ID packet during the Self-ID period (when the CXD1945R's physical_ID is established), it automatically performs status output of the PHY register information at address "00h" including its own physical_ID to the Link.

If status output is interrupted by packet receive, etc., that status information is output repeatedly according to the following rules.

- Information output before the interruption is cleared.
- If the information to be output was already output before the interruption, that status output is not repeated.
- Status output is basically performed in 4-bit/16-bit units.

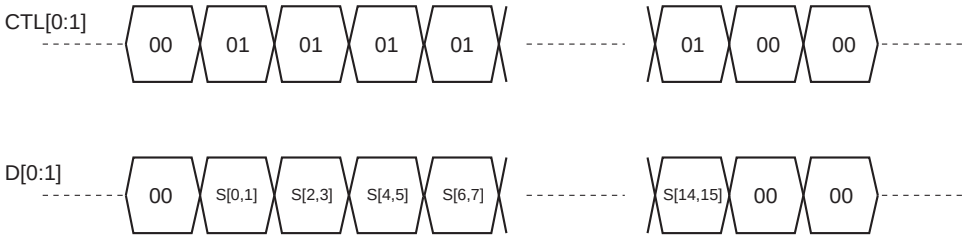


Fig. 3-4. Status

bit	Name	Description
0	Arbitration Reset Gap	Arbitration reset gap detected
1	Subaction Gap	Subaction gap detected
2	Bus Reset	Bus reset detected
3	PHY Interrupt	Interrupt to host requested
4 to 7	Address	Address of PHY register returning the status
8 to 15	Data	Status data

Table 3-9. Status Format

The CXD1945R performs status output as a Phy interrupt in the following case.

- When the bus configuration is detected as a loop

3-1-3-3. Transmit

The CXD1945R performs arbitration when it receives a bus request from the Link. If the CXD1945R wins at this arbitration, it returns Grant (11b) and then Idle to the CTL pin for 1 SCLK cycle each as the Grant to the Link, and then grants CTL and D control to the Link.

After that, the Link inputs Transmit (10b) or Hold (01b) to CTL and controls the PHY-Link interface. However, note that the CXD1945R allows the Link to input Idle (00b) for only 1 SCLK first to prevent data collision on the CTL bus. (See Fig. 3-5.)

The Link can input Hold (01b) to hold the bus until the transfer data is ready, but this hold time cannot exceed the MAX_BUS_HOLD time.

Fig. 3-5. Transmit

After the last bit of the packet data has been input, the Link inputs Idle (00b) or Hold (01b) for 1SCLK cycle and then inputs Idle for 1SCLK cycle. After that, the CXD1945R controls the PHY-Link interface.

The Hold (01b) bit is used to transfer the next packet without releasing the serial bus after the Link completes packet transfer. When the CXD1945R detects the Hold bit, it waits for the MIN_PACKET_SEPARATION time and then outputs Transmit to the CTL pin again for the Link. The Link then performs packet transfer operation in the same manner as above.

This Hold operation is used when transferring a response packet after Ack packet transmit, and when transferring multiple isochronous packets during the same isochronous cycle. (Subaction concatenation)

However, note that in this case the CXD1945R recognizes that the packet speed for the second and subsequent packets is the same as the initial packet speed.

3-1-3-4. Receive

When the CXD1945R receives a packet, it outputs Receive (10b) to the CTL pin and "1" to the D pin for the Link. After that the CXD1945R outputs the speed code (SP) and commences packet data output. The CXD1945R continues asserting Receive (10b) to the CTL pin until data receive is completed.

After the CXD1945R asserts Receive, the receive operation may complete without outputting the packet data.

If the Link supports only 100Mbps, the speed code (SP) must be checked and 200Mbps receive packet data ignored.

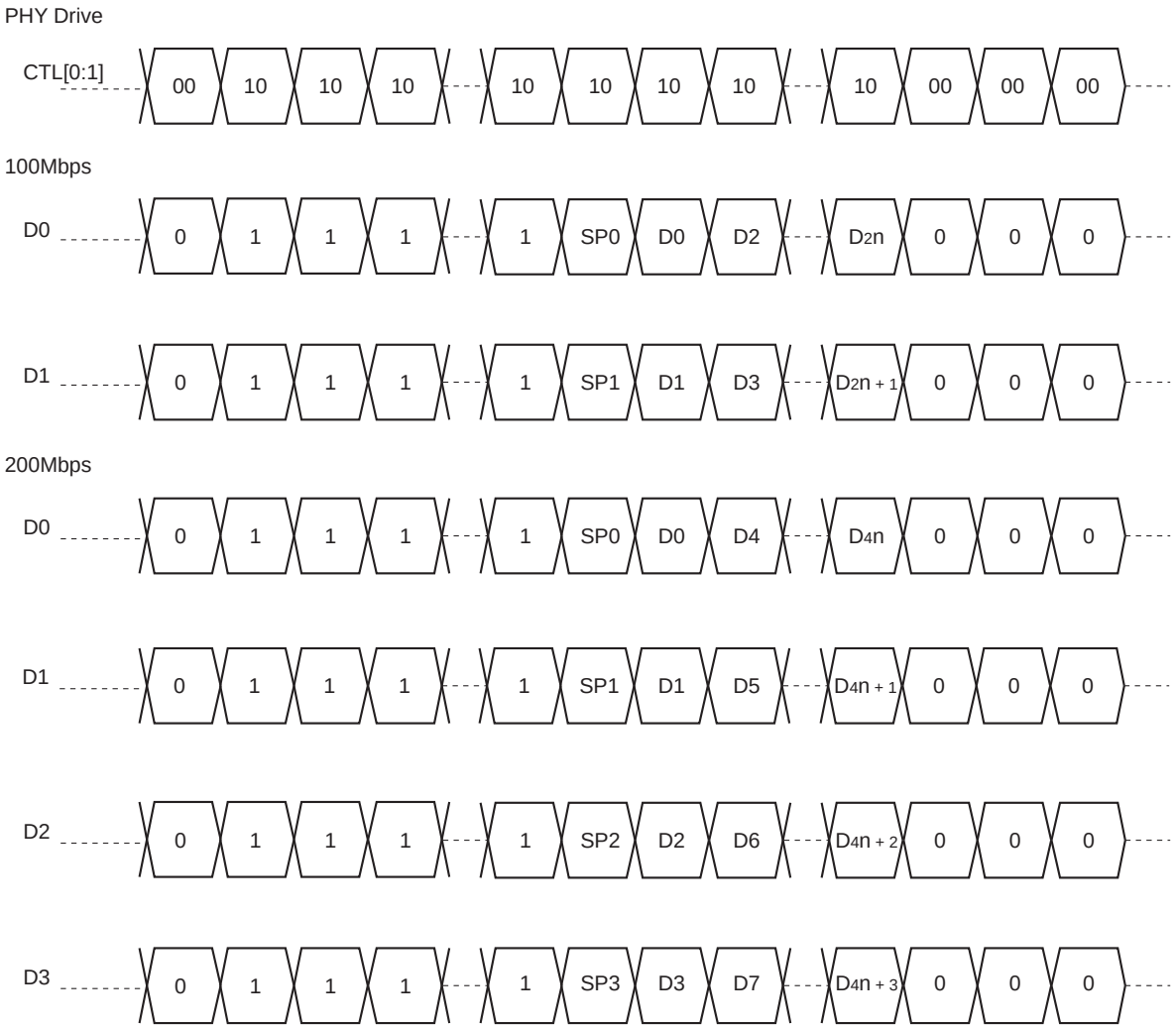


Fig. 3-6. Receive

SP[0:3]	Data Rate
00XX	100Mbps
0100	200Mbps

Table 3-10. Speed Code (SP[0:3])

3-1-4. CMC/LINKON Pin Connection

This pin is normally used as the CMC (Configuration Manager Capable) input pin. The value input here is reflected to the c (CONTENDER) field in the Self-ID packet.
When CMC is high, this indicates that this node has Bus Manager functions.
This pin also functions as the Link-On signal output pin. Therefore, it must be pulled up or down to DV_{DD} or DV_{SS} by a 10kΩ resistor as shown in Figs. 3-7 and 3-8.
The Link-On signal is an AC signal with a frequency of 6.144MHz and a duty of 50%, and is output when a Link-On packet addressed to this node is received while LPS is low and the CXD1945R recognizes the Link power as being OFF. Output of this signal starts after the Link-On packet is received and continues until either LPS goes high and the CXD1945R recognizes the Link power as being ON or a bus reset occurs.
The CMC/LINKON connection when CMC = 1 is shown in Fig. 3-7, and when CMC = 0, in Fig. 3-8.

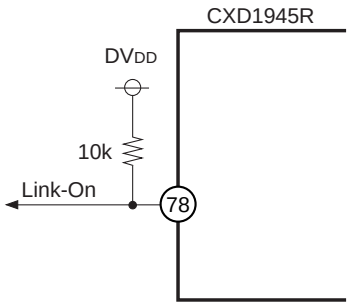


Fig. 3-7. CMC/LINKON Pin when CMC = 1

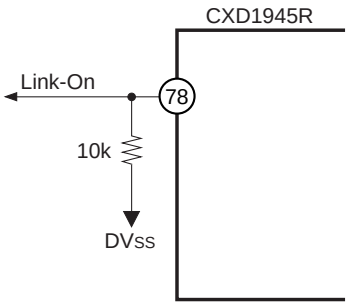


Fig. 3-8. CMC/LINKON Pin when CMC = 0

3-1-5. DIRECT

This pin inputs the PHY-Link interface connection information.
If the PHY-Link interface is DC connected, this pin is set high.
The CXD1945R does not support AC connection.

3-2. Cable Interface

3-2-1. Cable Interface Circuit

Fig. 3-9 shows the cable interface connection circuit.

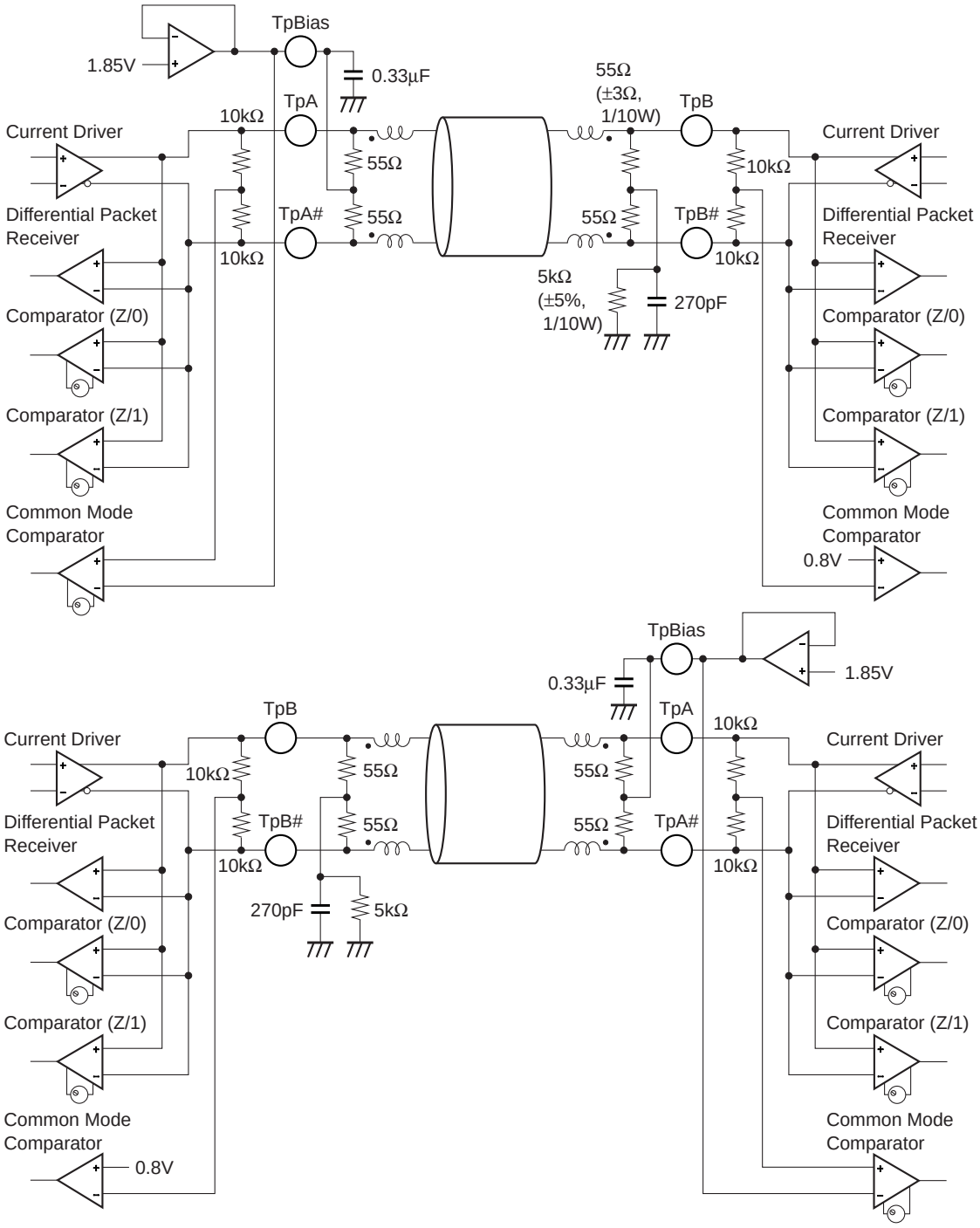


Fig. 3-9. Cable Interface

Dedicated IEEE 1394 cables are used as the cable media, and two sets of shielded twisted pair cables are used for data transmit and receive. As shown in Fig. 3-9, each twisted pair cable connects the TpA pair of this node with the TpB pair of the opposing node.
Both the TpA and TpB sides require two 55Ω (±3Ω, 1/10W) terminating resistors in accordance with the cable impedance. Locate these terminating resistors as close to the IC pins as possible.
TpBias (typ. 1.85V) is connected to the node between the terminating resistors on the TpA side in order to set the cable in-phase DC potential. Connect 0.33µF to TpBias for decoupling. The in-phase current for the speed signal described hereafter is supplied from this capacitor. Note that this capacitor is used to compensate the phase of the internal operational amplifier, so it is necessary even when not actually using TpBias (unused port, etc.).
Connect 5kΩ (±5%, 1/10W) and 270pF (10V) to the node between the terminating resistors on the TpB side to pull it down. As a result, when the cable is disconnected and the DC bias from the opposing node TpA is cut off, the TpB side DC potential drops to near 0V and this can be detected by an in-phase comparator. The 270pF is for decoupling.
Fig. 3-9 shows the case in which the coil located between the terminating resistor and the cable is a common mode coil (250nH, K > 0.97) for limiting the in-phase signal bandwidth. When using a coil, connect it in this position to reduce electromagnetic interference (EMI) due to in-phase noise generated at the signal transition point. This has no effect on data transmit or receive, so there are no problems with communication even if a coil is not used.

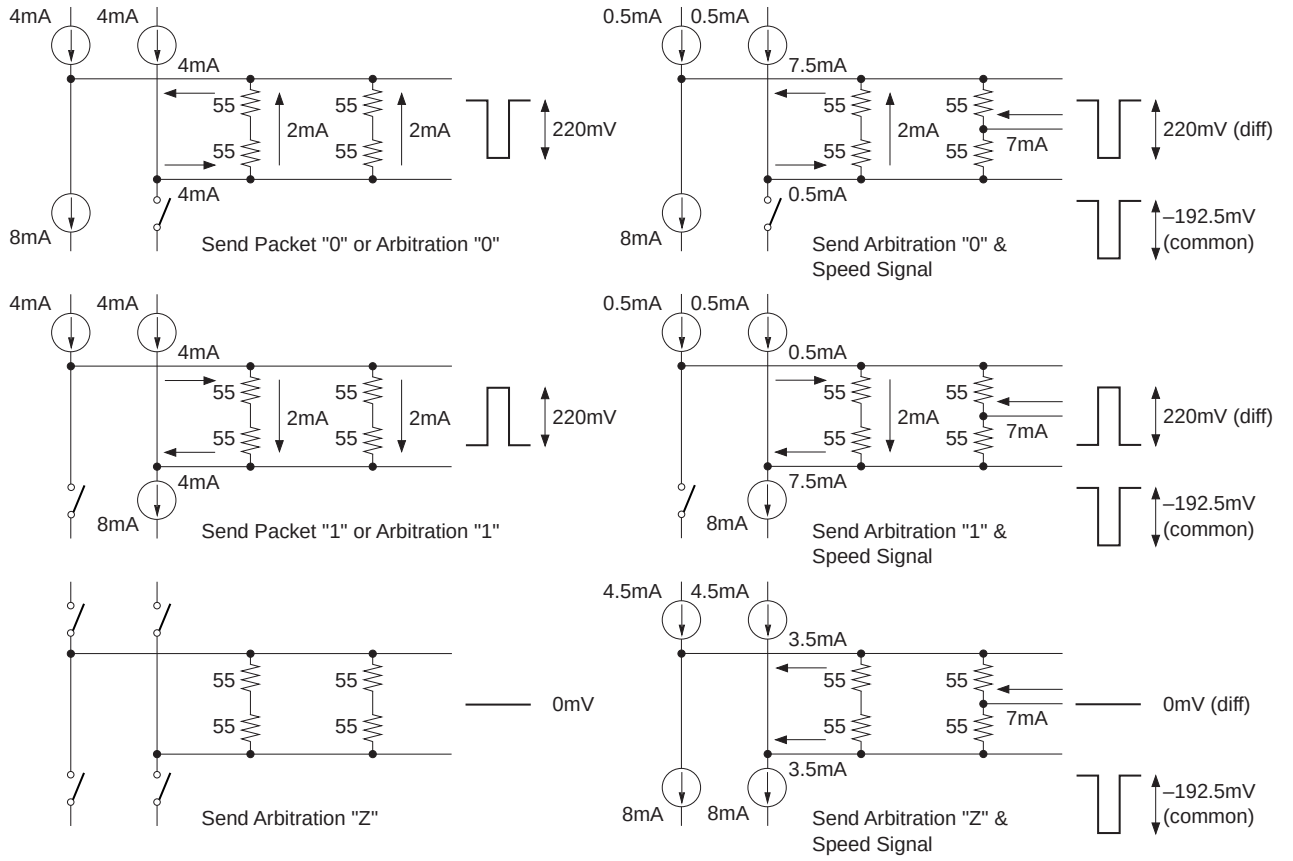
3-2-2. Description of Cable Interface Operation

The communication phases with the opposing node can be broadly divided into "arbitration" and "data packet transmit/receive". Arbitration transmit/receive is ternary logic (0, 1, Z; differential) and is performed by full-duplex communication with the speed signal (in-phase) superimposed. Packet transmit/receive is binary logic (0, 1; differential) and is performed by semi-duplex communication. In either case, transmit is performed by the high impedance current driver, and receive by detecting the differential or in-phase voltage at both ends of the terminating resistors with a comparator or a packet receiver.
The signals transmitted and received by TpA and TpB are as follows.

TpA:
- Differential signal: Arbitration transmit/receive, packet transmit (Strobe signal), packet receive (Data signal)
- In-phase signal: Speed signal receive, cable bias (TpBias)

TpB:
- Differential signal: Arbitration transmit/receive, packet transmit (Data signal), packet receive (Strobe signal)
- In-phase signal: Speed signal transmit, connection status detection

Fig. 3-10 shows the current driver status, cable current, and the differential and in-phase voltage waveforms observed at the terminating resistors during various data transmit. (Fig. 3-10 illustrates various signal states, and does not indicate the waveform for a particular bus phase.)



"Z"	"0" Arbitration			"1" Arbitration			"Z" Arbitration		
	Spd Sig "OFF"	Spd Sig "ON"	Spd Sig "OFF"	Spd Sig "OFF"	Spd Sig "ON"	Spd Sig "OFF"	Spd Sig "OFF"	Spd Sig "ON"	Spd Sig "OFF"

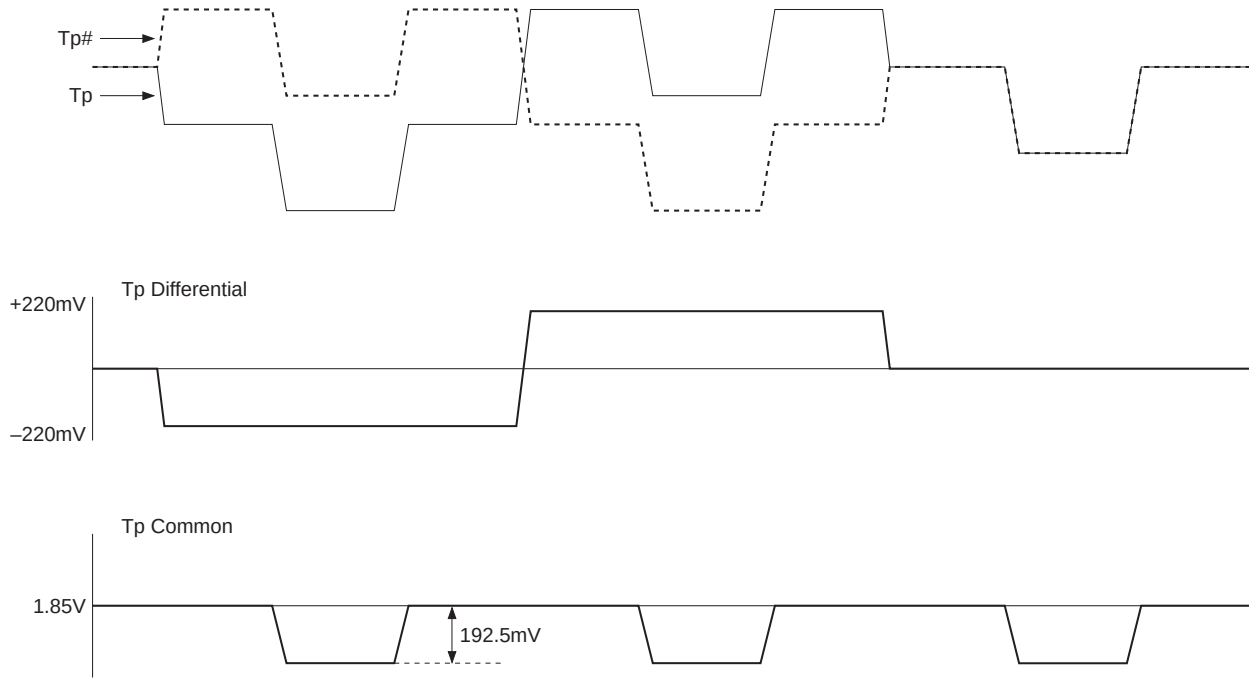


Fig. 3-10. Driver Current and Output Waveforms

3-2-3. CPS (Cable Power Status)

The CPS pin is connected to the cable power (Vp) via an external resistor Rcps (normally 226kΩ), and detects when the cable power drops below the threshold (normally 7.5V). When not used, connect to AV_{DD}.
The relationship between the threshold value Vt and the external resistor Rcps is given by the following formula.

$$Vt = 1.85 + Rcps \times 25E\text{-}6$$

3-2-4. Processing for Unused Ports

The CXD1945R has three ports. When using only one or two of these ports, connect the unused port pins as follows.

Unused port pin symbol	Connection
TpAp, TpAn	No connected
TpBp, TpBn	AV_{SS}
TpBias	To AV_{SS} via 0.33µF

Table 3-11. Processing for Unused Port Pins

The circuit diagram when using only one port is shown below as an example.

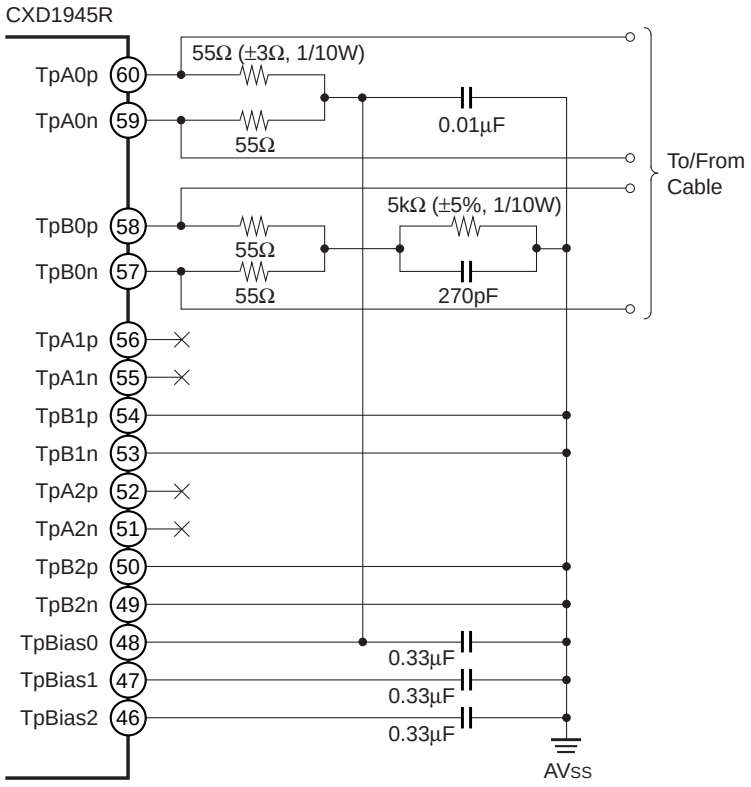


Fig. 3-11. Circuit Diagram when Using Only One Port

3-3. Clock Circuit

3-3-1. Crystal Oscillator

An oscillator output frequency of 24.576MHz ±100ppm is necessary. The crystal itself should have an accuracy of ±50ppm when load capacitance of 10pF is connected.

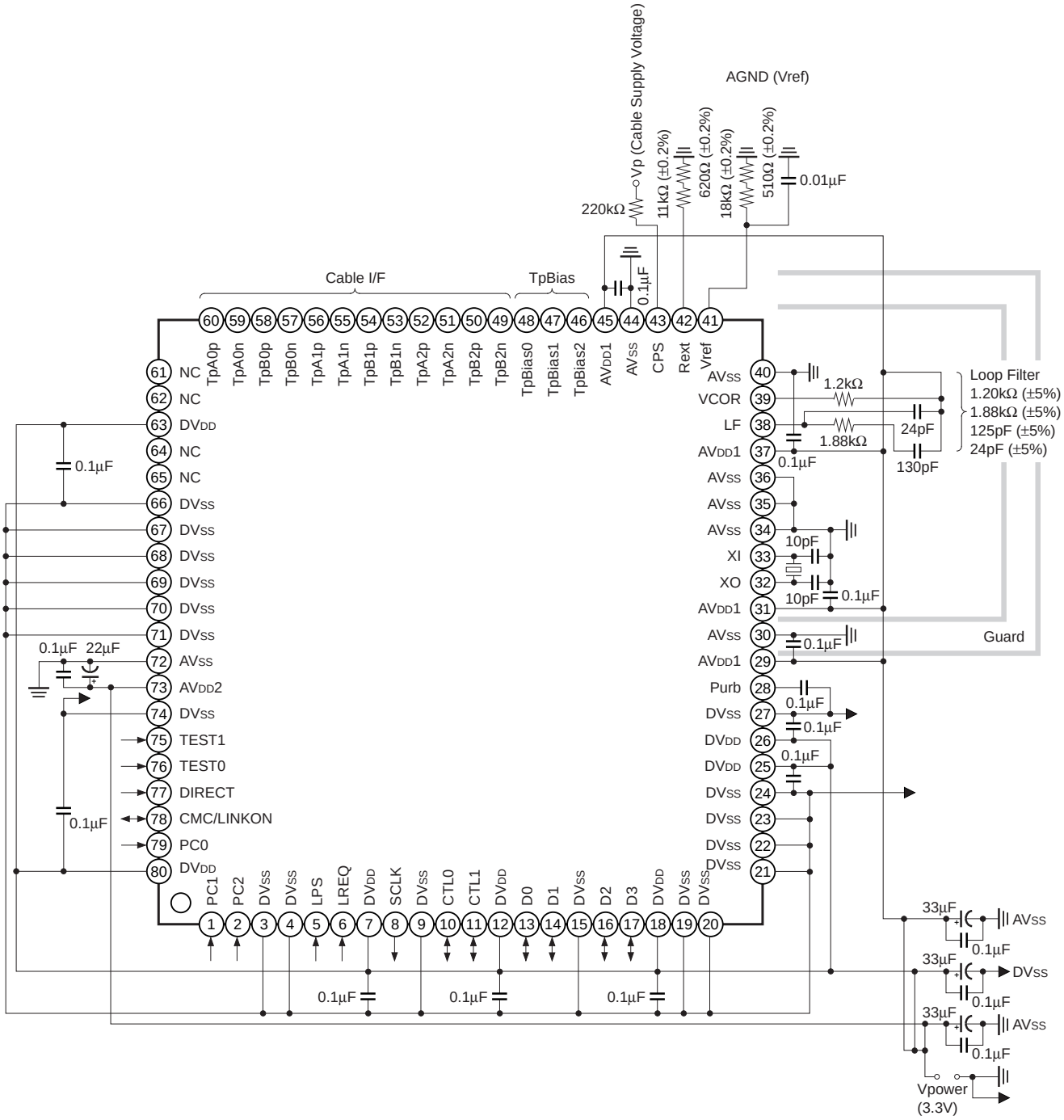
3-3-2. PLL

The PLL multiplies the 24.576MHz output from the crystal oscillator by 8 times to generate 196.608MHz.
PLL lock time is 100µs or less.

3-4. Hardware Reset

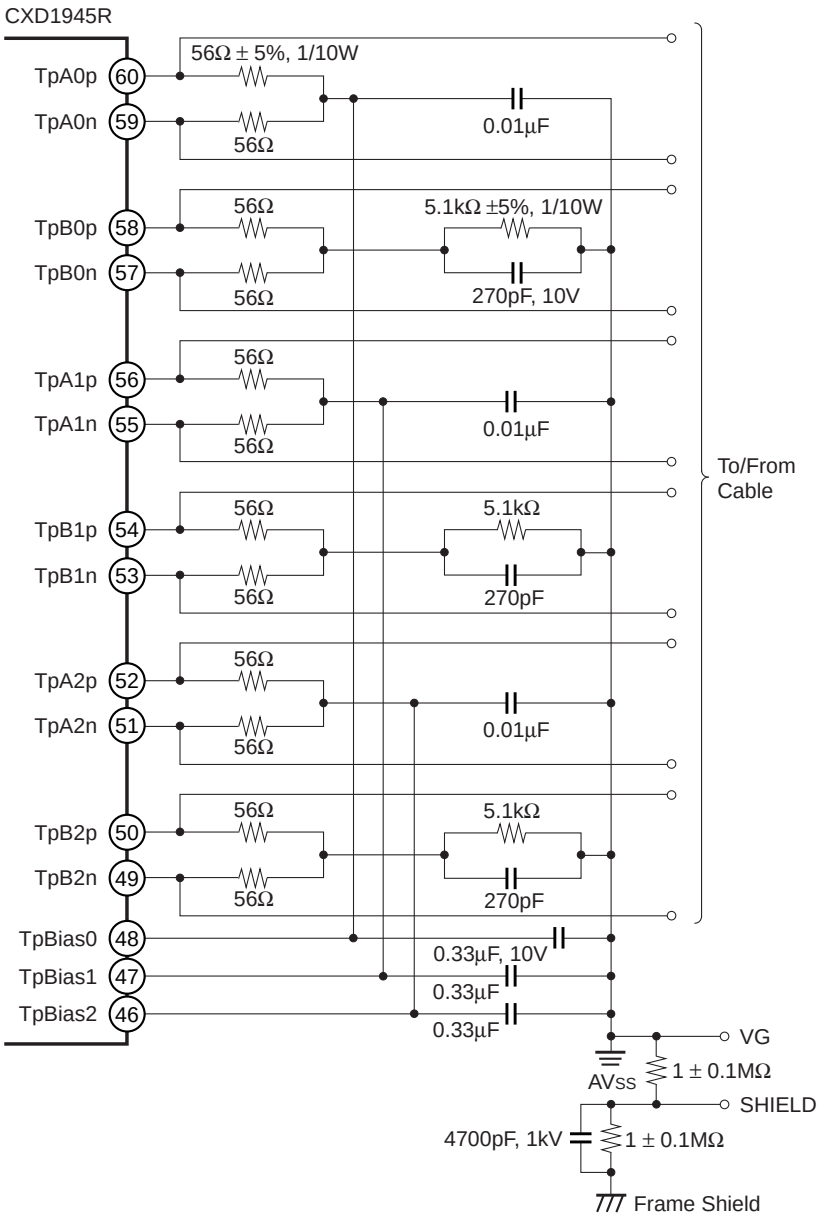
A reset pulse with a minimum width of 15ms is generated during power-on by connecting the Purb pin to ground via a 0.1µF external capacitor. All state machines are reset by externally applying low level to this pin.

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Cable Interface Connection Circuit Example

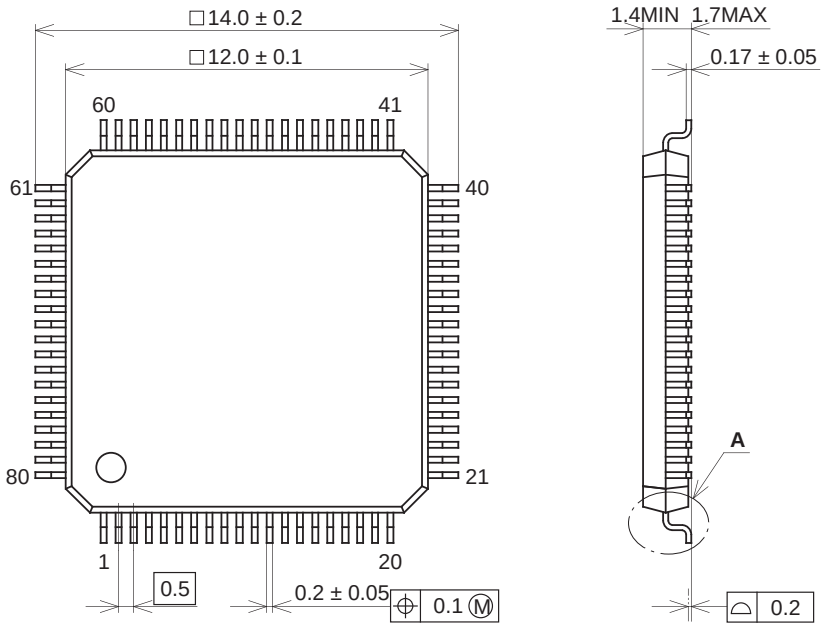


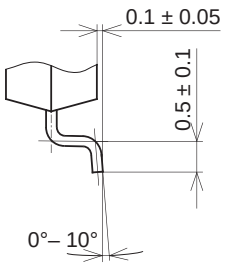
• Reduce the parasitic impedance of the cable interfaces (TpA, TpB) as much as possible.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN LQFP(PLASTIC)





DETAIL **A**

SONY CODE	LQFP-80P-L231
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.5 g