37V/1.2A Step-Down Regulator in 3mm × 3mm DFN and MSE

FEATURES

- **Wide Input Range:**
  Operation from 3.6V to 37V
  Overvoltage Lockout Protects Circuit Through 60V Transients
- **Low Minimum On-Time:**
  Converts 16V_{IN} to 3.3V_{OUT} at 2MHz
- **1.2A Output Current**
- **Adjustable Frequency: 300kHz to 2.5MHz**
- **Constant Switching Frequency at Light Loads**
- **Can Be Synchronized to External Clock**
- Tracking and Soft-Start
- Precision UVLO
- Short-Circuit Robust
- I_Q in Shutdown <1µA
- Internally Compensated
- Thermally Enhanced MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- Automotive Systems
- Battery-Powered Equipment
- Wall Transformer Regulation
- Distributed Supply Regulation

DESCRIPTION

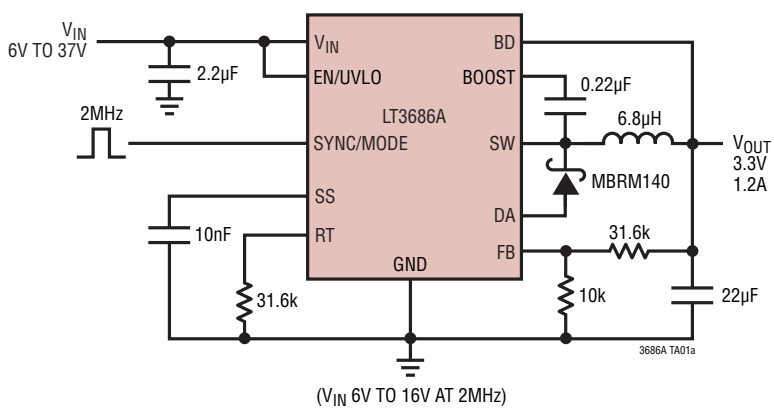
The LT®3686A is a current mode PWM step-down DC/DC converter with an internal power switch. The wide input range of 3.6V to 37V makes the LT3686A suitable for regulating power from a wide variety of sources, including 24V industrial supplies and automotive batteries. Its high maximum frequency allows the use of tiny inductors and capacitors, resulting in a very small solution. Operating frequency above the AM band avoids interfering with radio reception, making the LT3686A particularly suitable for automotive applications.

Cycle-by-cycle current limit, thermal shutdown and DA current sense provide protection against fault conditions. Soft-start and frequency foldback eliminate input current surge during start-up. An optional internal regulated active load at the output via the BD pin keeps the LT3686A at full switching frequency at light loads, resulting in low, predictable output ripple above the audio and AM bands. Internal compensation and an internal boost diode reduce external component count.

The LT3686A offers external synchronization capability, whereas the LT3686 does not.

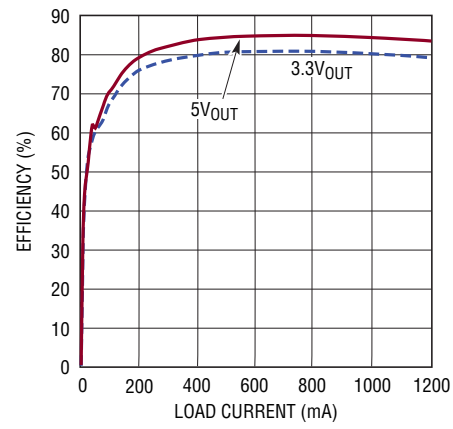
TYPICAL APPLICATION

3.3V Step-Down Converter



(V_{IN} 6V TO 16V AT 2MHz)

12V_{IN} Efficiency (2MHz)

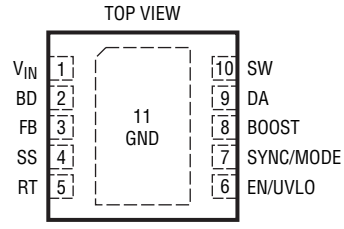


ABSOLUTE MAXIMUM RATINGS

(Note 1)

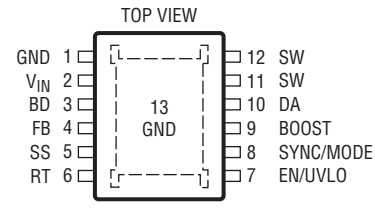
Input Voltage (V_{IN}) (Note 7) 60V
BOOST Voltage 55V
BOOST Pin Above SW Pin 25V
FB Voltage 6V
EN/UVLO Voltage (Note 7) 60V
BD Voltage 25V
RT Voltage 6V
SS Voltage 2.5V
SYNC/MODE Voltage 6V
Operating Junction Temperature Range (Note 2)
LT3686AE ..... –40°C to 125°C
LT3686AI ..... –40°C to 125°C
LT3686AH ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (MSE Package Only, Soldering, 10 Sec) ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3686AEDD#PBF	LT3686AEDD#TRPBF	LFRK	10-Lead Plastic DFN	–40°C to 125°C
LT3686AIDD#PBF	LT3686AIDD#TRPBF	LFRK	10-Lead Plastic DFN	–40°C to 125°C
LT3686AEMSE#PBF	LT3686AEMSE#TRPBF	3686A	12-Lead Plastic MSOP	–40°C to 125°C
LT3686AIMSE#PBF	LT3686AIMSE#TRPBF	3686A	12-Lead Plastic MSOP	–40°C to 125°C
LT3686AHMSE#PBF	LT3686AHMSE#TRPBF	3686A	12-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

*For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{EN/UVLO}$ ≥ 1.34V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current at Shutdown	$V_{EN/UVLO}$ < 0.4V $V_{EN/UVLO}$ = 1V			0.1 10	1 15	µA µA
Quiescent Current	Not Switching, SYNC/MODE ≤ 0.4V Not Switching, SYNC/MODE ≥ 0.8V			1.1 1.2	1.3 1.4	mA mA
Internal Undervoltage Lockout				3.4	3.6	V
Overvoltage Lockout		●	37	38	39	V
Feedback Voltage	V_{IN} = 3.6V ↔ 37V	 ●	0.790 0.785	0.8 0.8	0.810 0.815	V V
FB Pin Bias Current				60	100	nA
Switching Frequency	I_{DA} < 1.2A R_T = 15.4kΩ, IDA < 1.2A		0.3 1.9	 2.1	2.5 2.3	MHz MHz
Minimum On Time	SYNC/MODE > 0.8V, BD < 6V			100	110	ns
Minimum Off Time				150	200	ns
Switch V_{CESAT}	I_{SW} = 1.2A			680		mV
Switch Current Limit	(Note 3)	 ●	1.9 1.85	2.3 2.3	2.6 2.65	A A
Switch Active Current	SW = 10V (Note 4) SW = 0V (Note 5)			400 20	600 30	µA µA
BOOST Pin Current	I_{SW} = 1.2A			20		mA
Minimum Boost Voltage Above Switch	I_{SW} = 1.2A			2.2	2.4	V
Max BD Pin Active Load Current	SYNC/MODE > 0.8V, BD < 6V		30	40		mA
BD Pin Voltage to Disable Active Load		●	6	6.5	7	V
DA Pin Current to Stop OSC		●	1.2	1.7		A
SYNC/MODE High		●	0.8			V
SYNC/MODE Low		●			0.4	V
SYNC/MODE Bias Current					0.2	µA
SS Threshold				0.9		V
SS Source Current	V_{SS} = 1V		1.3	2	2.7	µA
EN/UVLO Bias Current	$V_{EN/UVLO}$ = 10V $V_{EN/UVLO}$ = 0V				40 1	µA µA
EN/UVLO Threshold to Turn Off		●	1.22	1.28	1.34	V
EN/UVLO Hysteresis Current			1.8	2.4	3	µA
Boost Diode Forward Drop	I_{BD} to I_{BOOST} = 200mA			0.85		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3686AE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3686AI is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3686AH is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. (Note 6)

Note 3: Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycle.

Note 4: Current flows into pin.

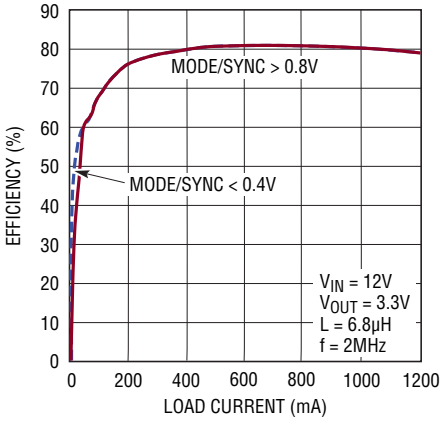
Note 5: Current flows out of pin.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability. See High Temperature Considerations section. Also see Operation section.

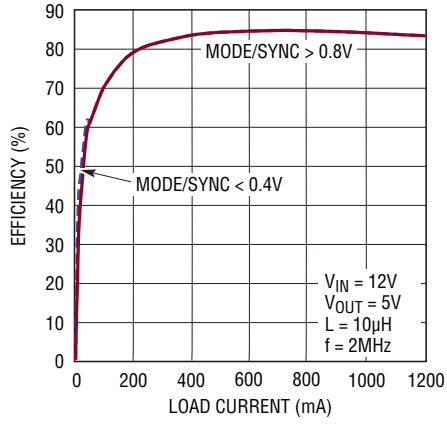
Note 7: Absolute Maximum Voltage at V_{IN} and EN/UVLO pins is 60V for nonrepetitive one second transients, and 55V for continuous operation.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

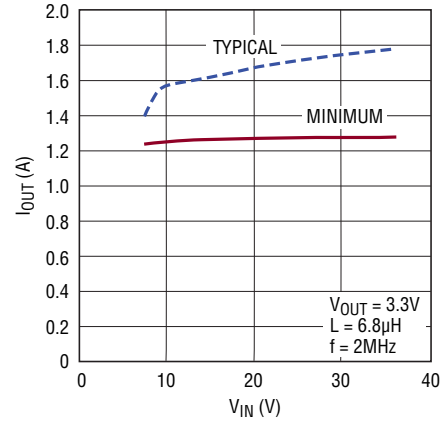
3.3V_{OUT} Efficiency (2MHz)



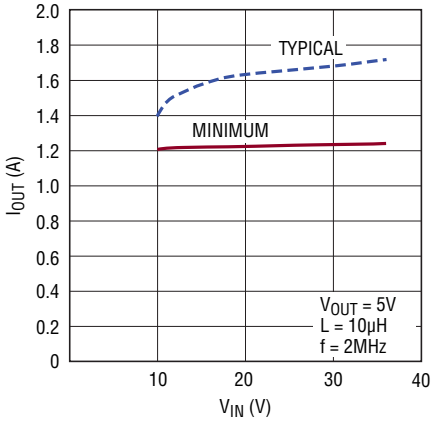
5V_{OUT} Efficiency



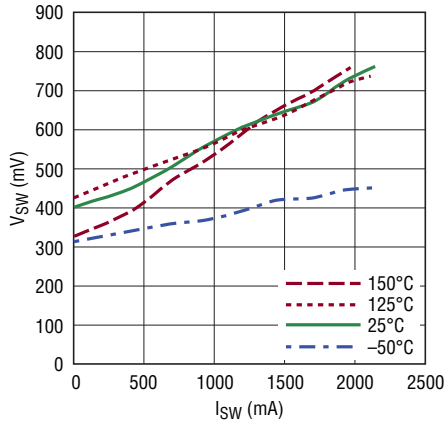
3.3V_{OUT} Maximum Load Current



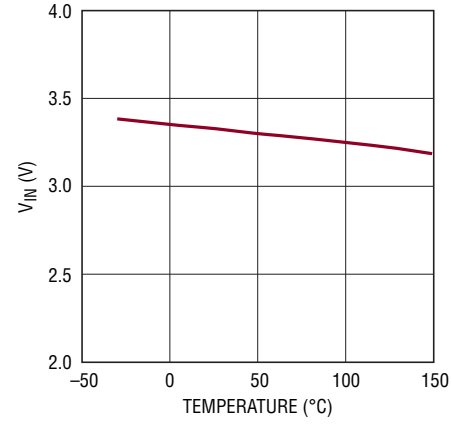
5V_{OUT} Maximum Load Current



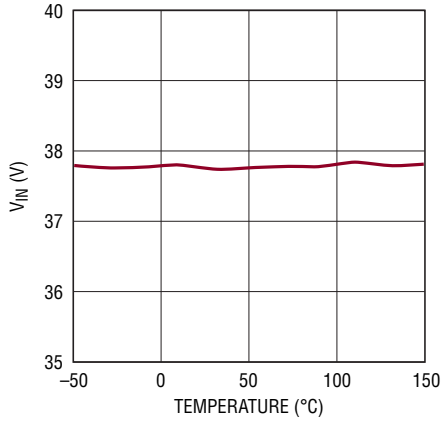
Switch Voltage Drop



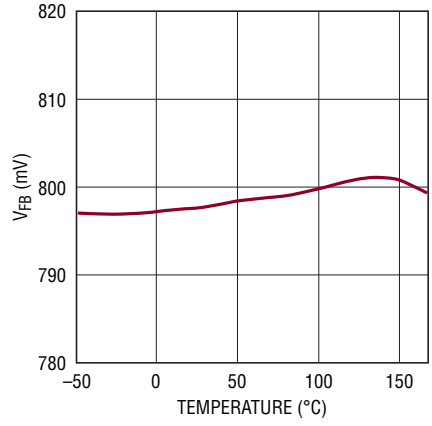
Internal Undervoltage Lockout (UVLO)



Overvoltage Lockout (OVLO)

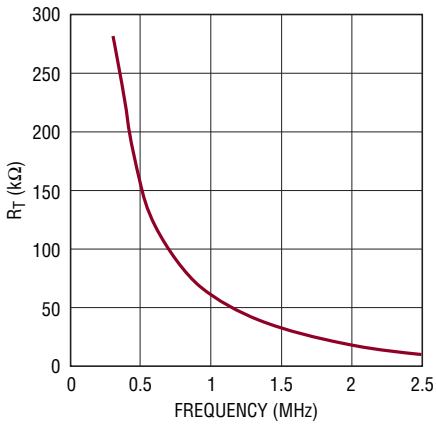


V_{FB} vs Temperature



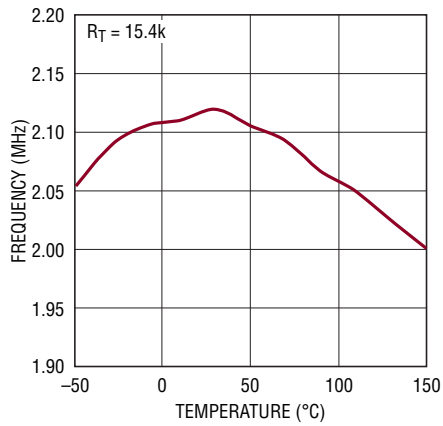
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Switching Frequency vs R_T



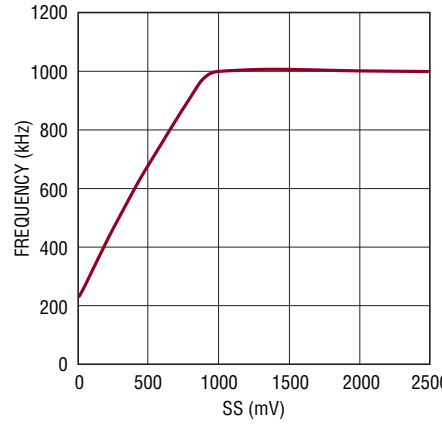
3686A G09

Switching Frequency vs Temperature



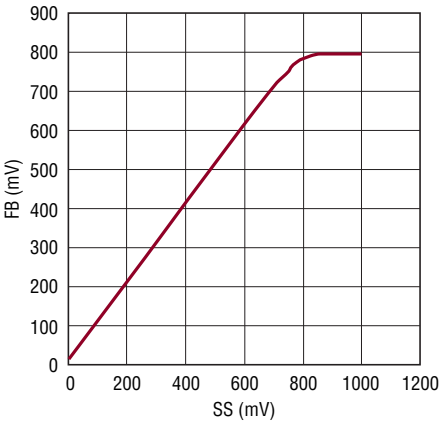
3686A G10

Soft-Start/Track vs Frequency (1MHz)



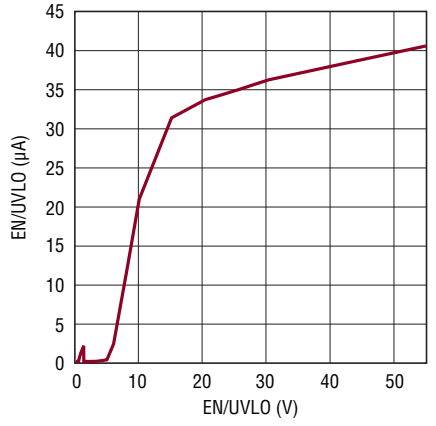
3686A G11

Soft-Start/Track vs V_{FB}



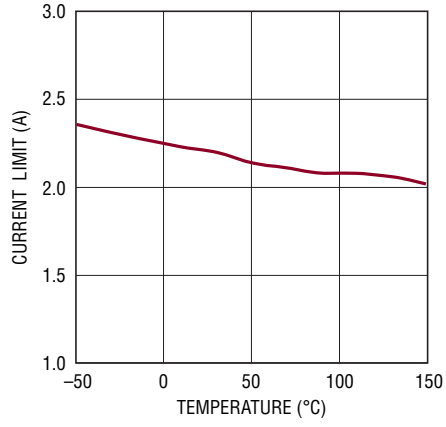
3686A G12

EN/UVLO Pin Current



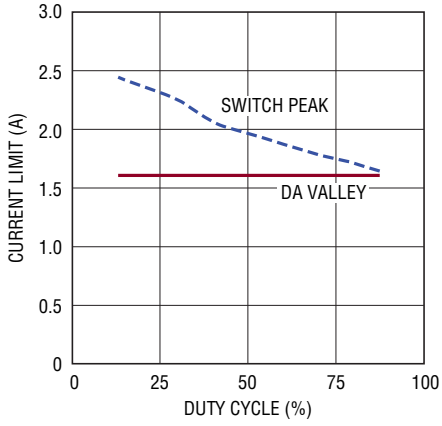
3686A G13

Switch Current Limit vs Temperature



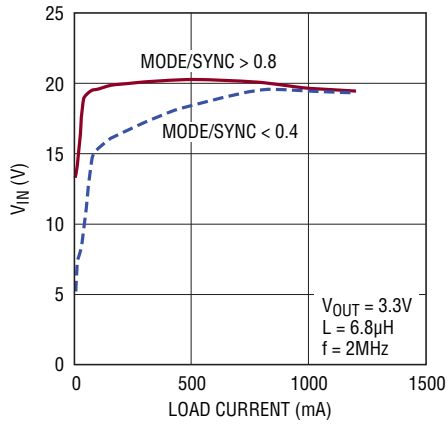
3686A G14

Current Limit vs Duty Cycle



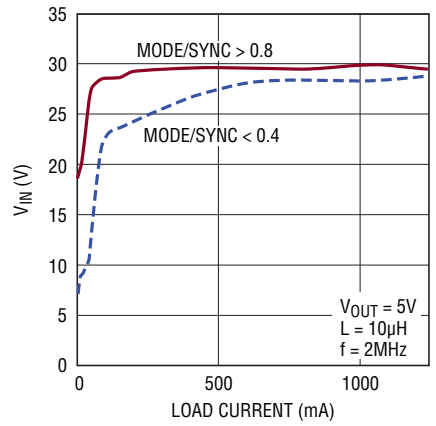
3686A G15

3.3V_{OUT} Maximum V_{IN} for Full Frequency (2MHz)



3686A G16

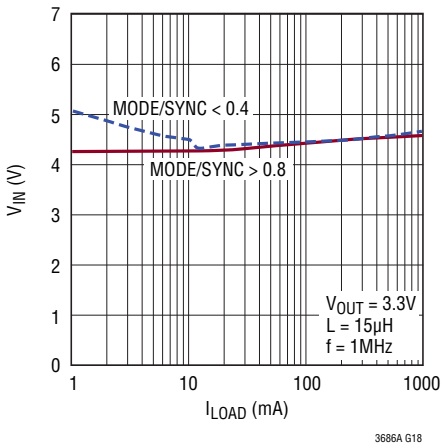
5V_{OUT} Maximum V_{IN} for Full Frequency (2MHz)



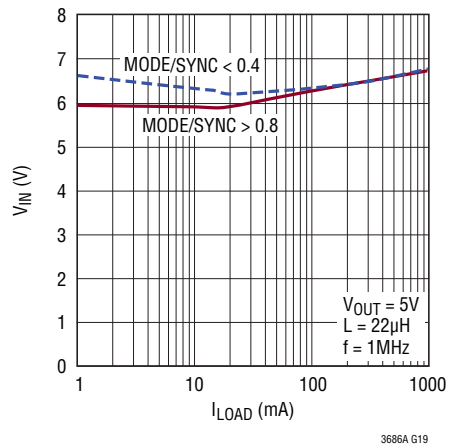
3686A G17

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

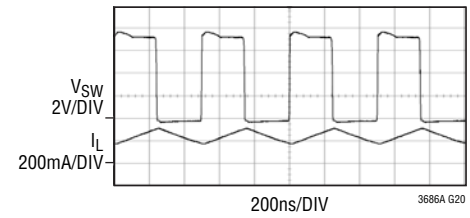
3.3V_{OUT} Typical Minimum Input Voltage



5V_{OUT} Typical Minimum Input Voltage

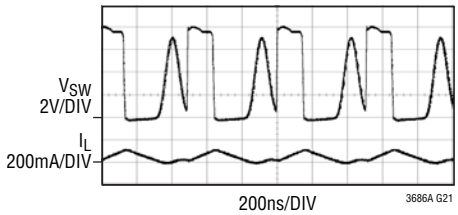


Continuous Mode Waveform



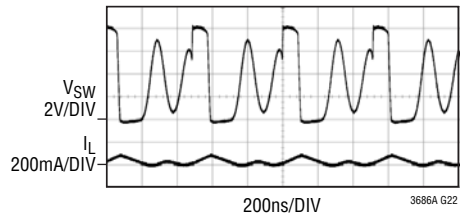
V_{IN} = 10V
V_{OUT} = 3.3V
L = 6.8µH
f = 2MHz
C_{OUT} = 22µF
I_{LOAD} = 200mA
MODE/SYNC = 0V

Light Load Discontinuous Mode Waveform



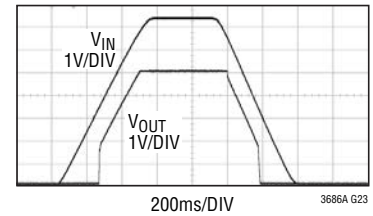
V_{IN} = 10V
V_{OUT} = 3.3V
L = 6.8µH
f = 2MHz
C_{OUT} = 22µF
I_{LOAD} = 25mA
MODE/SYNC = 0V

Fixed Frequency No Load Waveform



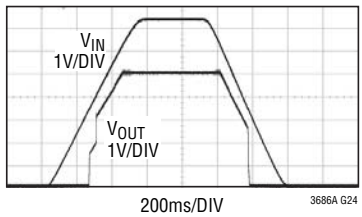
V_{IN} = 10V
V_{OUT} = 3.3V
L = 6.8µH
f = 2MHz
C_{OUT} = 22µF
I_{LOAD} = 0mA
MODE/SYNC = 3.3V

Start-Up Shutdown Waveform I_{LOAD} = 5mA



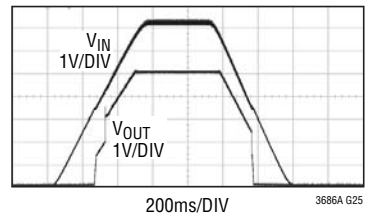
V_{OUT} = 5V
L = 22µH
f = 1MHz
I_{LOAD} = 5mA
MODE/SYNC = 0V

Start-Up Shutdown Waveform I_{LOAD} = 5mA



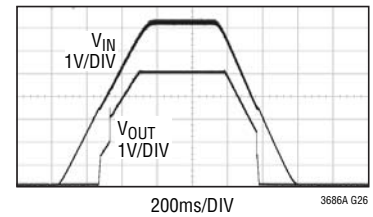
V_{OUT} = 5V
L = 22µH
f = 1MHz
I_{LOAD} = 5mA
MODE/SYNC = 1V

Start-Up Shutdown Waveform I_{LOAD} = 500mA



V_{OUT} = 5V
L = 22µH
f = 1MHz
I_{LOAD} = 500mA
MODE/SYNC = 0V

Start-Up Shutdown Waveform I_{LOAD} = 500mA



V_{OUT} = 5V
L = 22µH
f = 1MHz
I_{LOAD} = 500mA
MODE/SYNC = 1V

PIN FUNCTIONS (DFN/MSE)

V_{IN} (Pin 1/2): The V_{IN} pin supplies current to the LT3686A's internal regulator and to the internal power switch. This pin must be locally bypassed.

BD (Pin 2/3): When the SYNC/MODE Pin is driven with clock pulses or tied greater than 0.8V, the LT3686A will prevent pulse-skipping at light loads by regulating an active load on the BD pin; see Applications Information section Fixed Frequency at Light Load.

FB (Pin 3/4): The LT3686A regulates its feedback pin to 0.8V. Connect the feedback resistor divider tap to this pin. Set the output voltage according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

A good value for R2 is 10k.

SS (Pin 4/5): Provides Soft-Start and Tracking. An internal 2µA current source tied to a 2.5V reference supplies current to this pin to charge an external capacitor to create a voltage ramp at the pin. Feedback voltage and switching frequency both track SS voltage. Feedback voltage stops tracking at 0.8V. SS is reset under UVLO, OVLO and thermal shutdown conditions. Float the pin if soft-start feature is not being used.

RT (Pin 5/6): The RT pin is used to program the oscillator frequency. Select the value of R_T resistor according to table 1 in the applications section of the data sheet.

EN/UVLO (Pin 6/7): The EN/UVLO pin is used to start up the LT3686A. Pull the pin below 0.4V to shutdown the LT3686A. The 1.28V threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached the programmed level. Do not drive the EN/UVLO pin above V_{IN}.

SYNC/MODE (Pin 7/8): The SYNC/MODE pin is used to synchronize the internal oscillator of the LT3686A to an external signal. The SYNC signal can be driven by a signal with pulse width of at least 200ns on and off time. The SYNC/MODE Pin also acts as mode select for the BD active load; when it is driven with pulses or tied above 0.8V, the LT3686A will prevent pulse skipping at light loads by regulating an active load on the BD pin. To disable the active load, tie SYNC/MODE to below 0.4V.

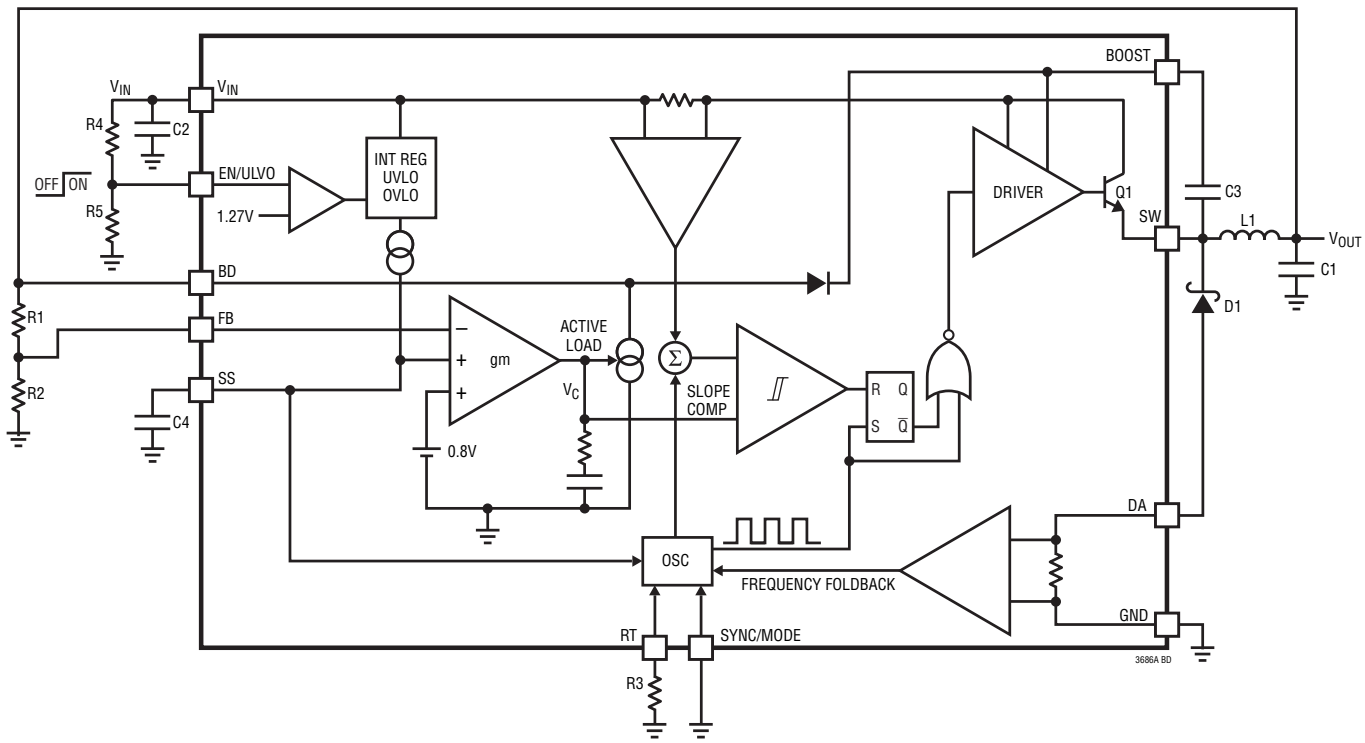
BOOST (Pin 8/9): The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch.

DA (Pin 9/10): Connect catch diode (D1) anode to this pin.

SW (Pin 10/11, 12): The SW pin is the output of the internal power switch. Connect this pin to the inductor, catch diode and boost capacitor.

GND (Exposed Pad Pin 11/Pin 1, Exposed Pad Pin 13): The exposed pad GND pin is the only ground connection for the device. The exposed pad should be soldered to a large copper area to reduce thermal resistance.

BLOCK DIAGRAM



OPERATION

The LT3686A is a current mode step-down regulator. The EN/UVLO pin is used to place the LT3686A in shutdown. The 1.28V threshold on the EN/UVLO pin can be programmed by an external resistor divider (R4, R5) to disable the LT3686A. When the EN/UVLO pin is driven above 1.28V, an internal regulator provides power to the control circuitry. This regulator includes both overvoltage and undervoltage lockout to prevent switching when V_{IN} is more than 37V or less than 3.6V.

Tracking soft-start is implemented by providing constant current via the SS pin to an external soft-start capacitor (C4) to generate a voltage ramp. FB voltage is regulated to the voltage at the SS pin until it exceeds 0.8V; FB is then regulated to the reference 0.8V. Soft-start also reduces the oscillator frequency to avoid hitting current limit during start-up. The SS capacitor is reset during fault events such as overvoltage, undervoltage, thermal shutdown and startup.

An oscillator is programmed by resistor R_T. The oscillator sets an RS flip-flop, turning on the internal 1.2A power switch Q1. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the V_C node. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp (not shown) on the V_C node provides current limit.

The switch driver operates from either V_{IN} or from the BOOST pin. An external capacitor and the internal boost diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

A comparator monitors the current flowing through the catch diode via the DA pin and reduces the LT3686A's operating frequency when the DA pin current exceeds the 1.7A valley current limit. This helps to control the output current in fault conditions such as shorted output with high input voltage. The DA comparator works in conjunction with the switch peak current limit comparator to determine the maximum deliverable current of the LT3686A.

The SYNC/MODE pin doubles as mode select for the BD active load circuit. The active load is enabled when SYNC/MODE is driven with sync pulses or tied above 0.8V and disabled when SYNC/MODE is tied below 0.4V. The LT3686A will prevent pulse skipping at light loads by regulating the active load. The active load will assist startup by guaranteeing a minimum load to charge the boost capacitor. It also hastens the recharge of boost capacitor when operating beyond maximum duty cycle.

The active load works only when the BD pin is less than 6V.

APPLICATIONS INFORMATION

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the 1% resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

R2 should be 20k or less to avoid bias current errors. Reference designators refer to the Block Diagram.

Programmable Undervoltage Lockout

The EN/UVLO pin can be programmed by an external resistor divider between V_{IN} and the EN/UVLO pin. Choose the resistors according to:

$$R4 = R5\left(\frac{V_{IN}}{1.28V} - 1\right)$$

R4 also sets the hysteresis voltage for the programmable UVLO:

$$\text{Hysteresis} = R4 \bullet 2.4\mu A$$

Once V_{IN} drops below the programmed voltage, the LT3686A will enter a low quiescent current state (Iq ≈ 15µA). To shutdown the LT3686A completely (Iq < 1µA), reduce EN/UVLO pin voltage to below 0.4V.

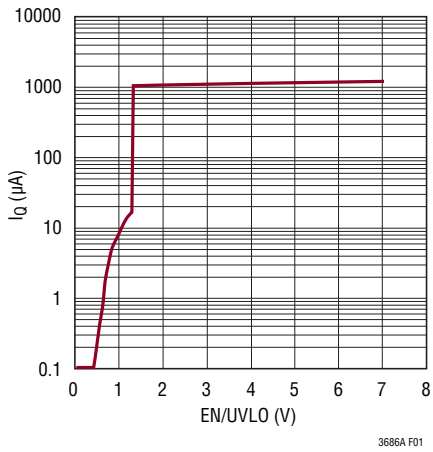


Figure 1. I_Q vs $V_{EN/UVLO}$ (V_{IN} = 10V)

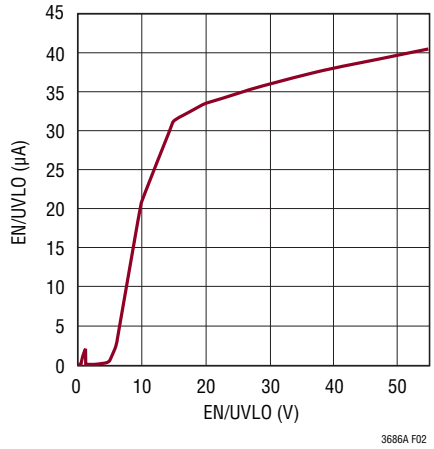


Figure 2. EN/UVLO Pin Current

Input Voltage Range

The input voltage range for the LT3686A applications depends on the output voltage and on the absolute maximum ratings of the V_{IN} and BOOST pins. The minimum input voltage is determined by either the LT3686A's minimum operating voltage of 3.6V, or by its maximum duty cycle.

The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = \frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}$$

Where V_D is the forward voltage drop of the catch diode (~0.4V) and V_{SW} is the voltage drop of the internal switch (~0.67V at maximum load). This leads to a minimum input voltage of:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_D}{DC_{MAX}} - V_D + V_{SW}$$

DC_{MAX} can be adjusted with frequency.

The boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to sustain the charge across the boost capacitor.

APPLICATIONS INFORMATION

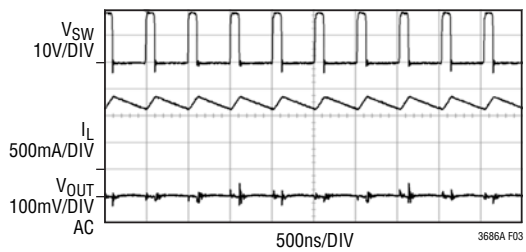
The maximum input voltage is determined by the absolute maximum ratings of the V_{IN} and BOOST pins. For fixed frequency operation, the maximum input voltage is determined by the minimum duty cycle DC_{MIN}:

$$V_{IN(MAX)} = \frac{V_{OUT} + V_D}{DC_{MIN}} - V_D + V_{SW}$$

DC_{MIN} can be adjusted with frequency. Note that this is a restriction on the operating input voltage for fixed frequency operation; the circuit will tolerate transient inputs up to the absolute maximum ratings of the V_{IN} and BOOST pins.

Minimum On Time

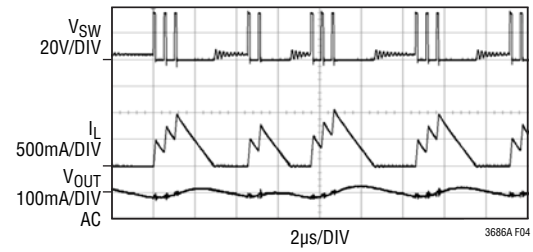
As the input voltage is increased, the LT3686A is required to switch for shorter periods of time. Delays associated with turning off the power switch dictate the minimum on time of the part. The minimum on time for the LT3686A is 100ns (Figure 3).



V_{IN} = 18V
V_{OUT} = 3.3V
L = 6.8µH
C_{OUT} = 22µF
I_{LOAD} = 1.2mA

Figure 3. Continuous Mode Operation Near Minimum On Time

When the required on time decreases below the typical minimum on time of 100ns, instead of the switch pulse width becoming narrower to accommodate the lower duty cycle requirement, the switch pulse width remains fixed at 100ns. The inductor current ramps up to a value exceeding the load current and the output ripple increases. The part then remains off until the output voltage dips below the programmed value before it begins switching again (Figure 4).



V_{IN} = 35V
V_{OUT} = 3.3V
L = 6.8µH
C_{OUT} = 22µF
I_{OUT} = 300mA

Figure 4. Pulse Skip Occurs When Required On Time Is Below 100ns

Provided that the load can tolerate the increased output voltage ripple and that the components have been properly selected, operation while pulse skipping is safe and will not damage the part. As the input voltage increases, the inductor current ramps up quicker, the number of skipped pulses increases, and the output voltage ripple increases.

Inductor current may reach current limit when operating in pulse skip mode with small valued inductors. In this case, the LT3686A will periodically reduce its frequency

APPLICATIONS INFORMATION

to keep the inductor valley current to 1.7A (Figure 5). Peak inductor current is therefore peak current plus minimum switch delay:

$1.7A + (V_{IN} – V_{OUT})/L \bullet 100ns$

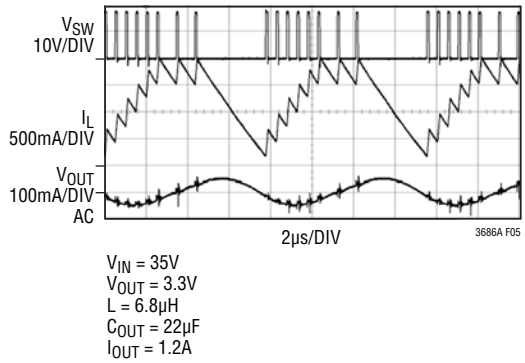


Figure 5. Pulse Skip with Large Load Current Will Be Limited by the DA Valley Current Limit. Notice the Flat Inductor Valley Current and Reduced Switching Frequency

The part is robust enough to survive prolonged operation under these conditions as long as the peak inductor current does not exceed 2A. Inductor current saturation and junction temperature may further limit performance during this operating regime.

Frequency Selection

The maximum frequency that the LT3686A can be programmed to is 2.5MHz. The minimum frequency that the LT3686A can be programmed to is 300kHz. The switching frequency is programmed by tying a 1% resistor from the RT pin to ground. Table 1 can be used to select the value of R_T. Minimum on-time and edge loss must be taken into consideration when selecting the intended frequency of operation. Higher switching frequency increases power dissipation and lowers efficiency. Finite transistor bandwidth limits the speed at which the power switch can be turned on and off, effectively setting the minimum on-time of the LT3686A. For a given output voltage, the minimum on-time determines the maximum input voltage to remain in continuous mode operation outlined in the Minimum On Time section of the data sheet. Finite transition time results in a small amount of power dissipation each time the power switch turns on and off (edge loss). Edge loss increases with frequency, switch current, and input voltage.

Table 1. R_T vs Frequency

FREQUENCY (MHz)	R_T (kΩ)	MIN SYNC FREQUENCY (MHz)
2.5	9.53	N/A
2.3	12.1	N/A
2.1	15.4	N/A
1.9	20.0	N/A
1.8	22.6	2.50
1.7	25.5	2.30
1.5	31.6	1.99
1.3	40.2	1.70
1.1	52.3	1.42
0.9	69.8	1.14
0.7	97.6	0.874
0.5	150	0.615
0.3	280	0.363

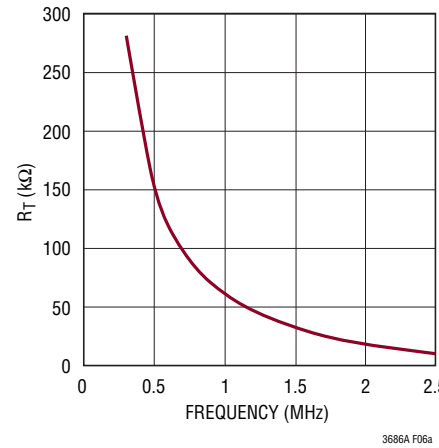


Figure 6a. Switching Frequency vs R_T

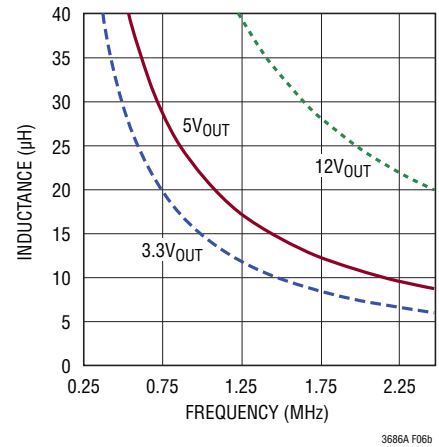


Figure 6b. Suggested Inductance vs Frequency

APPLICATIONS INFORMATION

The SYNC/MODE pin is used to synchronize the internal oscillator with an external square wave. The synchronizing clock signal to the LT3686A should be below 2.5MHz with pulse width of at least 200ns on and off time, a low state below 0.4V and a high state above 0.8V. The SYNC frequency must be higher than the RT programmed frequency; see Table 1.

The inductor value should be chosen based on the RT frequency rather than the highest synchronization frequency.

The SYNC/MODE pin doubles as mode select for the BD active load circuit. The active load is enabled when SYNC/MODE is driven with clock pulses or tied greater than 0.8V and disabled when SYNC/MODE is tied below 0.4V. See Fixed Frequency at Light Load section.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = \frac{4(V_{OUT} + V_D)}{f}$$

where V_D is the voltage drop of the catch diode (~0.4V), L is in µH, frequency is in MHz. With this value there will be no subharmonic oscillation. The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation during fault conditions, the saturation current should be above 2A. To keep efficiency high, the series resistance (DCR) should be less than 0.1Ω. Table 2 lists several vendors and types that are suitable. For small size, the inductor can be chosen according to:

$$L = \frac{2(V_{OUT} + V_D)}{f}$$

Using a smaller value inductor will increase inductor current ripple and reduce the V_{IN} voltage at which the active load can keep the LT3686A at full switching frequency.

There are several graphs in the Typical Performance Characteristics section of this data sheet that show the maximum load current as a function of input voltage and inductor value for several popular output voltages. Low inductance may result in discontinuous mode operation, which is okay, but further reduces maximum load current. For details of the maximum output current and discontinuous mode operation, see Linear Technology Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), there is a minimum inductance required to avoid subharmonic oscillations. See Linear Technology Application Note 19.

Catch Diode

A low capacitance 1-2A Schottky diode is recommended for the catch diode, D1. The diode must have a reverse voltage rating equal to or greater than the maximum input voltage. The MBRM140 is a good choice; it is rated for 1A continuous forward current and a maximum reverse voltage of 40V.

Input Capacitor

Bypass the input of the LT3686A circuit with a 2.2µF or higher value ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage and should not be used. A 2.2µF ceramic is adequate to bypass the LT3686A and will easily handle the ripple current. However, if the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be

Table 2.

VENDOR	URL	PART SERIES	INDUCTANCE RATE(µH)	SIZE (mm)
Sumida	www.sumida.com	CDRH4D28 CDRH5D28 CDRH8D28	1.2 to 4.7 2.5 to 10 2.5 to 33	4.5 x 4.5 5.5 x 5.5 8.3 x 8.3
Toko	www.toko.com	A916CY D585LC	2 to 12 1.1 to 39	6.3 x 6.2 8.1 x 8
Würth Elektronik	www.we-online.com	WE-TPC(M) WE-PD2(M) WE-PD(S)	1 to 10 2.2 to 22 1 to 27	4.8 x 4.8 5.2 x 5.8 7.3 x 7.3

APPLICATIONS INFORMATION

necessary. This can be provided with a low performance electrolytic capacitor. Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3686A and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 2.2µF capacitor is capable of this task, but only if it is placed close to the LT3686A and the catch diode (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3686A. A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT3686A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3686A's voltage rating. This situation is easily avoided; see the Hot Plugging Safely section.

Output Capacitor

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3686A to produce the DC output. In this role it determines the output ripple so low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3686A's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good value is:

$$C_{OUT} = \frac{145}{V_{OUT} \bullet f}$$

where C_{OUT} is in µF and frequency is in MHz. Use an X5R or X7R type and keep in mind that a ceramic capacitor biased with V_{OUT} will have less than its nominal capacitance. This choice will provide low output ripple and good transient response. Transient performance can be improved with a high value capacitor, but a phase lead capacitor across the feedback resistor, R1, may be required to get the full benefit (see the Compensation section).

For small size, the output capacitor can be chosen according to:

$$C_{OUT} = \frac{83}{V_{OUT} \bullet f}$$

where C_{OUT} is in µF and frequency is in MHz. However, using an output capacitor this small results in an increased loop crossover frequency and increased sensitivity to noise, requiring careful PCB design.

High performance electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier and should be 0.1Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance, because the capacitor must be large to achieve low ESR. Table 3 lists several capacitor vendors.

Table 3.

VENDOR	PHONE	URL	PART SERIES	COMMENTS
Panasonic	(714) 373-7366	www.panasonic.com	Ceramic Polymer Tantalum	EEF Series
Kemet	(864) 963-6300	www.kemet.com	Ceramic Tantalum	T494, T495
Sanyo	(408) 794-9714	www.sanyovideo.com	Ceramic Polymer Tantalum	POSCAP
Murata	(404) 436-1300	www.murata.com	Ceramic	
AVX		www.avxcorp.com	Ceramic Tantalum	TPS Series
Taiyo Yuden	(864) 963-6300	www.taiyo-yuden.com	Ceramic	

APPLICATIONS INFORMATION

Figure 7 shows the transient response of the LT3686A with several output capacitor choices. The output is 3.3V. The load current is stepped from 0.25A to 1A and back to 0.25A, and the oscilloscope traces show the output voltage. The upper photo shows the recommended value. The second photo shows the improved response (less voltage drop) resulting from a larger output capacitor and a phase lead capacitor. The last photo shows the response to a high performance electrolytic capacitor. Transient performance is improved due to the large output capacitance.

BOOST and BD Pin Considerations

Capacitor C3 and the internal boost diode are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.22µF capacitor will work well. Figure 8 shows two ways to arrange the boost circuit. The BOOST pin must be at least 2.2V above the SW pin for best efficiency. For outputs of 3V and above, the standard circuit (Figure 8a) is best. For outputs less than 3V and above 2.5V, place a discrete Schottky diode (such as the

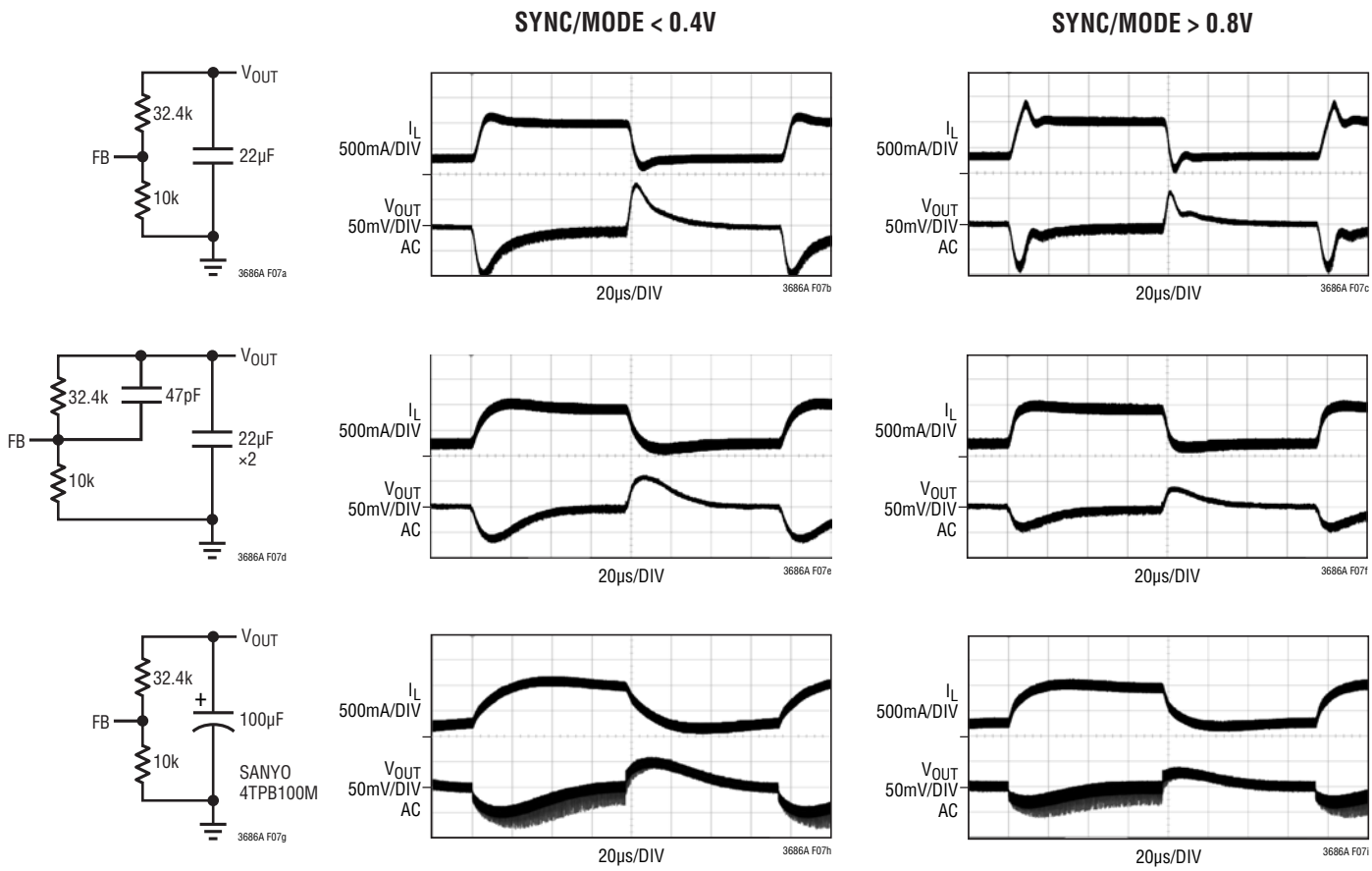


Figure 7. Transient Load Response of the LT3686A with Different Output Capacitors as the Load Current Is Stepped from 0.25A to 1A. V_{IN} = 12V, V_{OUT} = 3.3V, L = 6.8µH , Frequency = 2MHz

APPLICATIONS INFORMATION

BAT54) in parallel with the internal diode to reduce V_D. The following equations can be used to calculate and minimize boost capacitance in µF:

$$C_{BOOST} = \frac{0.065}{(V_{BD} + V_{CATCH} - V_D - 2.2) \bullet f}$$

V_D is the forward drop of the boost diode, V_{CATCH} is the forward drop of the catch diode (D1), and frequency is in MHz. A typical value of 0.22µF can be used for C_{BOOST}.

For lower output voltages the BD pin can be tied to an external voltage source with adequate local bypassing (Figure 8b). The above equations still apply for calculating the optimal boost capacitor for the chosen BD voltage. The absence of BD voltage during startup will increase minimum voltage to start and reduce efficiency. You must also be sure that the maximum voltage rating of BOOST pin is not exceeded. The BD pin can also be tied to V_{IN} (Figure 8c) but V_{IN} will be limited to 25V and the active load circuit is automatically disabled.

The minimum operating voltage of an LT3686A application is limited by the undervoltage lockout (3.6V) and by the maximum duty cycle as outlined above. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or

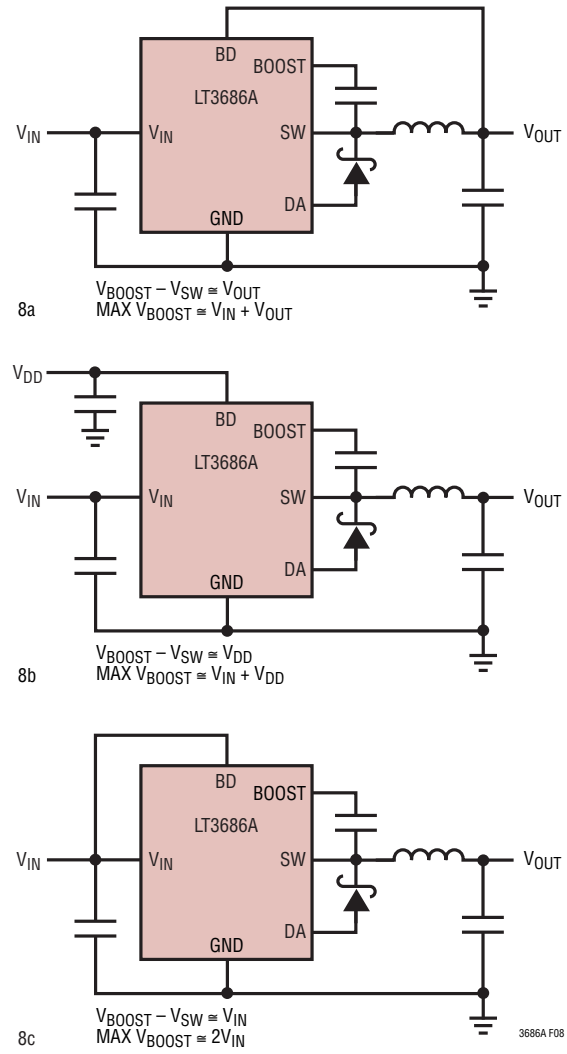


Figure 8.

APPLICATIONS INFORMATION

the LT3686A is turned on with its EN/UVLO pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly.

This minimum load will depend on the input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. Figure 9 shows plots of minimum load to start and to run as a function of input voltage. In many cases the discharged output capacitor will present a load to the switcher which will allow it to start. At light loads, the inductor current becomes discontinuous and the effective duty cycle can be very high. This reduces the minimum input voltage to approximately 400mV above V_{OUT}. At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle, requiring a higher input voltage to maintain regulation.

As the LT3686A enters dropout, the boost capacitor voltage will be limited by V_{OUT}, which is fixed by the maximum duty cycle. If the boost capacitor's voltage during dropout falls

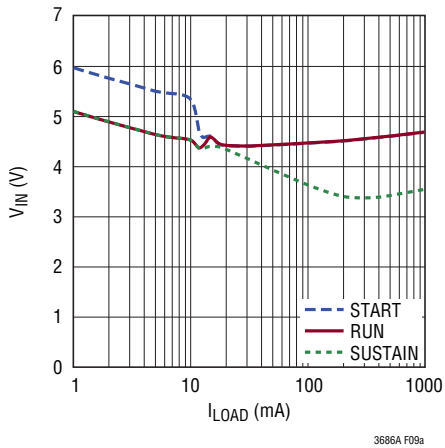


Figure 9a. Typical Minimum Input Voltage, V_{OUT} = 3.3V, f = 1MHz, L = 15µH, SYNC/MODE < 0.4V

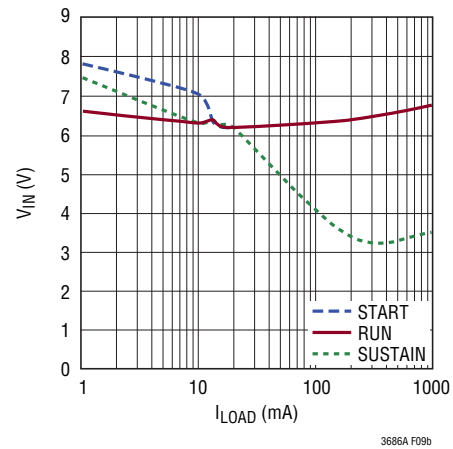


Figure 9b. Typical Minimum Input Voltage, V_{OUT} = 5V, f = 1MHz, L = 22µH, SYNC/MODE < 0.4V

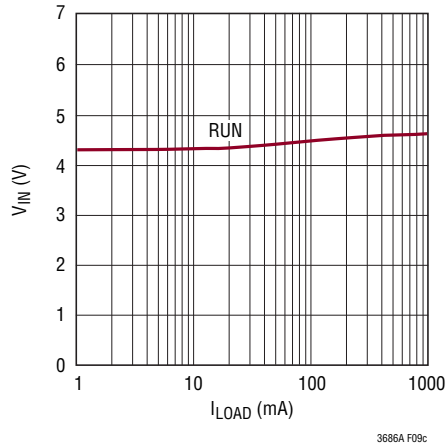


Figure 9c. Typical Minimum Input Voltage, V_{OUT} = 3.3V, f = 1MHz, L = 15µH, SYNC/MODE > 0.8V

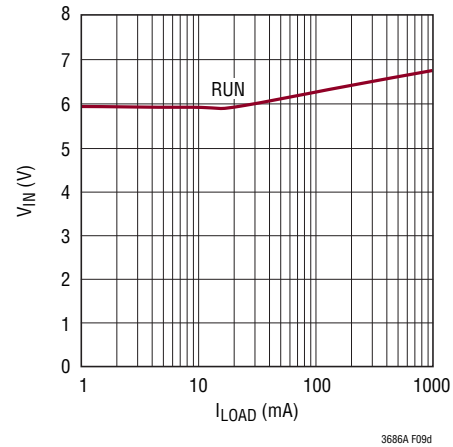


Figure 9d. Typical Minimum Input Voltage, V_{OUT} = 5V, f = 1MHz, L = 22µH, SYNC/MODE > 0.8V

APPLICATIONS INFORMATION

below the minimum voltage to sustain boosted operation (2.2V across the boost capacitor), the output voltage will fall suddenly to:

$$V_{OUT} = (V_{IN} – 2.2) \bullet DC_{MAX}$$

Figure 9 shows the minimum V_{IN} necessary to *sustain* boosted operation during dropout. Once V_{IN} drops below the *sustain* voltage, V_{IN} will need to reach the *start* voltage again to refresh the boost capacitor. The programmable undervoltage lockout (UVLO) function can be used to avoid operating unless V_{IN} is greater than the *start* voltage.

Fixed Frequency at Light Load

The LT3686A contains unique active load circuitry to allow for full frequency switching at very light loads. To enable the active load, drive the SYNC/MODE pin with clock pulses or a DC voltage greater than 0.8V.

Typical fixed frequency nonsynchronous buck regulators skip pulses at light loads. With a fixed input voltage, as the load current decreases in discontinuous mode, the regulator is required to switch for shorter periods of time. When the required on time decreases below the typical minimum on time, the regulator skips one or more pulses so the effective average duty cycle is equal to the required duty cycle. This likelihood of entering pulse-skipping is exacerbated by the tendency for minimum on time to increase at very light loads. Pulse-skipping is undesirable because it causes unpredictable, sub-harmonic output ripple that can interfere with the operation of other sensitive components such as AM receivers and audio equipment.

The BD active load is designed to combat pulse-skipping by providing an operational regime between full frequency discontinuous and pulse-skipping modes.

The maximum V_{IN} before pulse-skipping in discontinuous mode is directly dependent on load current; as the load decreases, so does the pulse-skipping boundary. An artificial load on the output helps push the pulse-skipping boundary higher. The LT3686A achieves this goal by commanding the minimum load necessary to keep itself at full switching frequency, hence the circuitry is called an active load.

As the LT3686A approaches minimum on time in discontinuous mode, its power switch transitions smoothly into a fixed on time, fixed frequency, open loop current source. Instead of controlling switch current, the internal error amplifier servos the active load on the output via the BD pin to maintain output voltage regulation. The impact on efficiency is mitigated by pulling the minimum current necessary to keep switching at full frequency. The necessary BD load to maintain output regulation depends on V_{IN}, inductor size, and load current. As the necessary BD load increases beyond its 40mA limit, pulse-skipping mode will resume.

The BD active load circuitry is enabled when MODE tied high and disabled when MODE is tied low. Even when activated, the active load will shutdown when BD voltage exceeds either 6V or V_{IN} in an effort to minimize power dissipation and intelligently react to external configurations.

To address the startup concerns delineated in the BOOST and BD Pin Considerations section, the active load will assist startup by pulling maximum current (40mA) to charge the boost capacitor voltage in the absence of an adequate load. An internal power good circuit will disable the BD active load when V_{FB} reaches 0.7V. Figure 9 compares plots of minimum input voltage to start and run as a function of load current. In many cases the discharged output capacitor will present a load to the switcher which will allow it to start. The plots show the worst-case situation where V_{IN} is ramping very slowly.

The active load also activates to hasten the recharge of boost cap when operating beyond maximum duty cycle.

When not in use, the active load pulls no current.

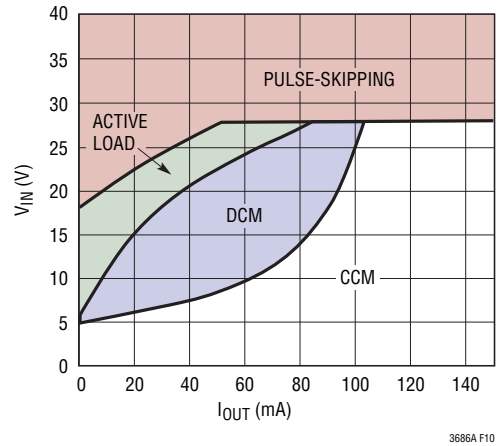


Figure 10. Regions of Operation ($5V_{OUT}$, 2MHz)

APPLICATIONS INFORMATION

Soft-Start

The SS pin is used to soft-start the LT3686A, eliminating input current surge during start-up. It can also be used to track another voltage in the system (Figure 11).

An internal 2µA current source charges an external soft-start capacitor to generate a voltage ramp. FB voltage is regulated to the voltage at the SS pin until it exceeds 0.8V, FB is then regulated to the reference 0.8V. Soft-start also reduces the oscillator frequency to avoid hitting current limit during start-up. Figure 12 shows the start-up waveforms with and without the soft-start circuit.

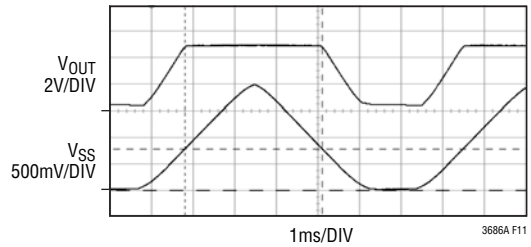


Figure 11. LT3686A Configured to Track Voltage on SS Pin

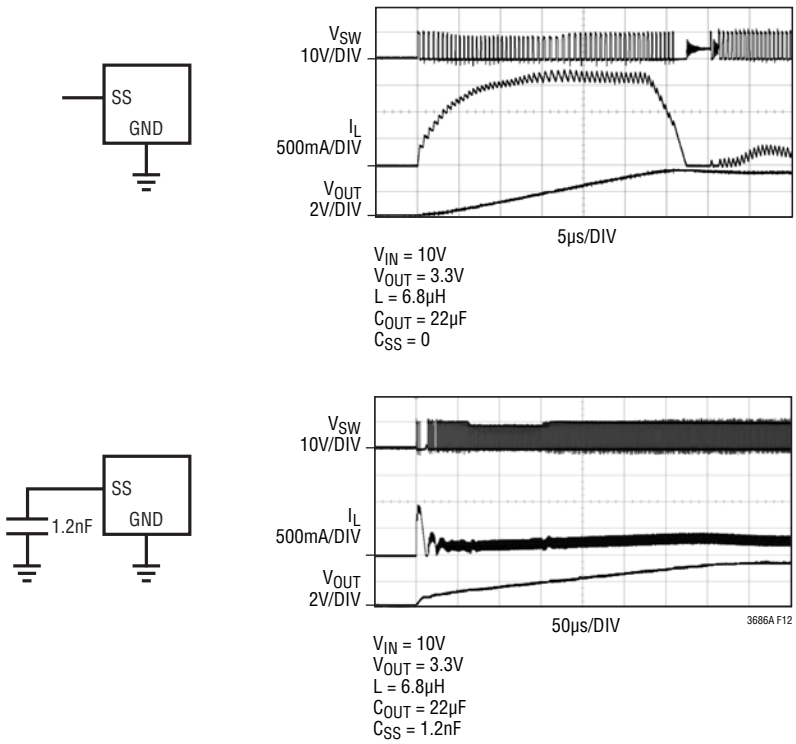


Figure 12. To Soft Start the LT3686A, Add a Capacitor to the SS Pin

APPLICATIONS INFORMATION

Short and Reverse Protection

If the inductor is chosen so that it won't saturate excessively, the LT3686A will tolerate a shorted output. When operating in short-circuit condition, the LT3686A will reduce its frequency until the valley current is 1.7A (Figure 13). There is another situation to consider in systems where the output will be held high when the input to the LT3686A is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LT3686A's output. If the V_{IN} pin is allowed to float and the EN/UVLO pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3686A's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a few mA in this state. If you ground the EN/UVLO pin, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3686A can pull large currents from the output through the SW pin and the V_{IN} pin. Figure 14 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LT3686A circuits. However, these capacitors can cause problems if the LT3686A is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LT3686A can ring to twice the nominal input voltage, possibly exceeding the LT3686A's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging

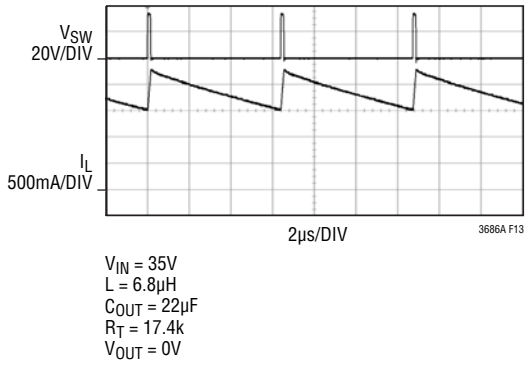


Figure 13. The LT3686A Reduces its Frequency from 2MHz to 160kHz to Protect Against Shorted Output

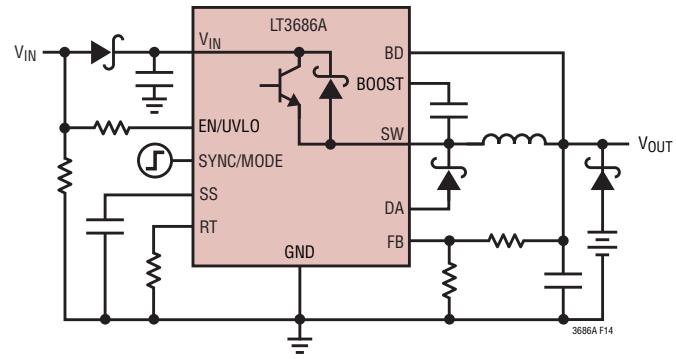


Figure 14. Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output; it Also Protects the Circuit from a Reversed Input. The LT3686A Runs Only When the Input is Present

APPLICATIONS INFORMATION

the LT3686A into an energized supply, the input network should be designed to prevent this overshoot. Figure 15 shows the waveforms that result when an LT3686A circuit is connected to a 24V supply through six feet of 24-gauge twisted pair. The first plot is the response with a 2.2µF ceramic capacitor at the input. The input voltage rings as high as 35V and the input current peaks at 20A. One method of damping the tank circuit is to add another capacitor with a series resistor to the circuit. In Figure 15b an aluminum electrolytic capacitor has been added. This capacitor's high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit. An alternative solution is shown in Figure 15c. A 1Ω resistor is added in series with the input to eliminate the voltage overshoot (it also reduces the peak input current). A 0.1µF capacitor improves high frequency filtering. This solution is smaller and less expensive than the electrolytic capacitor. For high input voltages its impact on efficiency is minor, reducing efficiency one percent for a 5V output at full load operating from 24V.

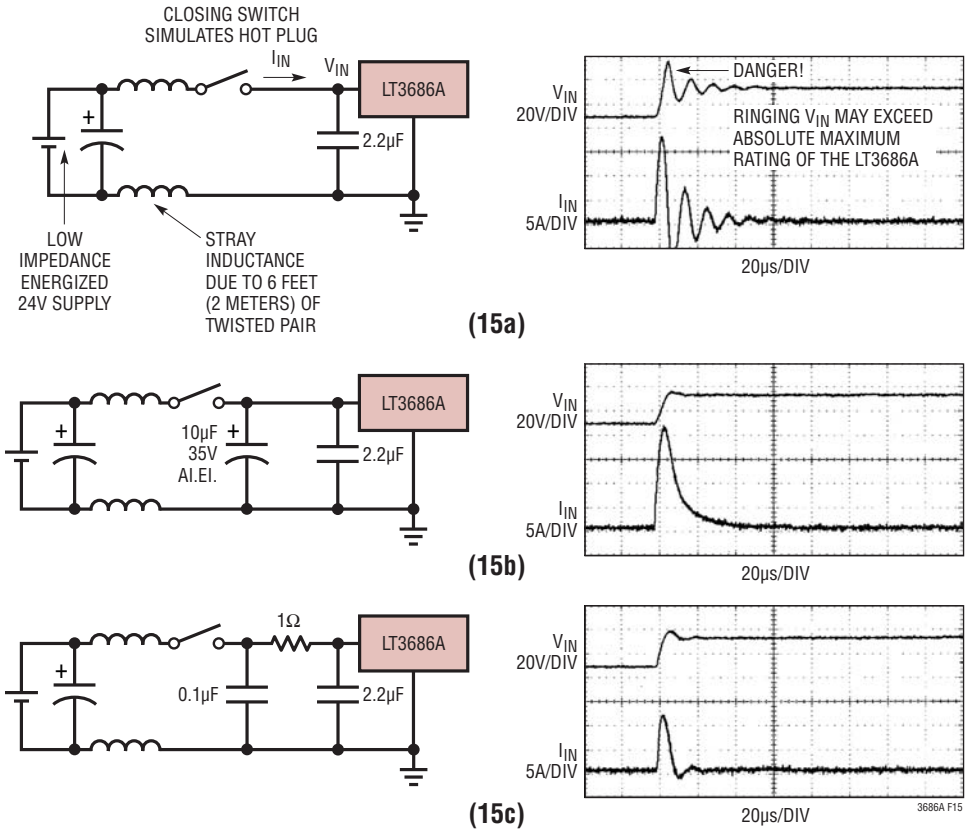


Figure 15. A Well Chosen Input Network Prevents Input Voltage Overshoot and Ensures Reliable Operation When the LT3686A Is Connected to a Live Supply

APPLICATIONS INFORMATION

Frequency Compensation

The LT3686A uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3686A does not require the ESR of the output capacitor for stability allowing the use of ceramic capacitors to achieve low output ripple and small circuit size. Figure 16 shows an equivalent circuit for the LT3686A control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C node. Note that the output capacitor integrates this current, and that the capacitor on the V_C node (C_C) integrates the error amplifier output current, resulting in two poles in the loop. R_C provides a zero. With the recommended output capacitor, the loop crossover occurs above the R_CC_C zero. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. With a larger ceramic capacitor (very low ESR), crossover may be lower and a phase lead capacitor (CPL) across the feedback divider may improve the phase margin and transient response. Large electrolytic capacitors may have an ESR large enough to create an additional zero, and the phase lead may not be necessary. If the output capacitor is different than the recommended capacitor, stability should be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

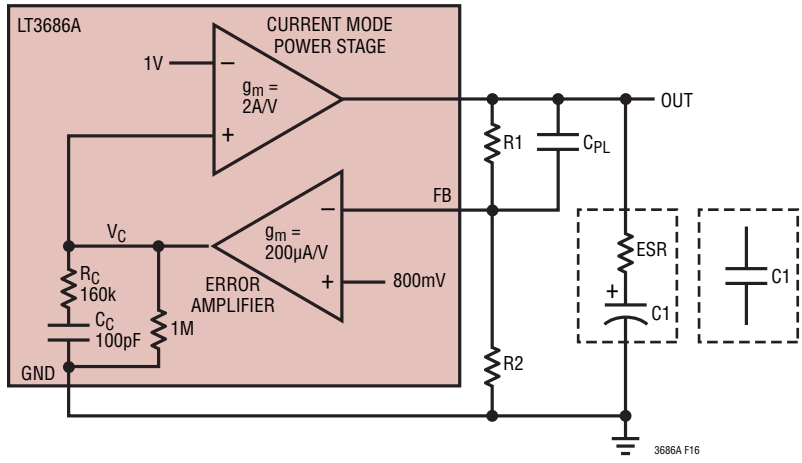


Figure 16. Model for Loop Response

APPLICATIONS INFORMATION

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 17 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3686A's V_{IN} and SW pins, the catch diode (D1) and the input capacitor (C2). The loop formed by these components should be as small as possible and tied to system ground in only one place. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location, ideally at the ground terminal of the output capacitor C1. The SW and BOOST nodes should be as small as possible. Finally, keep the FB node small so that the ground pin and ground traces will shield it from the SW and BOOST nodes. Include vias near the exposed GND pad of the LT3686A to help remove heat from the LT3686A to the ground plane.

High Temperature Considerations

The die temperature of the LT3686A must be lower than the maximum rating of 125°C (150°C for LT3686AH). For high ambient temperatures, care should be taken in the layout of the circuit to ensure good heat sinking of the LT3686A. The maximum load current should be derated as the ambient temperature approaches the maximum allowed junction temperature. The die temperature is calculated by multiplying the LT3686A power dissipation by the thermal resistance from junction to ambient. Power dissipation within the LT3686A can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss. The resulting temperature rise at full load is nearly independent of input voltage. Thermal resistance depends on the layout of the circuit board, but 43°C/W is typical for the (3mm × 3mm) DFN package.

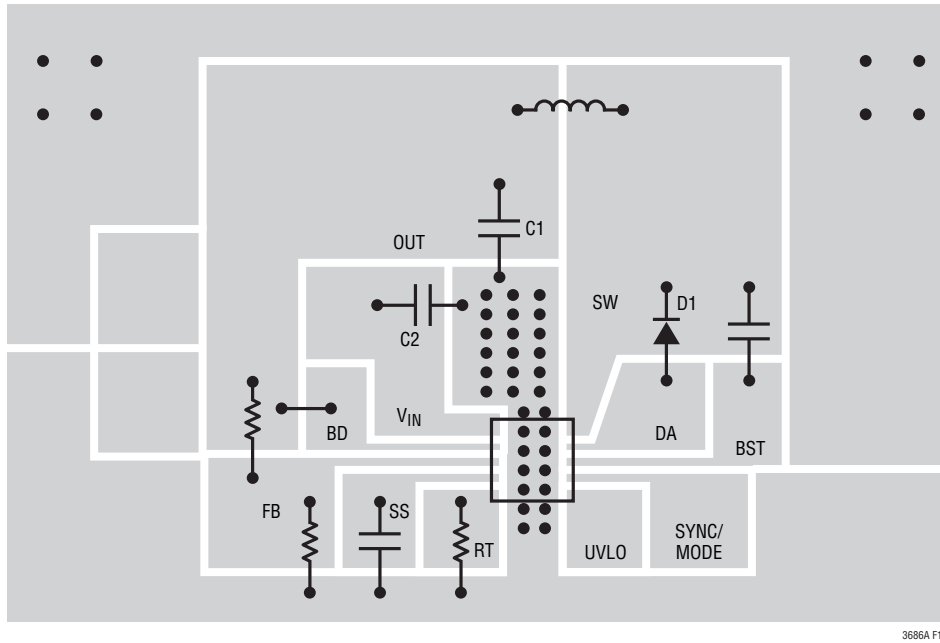


Figure 17. PCB Layout

APPLICATIONS INFORMATION

Outputs Greater Than 19V

Note that for outputs above 19V, the input voltage range will be limited by the maximum rating of the BOOST pin. The sum of input and output voltages cannot exceed the BOOST pin's 55V rating. The 25V circuit (Figure 18) shows how to overcome this limitation using an additional Zener diode.

Other Linear Technology Publications

Application Notes 19, 35 and 44 contain more detailed descriptions and design information for Buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

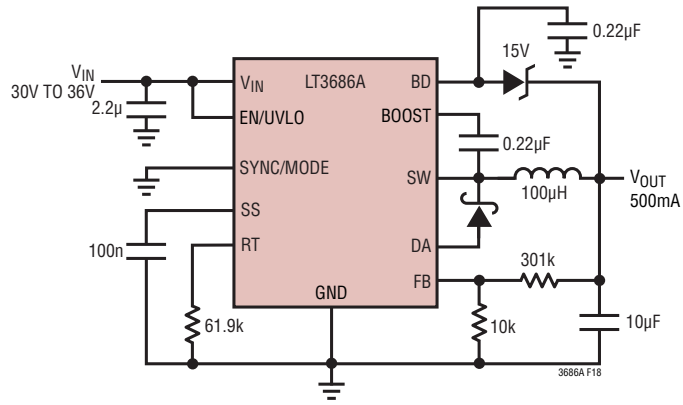
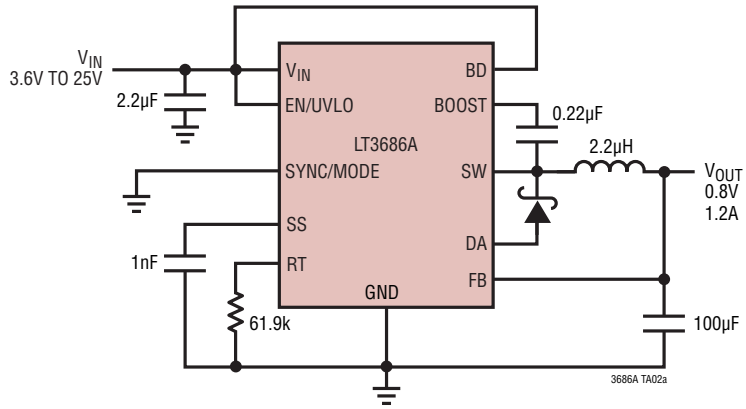


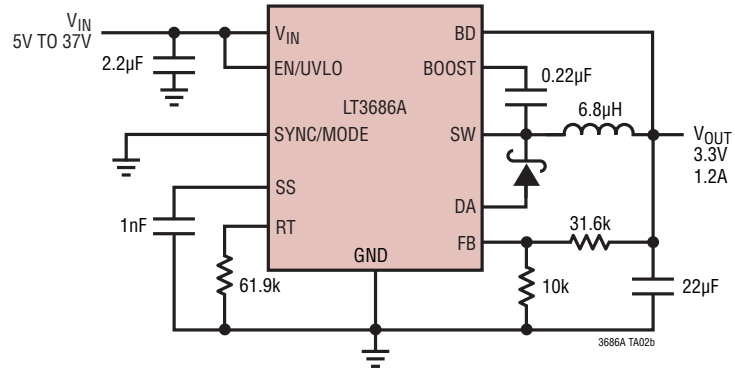
Figure 18. 25V Step-Down Converter

TYPICAL APPLICATIONS

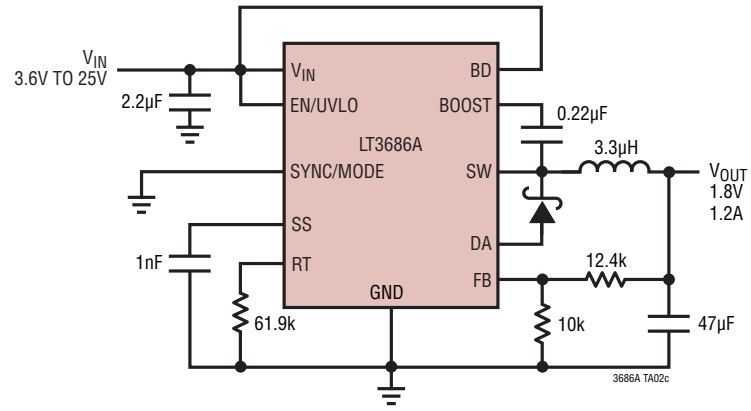
0.8V Step-Down Converter



3.3V Step-Down Converter

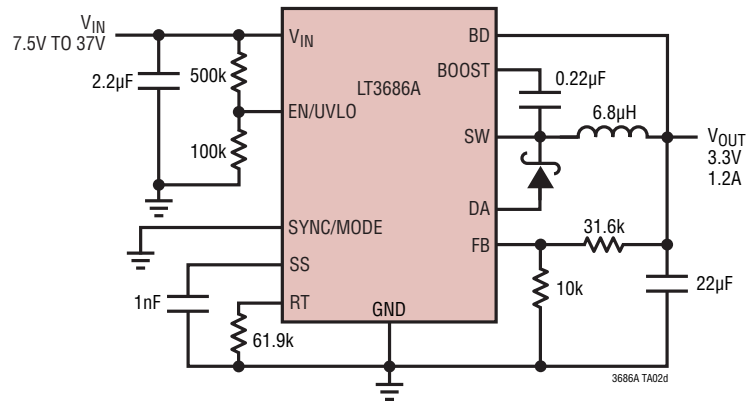


1.8V Step-Down Converter

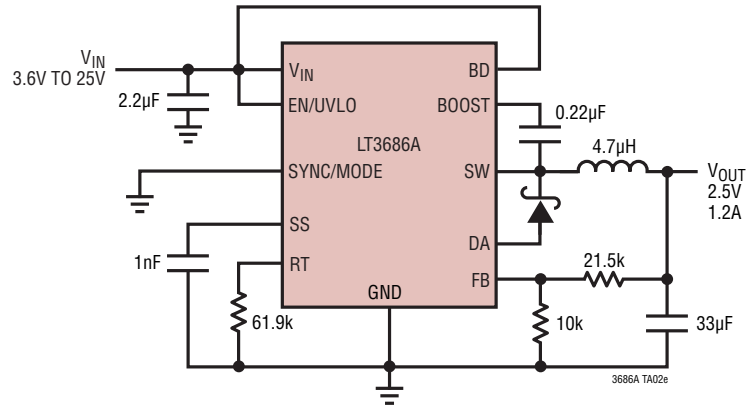


TYPICAL APPLICATIONS

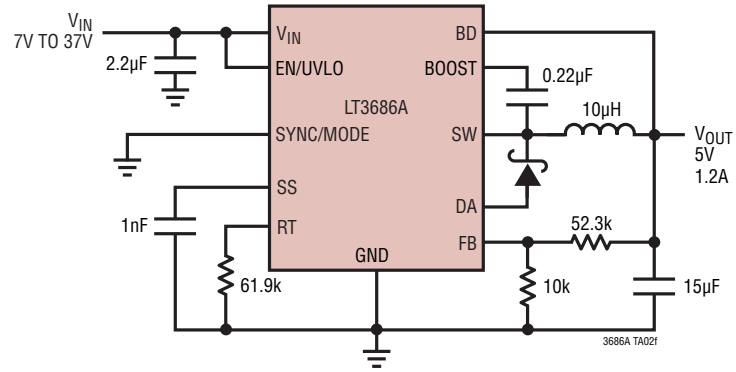
3.3V Step-Down Converter with Programmed UVLO



2.5V Step-Down Converter

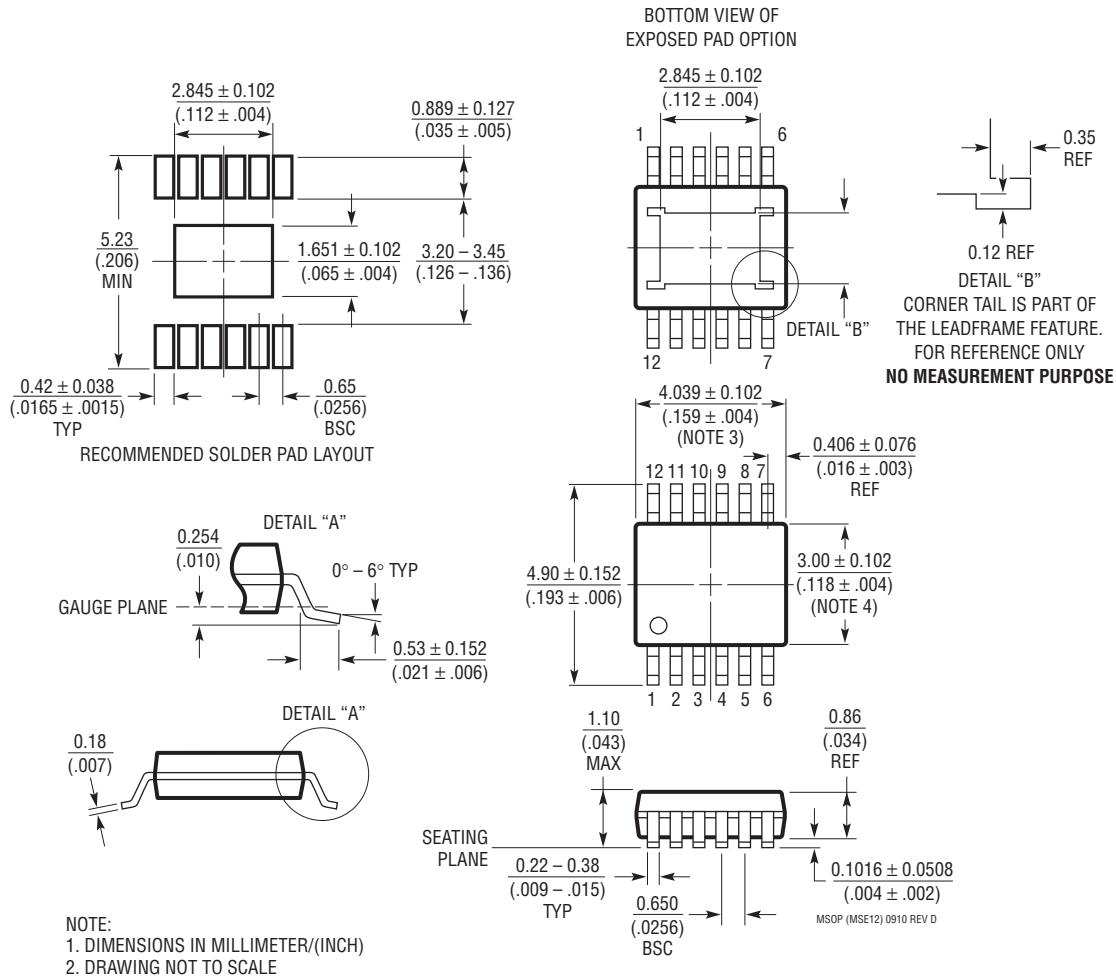


5V Step-Down Converter



PACKAGE DESCRIPTION

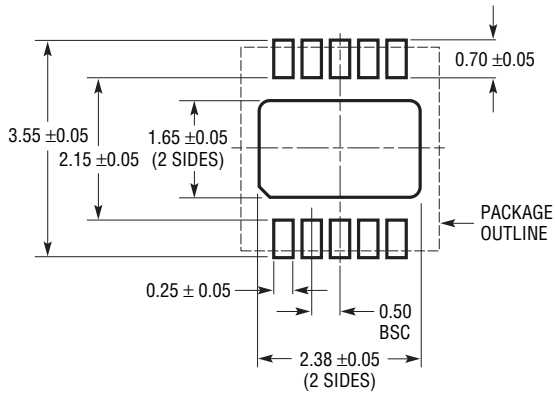
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev D)



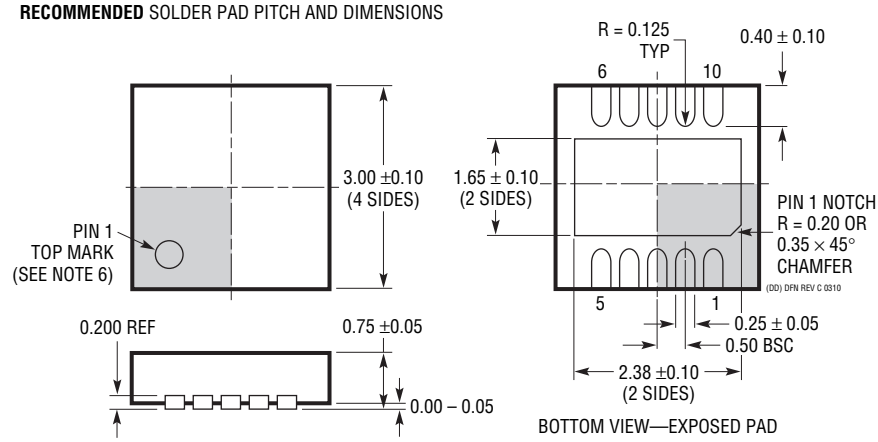
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

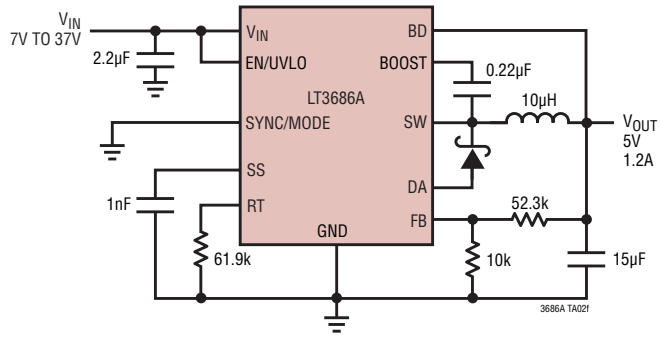
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/11	Revised MSOP in Features, Pin Configuration, Order Information and Package Description sections	1, 2, 27
		Updated Electrical Characteristics section	3
		Updated value for EN/UVLO pin in Pin Functions section	7
		Updated values in Operation section	9
		Revised equation in Programmable Undervoltage Lockout section, Table 1 and minor text edit to Minimum On Time in Applications Information section	10, 12, 13

TYPICAL APPLICATION

5V Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3686	37V, 55V with Transient Protection 1.2A, 2.5MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 37V, Transient to 55V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.1mA, I_{SD} <1µA, 10-Pin 3mm × 3mm DFN Package
LT3689	36V, 60V Transient Protection, 800mA, 2.2MHz, High Efficiency MicroPower Step-Down DC/DC Converter with POR Reset and Watchdog Timer	V_{IN}: 3.6V to 36V Transient to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1µA, 16-Pin 3mm × 3mm QFN Package
LT3682	36V, 60V_{MAX}, 1A, 2.2MHz, High Efficiency MicroPower Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1µA, 12-Pin 3mm × 3mm DFN Package
LT3970	40V, 350mA (I_{OUT}), 2.2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.5µA of Quiescent Current	V_{IN}: 4.2V to 40V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} <1µA, 10-Pin 2mm × 3mm DFN, 10-Pin MSOP Packages
LT3990	60V, 350mA (I_{OUT}), 2.2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.5µA of Quiescent Current	V_{IN}: 4.2V to 60V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} <1µA, 10-Pin 3mm × 3mm DFN, 16-Pin MSOPE Packages
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	V_{IN}: 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1µA, 10-Pin 3mm × 3mm DFN, 10-Pin MSOP Packages
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1µA, 10-Pin 3mm × 3mm DFN, 10-Pin MSOP Packages
LT3505	36V with Transient Protection to 40V, 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 34V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 2mA, I_{SD} = 2µA, 8-Pin 3mm × 3mm DFN, 8-Pin MSOP Packages
LT3437	60V, 400mA (I_{OUT}), MicroPower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 100µA, I_{SD} <1µA, 10-Pin 3mm × 3mm DFN, 16-Pin TSSOP Packages
LT1976/LT1977	60V, 1.2A (I_{OUT}), 200/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 100µA, I_{SD} <1µA, 16-Pin TSSOP Package

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