PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

# MC-22106

## MCP (MULTI-CHIP PACKAGE) FLASH MEMORY AND SRAM
## 16M-BIT FLASH MEMORY AND 1M-BIT SRAM

### Description

The MC-22106 is a MCP (Multi-Chip Package) of 16,777,216 bits (1,048,576 words by 16 bits) flash memory and 1,048,576 bits (131,072 words by 8 bits) static RAM.

The MC-22106 is packaged in a 48-pin plastic BGA.

### Features

**General Features**

- Fast access time : 100 ns (MAX.)
- Voltage range : $V_{CC}$ = 2.7 to 3.6 V
- Wide operating temperature : –20 to +85 °C

**Flash Memory Features**

- 1,048,576 words by 16 bits organization
- Minimum number of repetitions for program / erase : 100,000 times
- Sector erase architecture :
  35 sectors (1 × 8K bytes, 2 × 4K bytes, 1 × 16K bytes, and 31 × 32K bytes)
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- Boot code sector at the top sector
- Automatic erase function
- Functions for automatic erasure :
  Erase suspend / resume function
- Automatic program function
- Data polling and toggle bit
- Ready (Busy) output (RY (/BY))
- Supply current
  Reset mode : 5.0 μA (MAX.)
  Standby mode : 5.0 μA (MAX.)
  Operating mode : 35 mA (MAX.)

**SRAM Features**

- 131,072 words by 8 bits organization
- Supply current
  At operating : 35 mA (MAX.)
  At standby : 26 μA (MAX.)
- Two Chip Enable inputs : /CE1s, CE2s
- Data retention supply voltage : 2.0 to 3.6 V

**The information in this document is subject to change without notice.**

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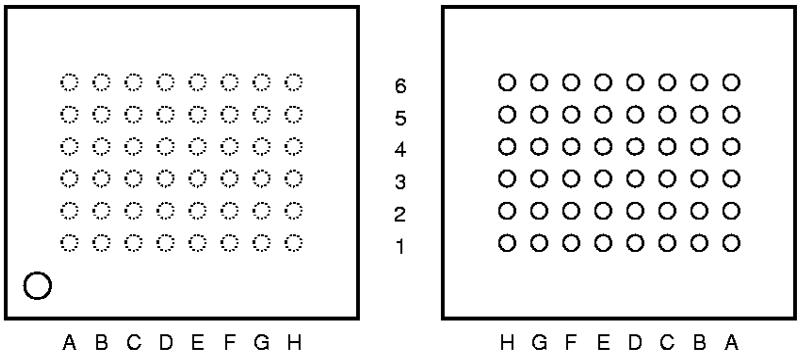
## Ordering Information

| Part number | Flash Memory Boot code sector | Flash Memory Access time (MAX.) | SRAM Access time (MAX.) | Package |
|---|---|---|---|---|
| MC-22106F1-DE1-B10 | at the top sector | 100 ns | 100 ns | 48-pin plastic BGA (10 × 14 mm) |

## Pin Configuration

**48-pin Plastic BGA (10 × 14 mm)**

**Top View** **Bottom View**




**Top View**

| | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 6 | /CE1s | Vss | I/O1 | A1 | A2 | A4 | CE2s | A9 |
| 5 | A10 | I/O5 | I/O2 | A0 | A3 | A7 | RY (/BY) | A14 |
| 4 | /OE | I/O7 | I/O4 | I/O0 | A6 | A18 | /RESET | A15 |
| 3 | A11 | A8 | A5 | I/O8 | I/O3 | I/O12 | A12 | A19 |
| 2 | A13 | A17 | SA | /CEf | I/O10 | Vccf | I/O6 | I/O15 / A–1 |
| 1 | /WE | Vccs | A16 | Vss | I/O9 | I/O11 | I/O13 | I/O14 |

**Common Pins**

A0 - A15 : Address Inputs
I/O0 - I/O7 : Data Inputs / Outputs
/OE : Output Enable
/WE : Write Enable
Vss : Ground
NC [Note] : No Connection

**Flash Memory Pins**

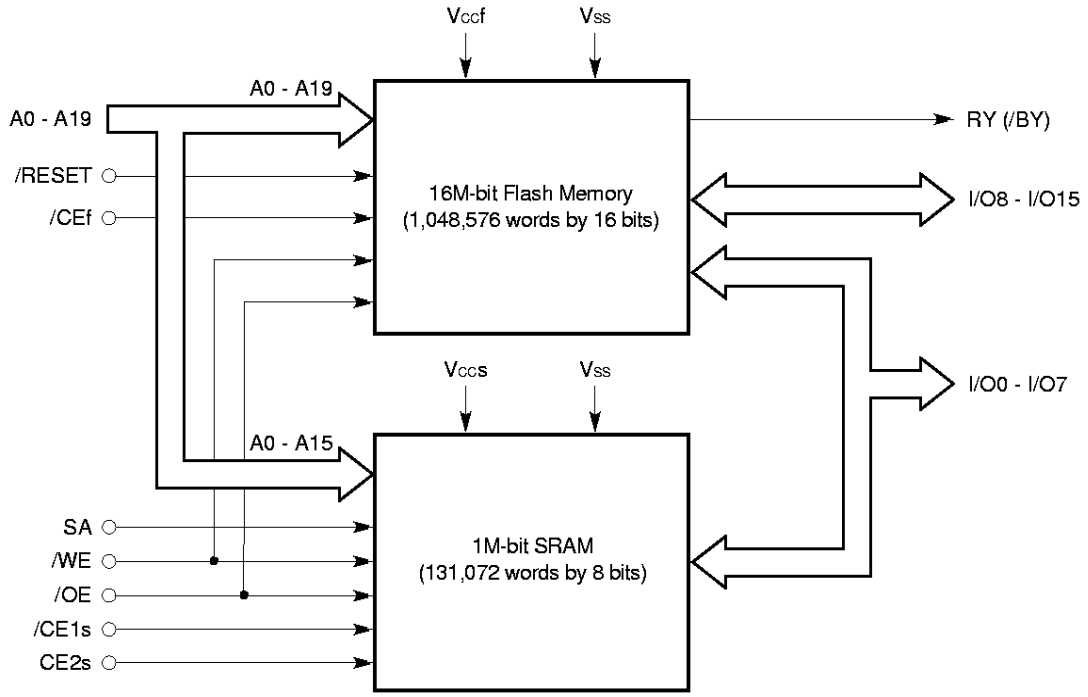
A16 - A19 : Address Inputs (Flash Memory)
I/O8 - I/O15 : Data Inputs / Outputs (Flash Memory)
/CEf : Chip Enable (Flash Memory)
RY (/BY) : Ready (Busy) Outputs
/RESET : Hardware Reset Input
Vccf : Supply Voltage (Flash Memory)

**SRAM Pins**

SA : Address Input (A16 for SRAM)
/CE1s : Chip Enable 1 (SRAM)
CE2s : Chip Enable 2 (SRAM)
Vccs : Supply Voltage (SRAM)

**Note** Some signals can be applied because this pin is not internally connected.

## Block Diagram




## Bus Operations

| Operation | Flash Memory | | SRAM | | Common | | |
|---|---|---|---|---|---|---|---|
| | /RESET | /CEf | /CE1s | CE2s | /OE | /WE | I/O0 - I/O7 |
| Full standby | H | H | H | × | × | × | Hi-Z |
| | | | × | L | | | |
| Output disable | H | × | × | × | H | H | Hi-Z |
| Read from Flash Memory [Note] | H | L | H | × | L | H | Data out |
| | | | × | L | | | |
| Write to Flash Memory | H | L | H | × | H | L | Data in |
| | | | × | L | | | |
| Flash Memory hardware reset | L | × | H | × | × | × | Hi-Z |
| | | | × | L | | | |
| Read from SRAM | H | H | L | H | L | H | Data out |
| Write to SRAM | H | H | L | H | × | L | Data in |

**Note** /WE can be $V_{IL}$ if /OE is $V_{IL}$, /OE at $V_{IH}$ initiates the write operations.

**Remarks 1.** × : Don't care

H : $V_{IH}$

L : $V_{IL}$

**2.** Other operations except for indicated in this table are inhibited.

**3.** Do not apply /CEf = $V_{IL}$, /CE1s = $V_{IL}$ and CE2s = $V_{IH}$ at a time.

## Sector Layout / Sector Address Table (Flash Memory)

| Sector Layout | Address | Sector address | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|
| 8K words | FFFFFH<br>FE000H | SA34 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | × |
| 4K words | FDFFFH<br>FD000H | SA33 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 4K words | ECFFFH<br>FC000H | SA32 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 16K words | FBFFFH<br>F8000H | SA31 | 1 | 1 | 1 | 1 | 1 | 0 | × | × |
| 32K words | F7FFFH<br>F0000H | SA30 | 1 | 1 | 1 | 1 | 0 | × | × | × |
| 32K words | EFFFFH<br>E8000H | SA29 | 1 | 1 | 1 | 0 | 1 | × | × | × |
| 32K words | E7FFFH<br>E0000H | SA28 | 1 | 1 | 1 | 0 | 0 | × | × | × |
| 32K words | DFFFFH<br>D8000H | SA27 | 1 | 1 | 0 | 1 | 1 | × | × | × |
| 32K words | D7FFFH<br>D0000H | SA26 | 1 | 1 | 0 | 1 | 0 | × | × | × |
| 32K words | CFFFFH<br>C8000H | SA25 | 1 | 1 | 0 | 0 | 1 | × | × | × |
| 32K words | C7FFFH<br>C0000H | SA24 | 1 | 1 | 0 | 0 | 0 | × | × | × |
| 32K words | BFFFFH<br>B8000H | SA23 | 1 | 0 | 1 | 1 | 1 | × | × | × |
| 32K words | B7FFFH<br>B0000H | SA22 | 1 | 0 | 1 | 1 | 0 | × | × | × |
| 32K words | AFFFFH<br>A8000H | SA21 | 1 | 0 | 1 | 0 | 1 | × | × | × |
| 32K words | A7FFFH<br>A0000H | SA20 | 1 | 0 | 1 | 0 | 0 | × | × | × |
| 32K words | 9FFFFH<br>98000H | SA19 | 1 | 0 | 0 | 1 | 1 | × | × | × |
| 32K words | 97FFFH<br>90000H | SA18 | 1 | 0 | 0 | 1 | 0 | × | × | × |
| 32K words | 8FFFFH<br>88000H | SA17 | 1 | 0 | 0 | 0 | 1 | × | × | × |
| 32K words | 87FFFH<br>80000H | SA16 | 1 | 0 | 0 | 0 | 0 | × | × | × |
| 32K words | 7FFFFH<br>78000H | SA15 | 0 | 1 | 1 | 1 | 1 | × | × | × |
| 32K words | 77FFFH<br>70000H | SA14 | 0 | 1 | 1 | 1 | 0 | × | × | × |
| 32K words | 6FFFFH<br>68000H | SA13 | 0 | 1 | 1 | 0 | 1 | × | × | × |
| 32K words | 67FFFH<br>60000H | SA12 | 0 | 1 | 1 | 0 | 0 | × | × | × |
| 32K words | 5FFFFH<br>58000H | SA11 | 0 | 1 | 0 | 1 | 1 | × | × | × |
| 32K words | 57FFFH<br>50000H | SA10 | 0 | 1 | 0 | 1 | 0 | × | × | × |
| 32K words | 4FFFFH<br>48000H | SA9 | 0 | 1 | 0 | 0 | 1 | × | × | × |
| 32K words | 47FFFH<br>40000H | SA8 | 0 | 1 | 0 | 0 | 0 | × | × | × |
| 32K words | 3FFFFH<br>38000H | SA7 | 0 | 0 | 1 | 1 | 1 | × | × | × |
| 32K words | 37FFFH<br>30000H | SA6 | 0 | 0 | 1 | 1 | 0 | × | × | × |
| 32K words | 2FFFFH<br>28000H | SA5 | 0 | 0 | 1 | 0 | 1 | × | × | × |
| 32K words | 27FFFH<br>20000H | SA4 | 0 | 0 | 1 | 0 | 0 | × | × | × |
| 32K words | 1FFFFH<br>18000H | SA3 | 0 | 0 | 0 | 1 | 1 | × | × | × |
| 32K words | 17FFFH<br>10000H | SA2 | 0 | 0 | 0 | 1 | 0 | × | × | × |
| 32K words | 0FFFFH<br>08000H | SA1 | 0 | 0 | 0 | 0 | 1 | × | × | × |
| 32K words | 07FFFH<br>00000H | SA0 | 0 | 0 | 0 | 0 | 0 | × | × | × |

## Command Definitions (Flash Memory)

| Command sequence | Bus cycles | 1st bus write cycle | | 2nd bus write cycle | | 3rd bus write cycle | | 4th bus read / write cycle | | 5th bus write cycle | | 6th bus write cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data |
| Read / Reset Note 1 | 1 | xxxH | F0H | – | – | – | – | – | – | – | – | – | – |
| Read / Reset Note 1 | 3 | 555H | AAH | 2AAH | 55H | 555H | F0H | RA | RD | – | – | – | – |
| Read Product ID code (Manufacturer code / Device code) | 3 | 555H | AAH | 2AAH | 55H | 555H | 90H | – | – | – | – | – | – |
| Program | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA | PD | – | – | – | – |
| Chip erase | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| Sector erase | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | SA | 30H |
| Sector erase suspend Note 2 | 1 | xxxH | B0H | – | – | – | – | – | – | – | – | – | – |
| Sector erase resume Note 3 | 1 | xxxH | 30H | – | – | – | – | – | – | – | – | – | – |
| Set to fast mode | 3 | 555H | AAH | 2AAH | 55H | 555H | 20H | – | – | – | – | – | – |
| Fast program Note 4 | 2 | xxxH | A0H | PA | PD | – | – | – | – | – | – | – | – |
| Reset from fast mode Note 4 | 2 | xxxH | 90H | xxxH | F0H | – | – | – | – | – | – | – | – |
| Extended sector protect Note 4 | 4 | xxxH | 60H | SPA | 60H | SPA | 40H | SPA | SD | – | – | – | – |

**Notes 1.** Both Read / Reset commands are functionally equivalent, resetting the device to the read mode.

**2.** Sector erase can be suspended during sector erase with Addr. = $V_{IH}$ or $V_{IL}$, Data = B0H.

**3.** Sector erase can be resumed after sector erase suspend with Addr. = $V_{IH}$ or $V_{IL}$, Data = 30H.

**4.** These commands are valid in fast mode.

**Remarks 1.** RA : Address of the memory location to be read.

RD : Data read from location RA during read operation.

PA : Address of the memory location to be programmed. Addresses are latched in the falling edge of the write pulse.

PD : Data to be programmed at location PA.

SA : Address of the sector to be erased. The combination of A19, A18, A17, A16, A15, A14, A13 and A12 will uniquely select any sector. See **Sector Address Table**.

SPA : Sector address to be protected. Set sector address (SA), and (A6, A1, A0) to (0, 1, 0).

SD : Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

**2.** Address bits A11 to A20 = $V_{IH}$ or $V_{IL}$ for all address commands except for Program Address (PA) and Sector Address (SA).

**3.** For Bus operation, see **Bus Operations**.

## Product ID Code (Manufacturer's Code / Device Code) (Flash Memory)

| Product ID Code | Address inputs | | | |
|---|---|---|---|---|
| | A6 | A1 | A0 | Hex |
| Manufacturer's Code | L | L | L | 04H |
| Device code | L | L | H | 22C4H |

| Product ID Code | Code outputs | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | I/O 15 | I/O 14 | I/O 13 | I/O 12 | I/O 11 | I/O 10 | I/O 9 | I/O 8 | I/O 7 | I/O 6 | I/O 5 | I/O 4 | I/O 3 | I/O 2 | I/O 1 | I/O 0 | Hex |
| Manufacturer's Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04H |
| Device code | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 22C4H |

**Remark** H : $V_{IH}$

L : $V_{IL}$

## Electrical Specifications

### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | with respect to $V_{SS}$ | –0.3 to +4.6 | V |
| Input / Output voltage | $V_T$ | with respect to $V_{SS}$ | –0.3 to $V_{CCf}$ +0.5 Note | V |
| | | | –0.3 to $V_{CCS}$ +0.5 Note | |
| Operating ambient temperature | $T_A$ | | –20 to +85 | °C |
| Storage temperature | $T_{stg}$ | | –55 to +125 | °C |

**Note** During voltage transitions, inputs may undershoot $V_{SS}$ to –2.0 V, or overshoot to $V_{CCf}$ + 0.5 V or $V_{CCS}$ + 0.5 V for pulse width (≤ 20 ns).

**Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Recommended Operating Conditions

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CCf}$, $V_{CCS}$ | | 2.7 | | 3.6 | V |
| Operating ambient temperature | $T_A$ | | –20 | | +85 | °C |

## DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

### Common

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | | 2.2 | | $V_{CC}$ + 0.3 | V |
| Low level input voltage | $V_{IL}$ | | –0.3 | | 0.6 | V |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = –500 μA, $V_{CCf}$ = $V_{CCs}$ = $V_{CC}$ (MIN.) | $V_{CC}$ – 0.5 | | | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = +2.1 mA, $V_{CCf}$ = $V_{CCs}$ = $V_{CC}$ (MIN.) | | | 0.4 | V |
| Input leakage current | $I_{LI}$ | | –1.0 | | + 1.0 | μA |
| Output leakage current | $I_{LO}$ | | –1.0 | | + 1.0 | μA |

### Flash Memory

| Parameter | Symbol | Test condition | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Flash memory $V_{CC}$ supply current (Read) | $I_{CC1f}$ | $V_{CCf}$ = $V_{CC}$ (MAX.), /CEf = $V_{IL}$, /OE = $V_{IH}$ | $t_{CYCLE}$ = 10 MHz | | | 35 | mA |
| | | | $t_{CYCLE}$ = 5 MHz | | | 17 | |
| Flash memory $V_{CC}$ supply current (Program / erase) | $I_{CC2f}$ | $V_{CCf}$ = $V_{CC}$ (MAX.), /CEf = $V_{IL}$, /OE = $V_{IH}$ | | | | 35 | mA |
| Flash memory $V_{CC}$ standby current | $I_{SB1f}$ | $V_{CCf}$ = $V_{CC}$ (MAX.), /CEf = $V_{CCf}$ ± 0.3 V, /RESET = $V_{CCf}$ ± 0.3 V | | | | 5 | μA |
| Flash memory $V_{CC}$ standby current (/RESET) | $I_{SB2f}$ | $V_{CCf}$ = $V_{CC}$ (MAX.), /RESET = $V_{SS}$ ± 0.3 V | | | | 5 | μA |
| Flash memory voltage for reading product ID code and temporary sector unprotect | $V_{ID}$ | | | 11.5 | 12 | 12.5 | V |
| Flash memory low $V_{CC}$ lock-out voltage | $V_{LKO}$ | | | 2.3 | | 2.5 | V |

### SRAM

| Parameter | Symbol | Test condition | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| SRAM $V_{CC}$ supply current | $I_{CC1s}$ | /CE1s = $V_{IL}$, CE2s = $V_{IH}$, $I_{I/O}$ = 0 mA | | $t_{CYCLE}$ = 10 MHz | | | 35 | mA |
| | | | | $t_{CYCLE}$ = 1 MHz | | | 12 | |
| | $I_{CC2s}$ | /CE1s ≤ 0.2 V, CE2s ≥ $V_{CCs}$ – 0.2 V, $I_{I/O}$ = 0 mA, $V_{IL}$ ≤ 0.2 V, $V_{IH}$ ≥ $V_{CCs}$ – 0.2 V | | $t_{CYCLE}$ = 10 MHz | | | 35 | mA |
| | | | | $t_{CYCLE}$ = 1 MHz | | | 8 | |
| SRAM $V_{CC}$ standby current | $I_{SB1s}$ | /CE1s = $V_{IH}$ or CE2s = $V_{IL}$ | | | | | 2 | mA |
| | $I_{SB2s}$ | /CE1s ≥ $V_{CCs}$ – 0.2 V, CE2s ≥ $V_{CCs}$ – 0.2 V or CE2s ≤ 0.2 V | $V_{CCs}$ = 3.0 V ± 0.3 V | $T_A$ = 25 °C | | 1 | 2 | μA |
| | | | | $T_A$ = –20 to +85 °C | | | 22 | |
| | | | $V_{CCs}$ = 3.3 V ± 0.3 V | $T_A$ = 25 °C | | 2 | 3 | |
| | | | | $T_A$ = –20 to +85 °C | | | 26 | |

### Capacitance ($T_A$ = 25 °C, f = 1 MHz)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | TBD | TBD | TBD | pF |
| Output capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V | TBD | TBD | TBD | pF |

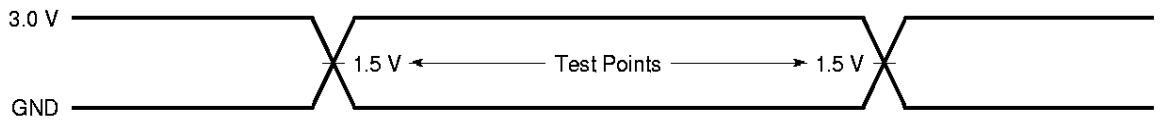
**Remarks 1.** $V_{IN}$ : Input voltage, $V_{OUT}$ : Output voltage

**2.** These parameters are periodically sampled and not 100% tested.

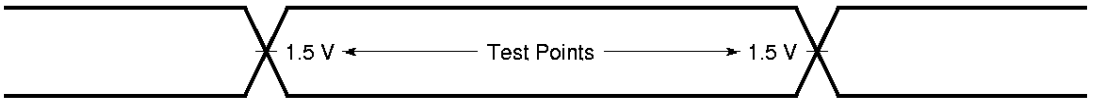
## AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

### AC Test Conditions

#### Input Waveform (Rise and Fall Time ≤ 5 ns)




#### Output Waveform



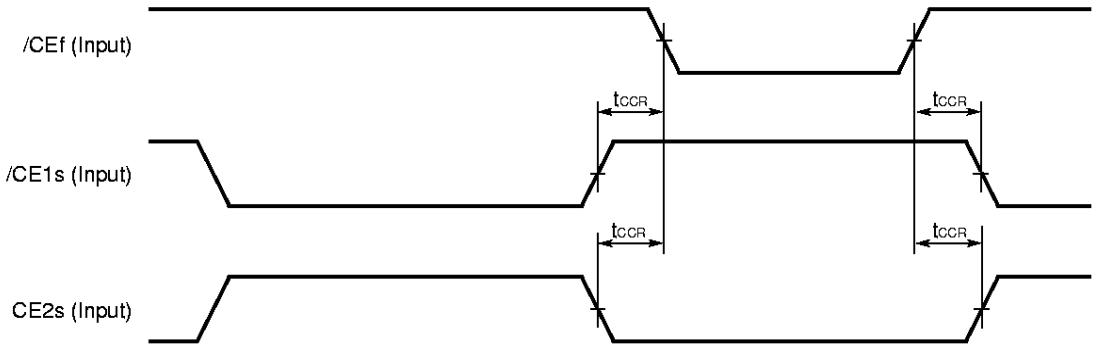

#### Output Load

1 TTL + 30 pF

### /CE Timing

| Parameter | Symbol | | Test Condition | MIN. | TYP. | MAX. | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | JEDEC | Standard | | | | | | |
| /CE recover time | – | $t_{CCR}$ | | 0 | | | ns | |

### Alternating SRAM to Flash Memory Timing Chart

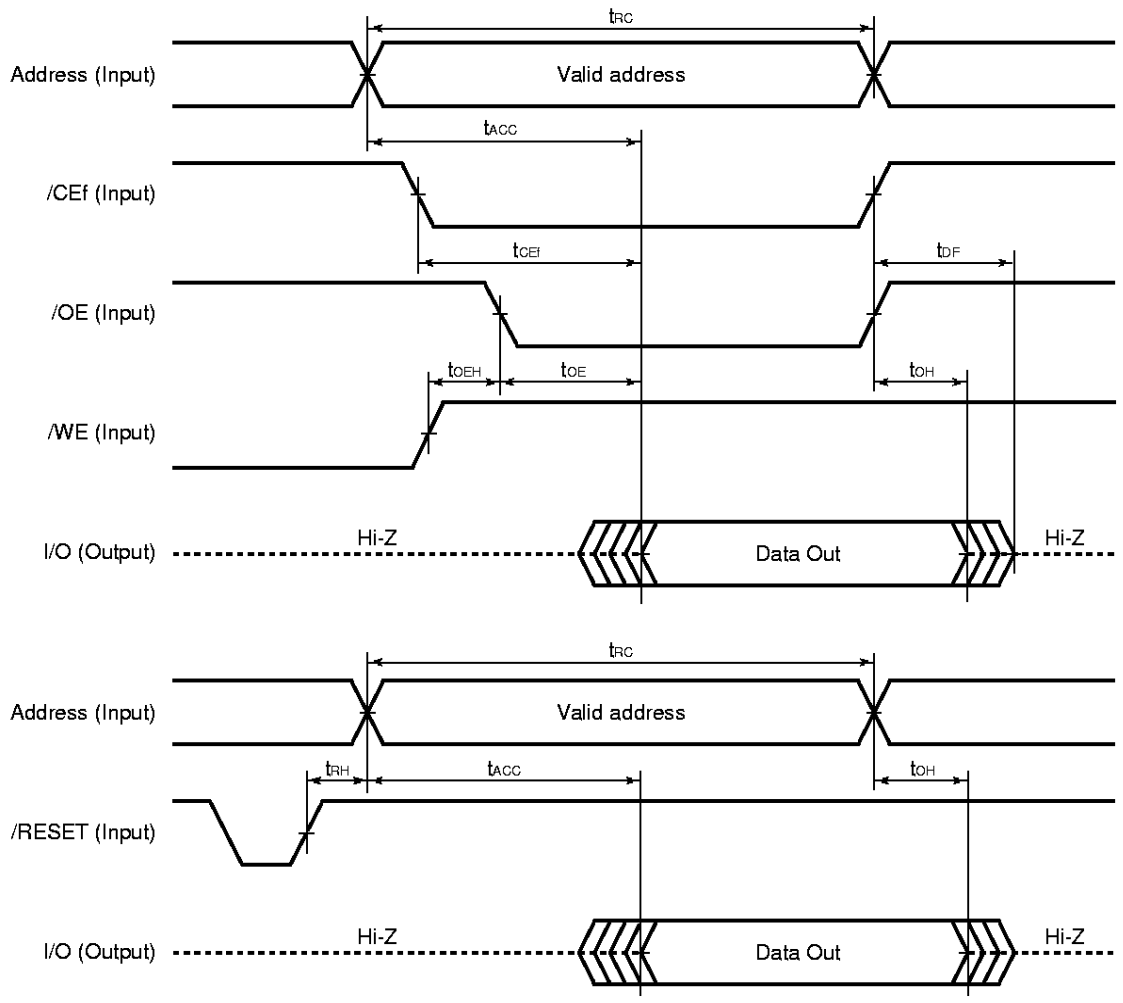


### Read Operations (Flash Memory)

| Parameter | Symbol | | Test Condition | MIN. | TYP. | MAX. | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | JEDEC | Standard | | | | | | |
| Read cycle time | $t_{AVAV}$ | $t_{RC}$ | | 100 | | | ns | |
| Address to output delay | $t_{AVQV}$ | $t_{ACC}$ | /CEf = /OE = $V_{IL}$ | | | 100 | ns | |
| /CEf to output delay | $t_{ELQV}$ | $t_{CEf}$ | /OE = $V_{IL}$ | | | 100 | ns | |
| /OE to output delay | $t_{GLQV}$ | $t_{OE}$ | /CEf = $V_{IL}$ | | | 40 | ns | |
| /CEf to output Hi-Z | $t_{EHQZ}$ | $t_{DF}$ | /OE = $V_{IL}$ | | | 30 | ns | |
| /OE to output Hi-Z | $t_{GHQZ}$ | $t_{DF}$ | /CEf = $V_{IL}$ | | | 30 | ns | |
| Output hold time from addresses, /CEf or /OE, whichever occurs first | $t_{AXQX}$ | $t_{OH}$ | | 0 | | | ns | |
| /RESET hold time before read | – | $t_{RH}$ | | 200 | | | ns | |
| /RESET pin low to read mode | – | $t_{READY}$ | | | | 20 | μs | |

**Remark** $t_{DF}$ is the time from inactivation of /CEf or /OE to high-impedance state output.

### Read Cycle Timing Chart (Flash Memory)



**Erase / Program Operations (Flash Memory)**

| Parameter | | Symbol | | MIN. | TYP. | MAX. | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | JEDEC | Standard | | | | | |
| Write cycle time | | $t_{AVAV}$ | $t_{WC}$ | 100 | | | ns | |
| Address setup time (/WE to address) | | $t_{AVWL}$ | $t_{AS}$ | 0 | | | ns | |
| Address setup time (/CEf to address) | | $t_{AVEL}$ | $t_{AS}$ | 0 | | | ns | |
| Address hold time (/WE to address) | | $t_{WLAX}$ | $t_{AH}$ | 50 | | | ns | |
| Address hold time (/CEf to address) | | $t_{ELAX}$ | $t_{AH}$ | 50 | | | ns | |
| Data setup time | | $t_{DVWH}$ | $t_{DS}$ | 50 | | | ns | |
| Data hold time | | $t_{WHDX}$ | $t_{DH}$ | 0 | | | ns | |
| /OE setup time | | – | $t_{OES}$ | 0 | | | ns | |
| /OE hold time | Read | – | $t_{OEH}$ | 0 | | | ns | |
| | Toggle and data polling | | | 10 | | | | |
| Read recover time before write (/OE to /CEf) | | $t_{GHEL}$ | $t_{GHEL}$ | 0 | | | ns | |
| Read recover time before write (/OE to /WE) | | $t_{GHWL}$ | $t_{GHWL}$ | 0 | | | ns | |
| /WE setup time (/CEf to /WE) | | $t_{WLEL}$ | $t_{WS}$ | 0 | | | ns | |
| /CEf setup time (/WE to /CEf) | | $t_{ELWL}$ | $t_{CS}$ | 0 | | | ns | |
| /WE hold time (/CEf to /WE) | | $t_{EHWH}$ | $t_{WH}$ | 0 | | | ns | |
| /CEf hold time (/WE to /CEf) | | $t_{WHEH}$ | $t_{CH}$ | 0 | | | ns | |
| Write pulse width | | $t_{WLWH}$ | $t_{WP}$ | 50 | | | ns | |
| /CEf pulse width | | $t_{ELEH}$ | $t_{CP}$ | 50 | | | ns | |
| Write pulse width high | | $t_{WHWL}$ | $t_{WPH}$ | 30 | | | ns | |
| /CEf pulse width high | | $t_{EHEL}$ | $t_{CPH}$ | 30 | | | ns | |
| Byte programming operation | | $t_{WHWH1}$ | $t_{WHWH1}$ | | 16 | | μs | |
| Sector erase operation | | $t_{WHWH2}$ | $t_{WHWH2}$ | | 1 | 15 | sec | 1 |
| $V_{CCf}$ setup time | | – | $t_{VCS}$ | 50 | | | μs | |
| Voltage transition time | | – | $t_{VLHT}$ | 4 | | | μs | 2 |
| Rise time to $V_{ID}$ | | – | $t_{VIDR}$ | 500 | | | ns | 2 |
| Recover time from RY (/BY) | | – | $t_{RB}$ | 0 | | | ns | |
| /RESET pulse width | | – | $t_{RP}$ | 500 | | | ns | |
| Delay time from embedded output enable | | – | $t_{EOE}$ | | | 100 | ns | |
| Program / Erase valid to RY (/BY) delay | | – | $t_{BUSY}$ | | | 90 | ns | |

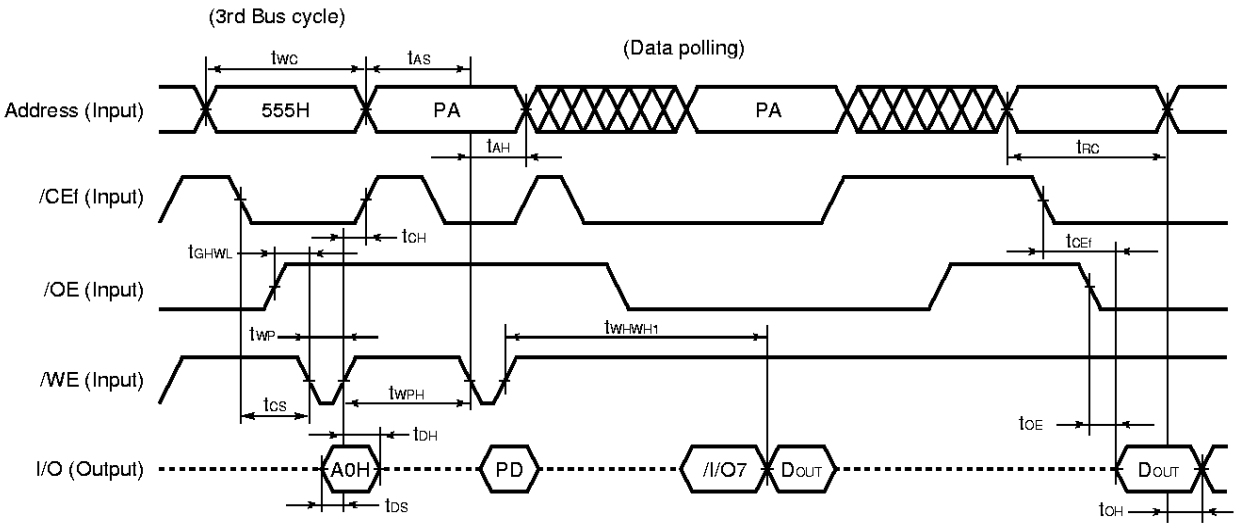
**Notes 1.** This does not include the preprogramming time.

**2.** For sector protect operation only.

**Erase / Program Performance (Flash Memory)**

| Parameter | Description | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Sector erase time | Excludes programming time prior to erasure | | 1 | 15 | sec |
| Byte programming time | Excludes system-level overhead | | 16 | 5,200 | μs |
| Chip programming time | Excludes system-level overhead | | 16.8 | 100 | sec |
| Erase / Program cycle | | 100,000 | | | cycles |

**Write Cycle Timing Chart (/WE Controlled) (Flash Memory)**




**Remarks 1.** This timing chart indicates last two bus cycles out of four bus cycles sequence.

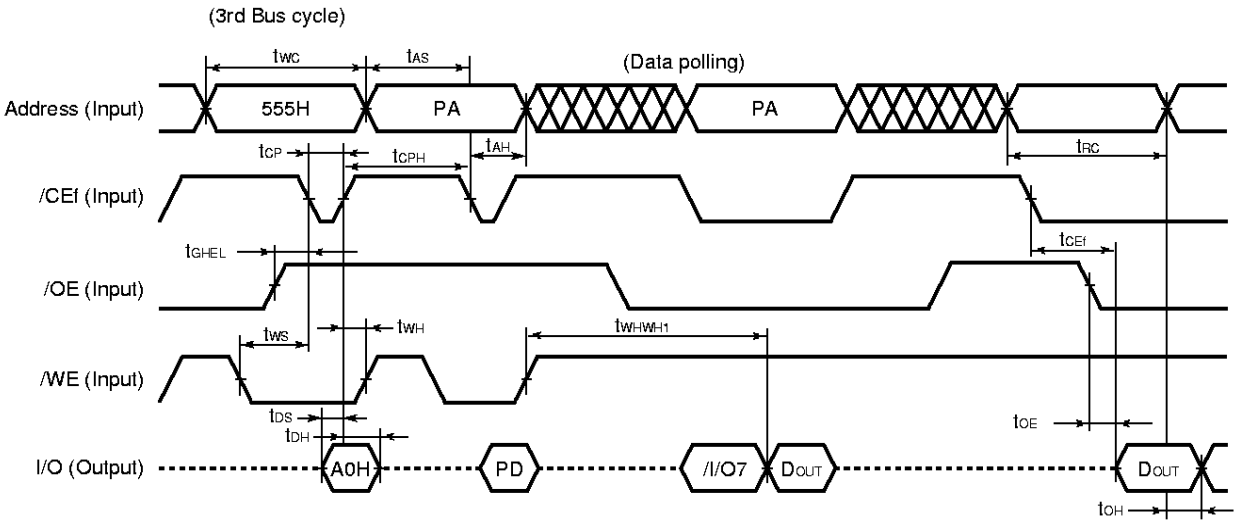
**2.** PA is address of the memory location to be programmed.

PD is data to be programmed at byte address.

/I/O7 is output of the complement of the data written to the device.

$D_{OUT}$ is output of the true data written to the device.

**Write Cycle Timing Chart (/CEf Controlled) (Flash Memory)**




**Remarks 1.** This timing chart indicates last two bus cycles out of four bus cycles sequence.

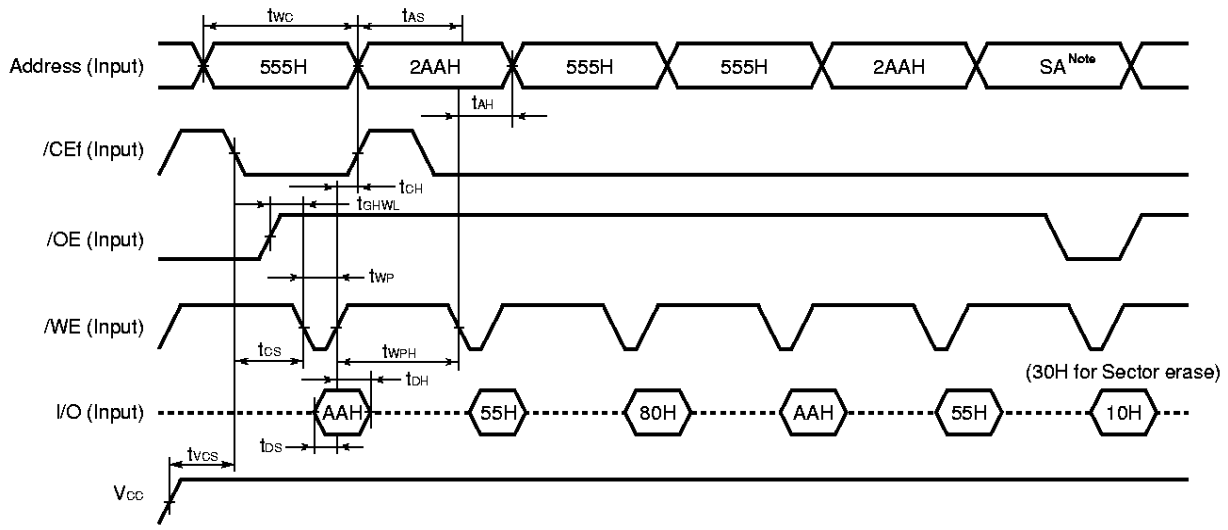
**2.** PA is address of the memory location to be programmed.

PD is data to be programmed at byte address.

/I/O7 is output of the complement of the data written to the device.

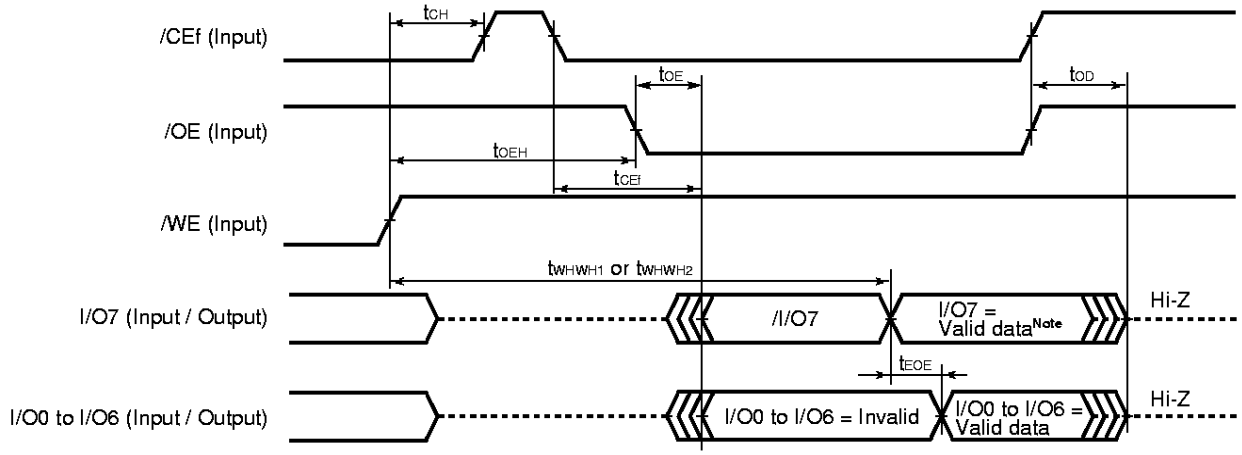
DOUT is output of the true data written to the device.

**Chip / Sector Erase Operation Timing Chart (Flash Memory)**



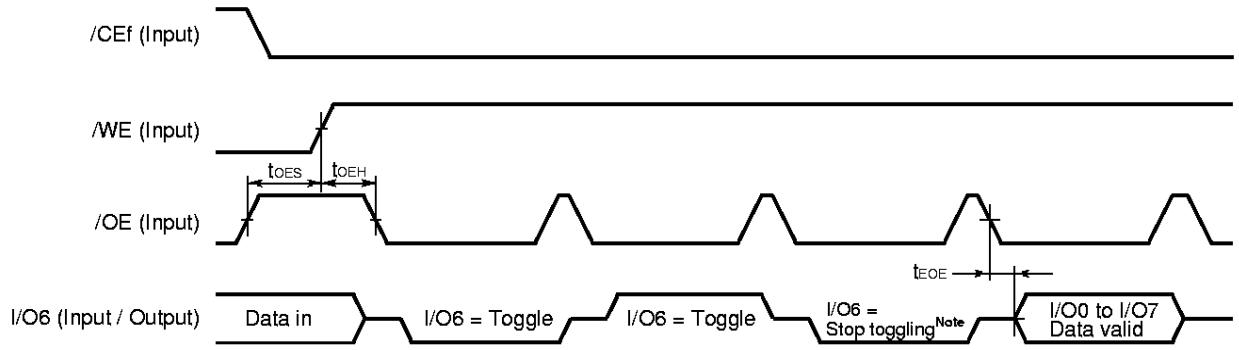

**Note** SA is the sector address for sector erase (see **Sector Address Table**). For chip erase, address = 555H.

**Data Polling during Automatic Program / Erase Operations Timing Chart (Flash Memory)**



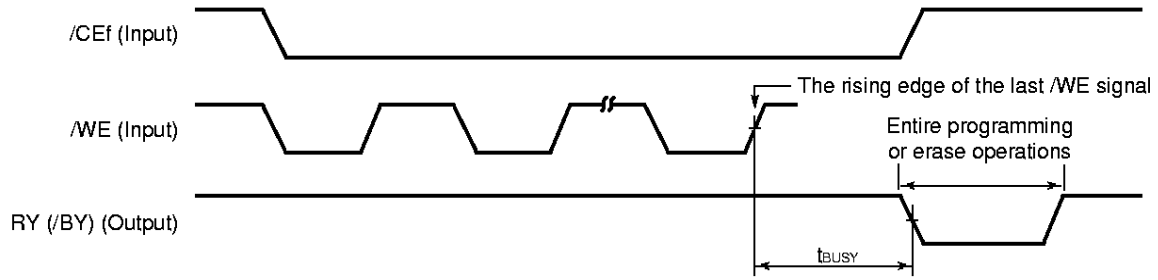

**Note** I/O7 = Valid data (the device has completed the automatic program / erase operation).

**Toggle Bit during Automatic Program / Erase Operations Timing Chart (Flash Memory)**

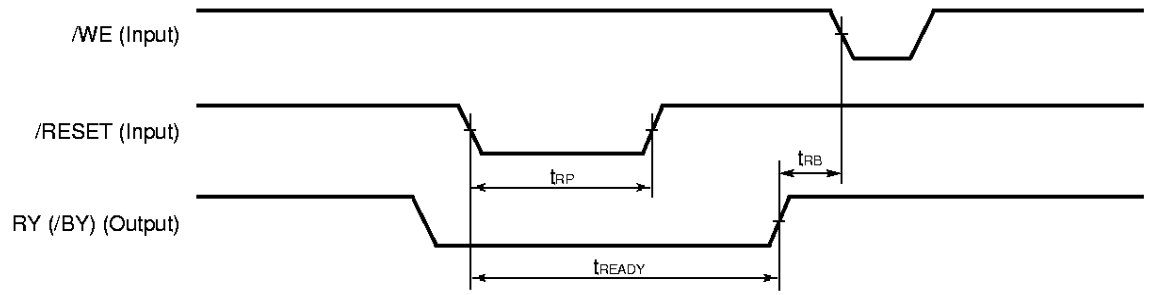



**Note** I/O6 = Stop toggling (the device has completed the automatic program / erase operation).

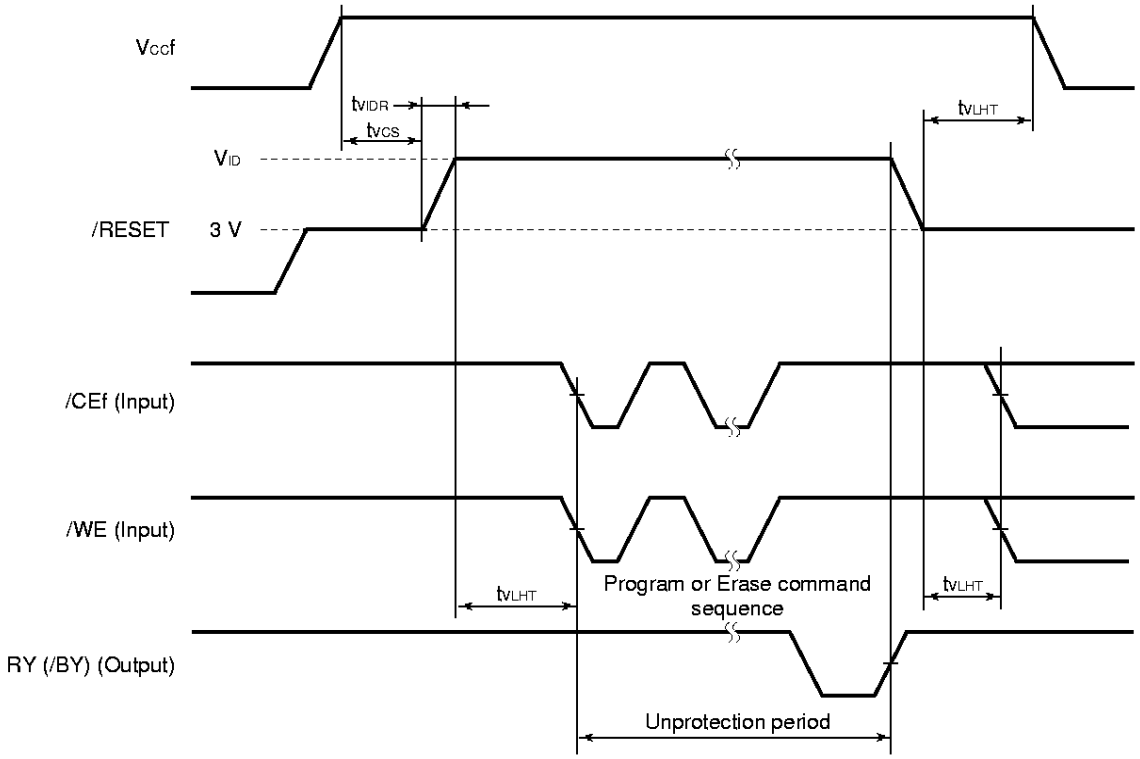
**RY (/BY) during Write / Erase Operations Timing Chart (Flash Memory)**



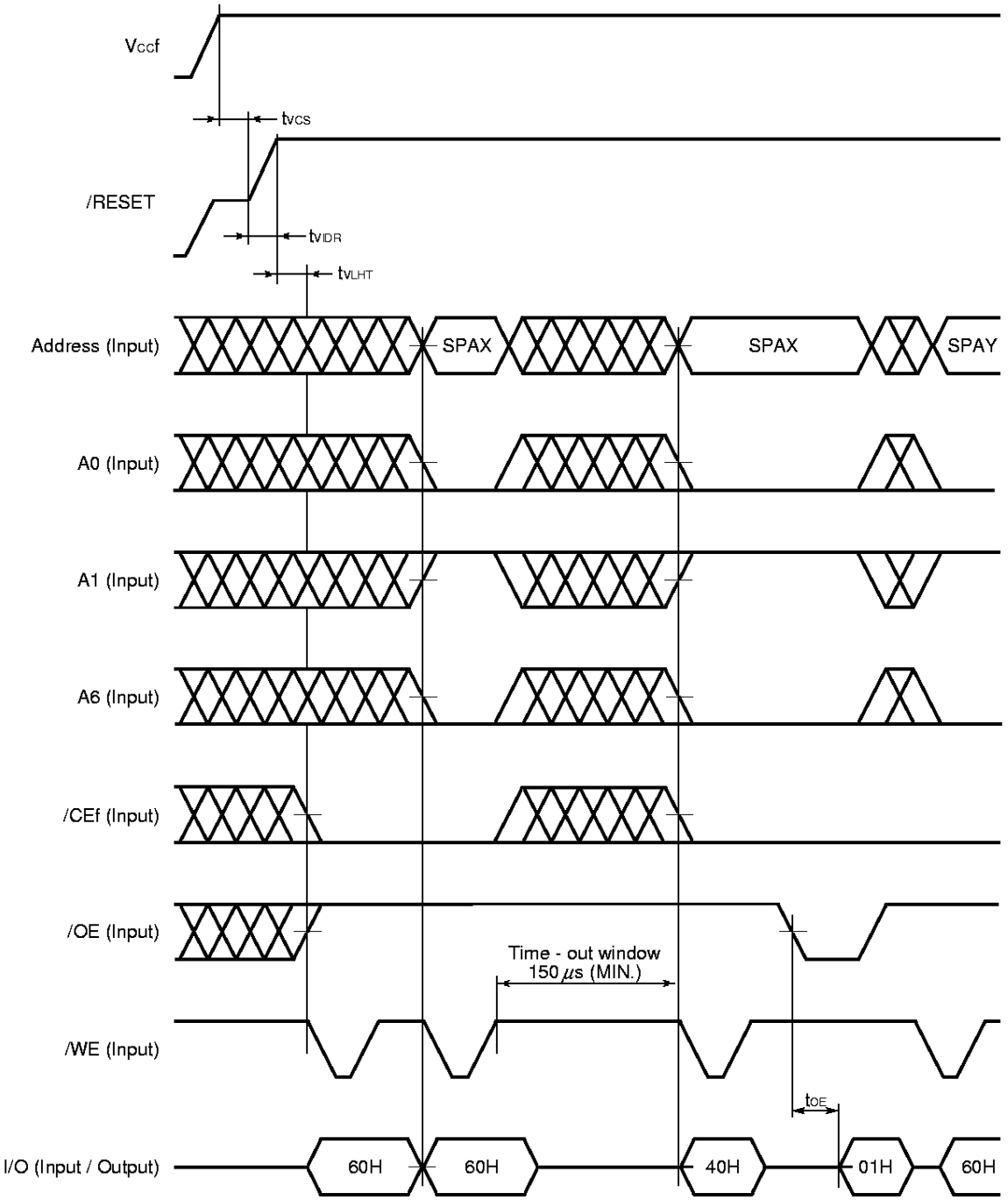

**/RESET, RY (/BY) Timing Chart (Flash Memory)**



**Temporary Sector Unprotect Timing Chart (Flash Memory)**



**Extended Sector Protect Timing Chart (Flash Memory)**



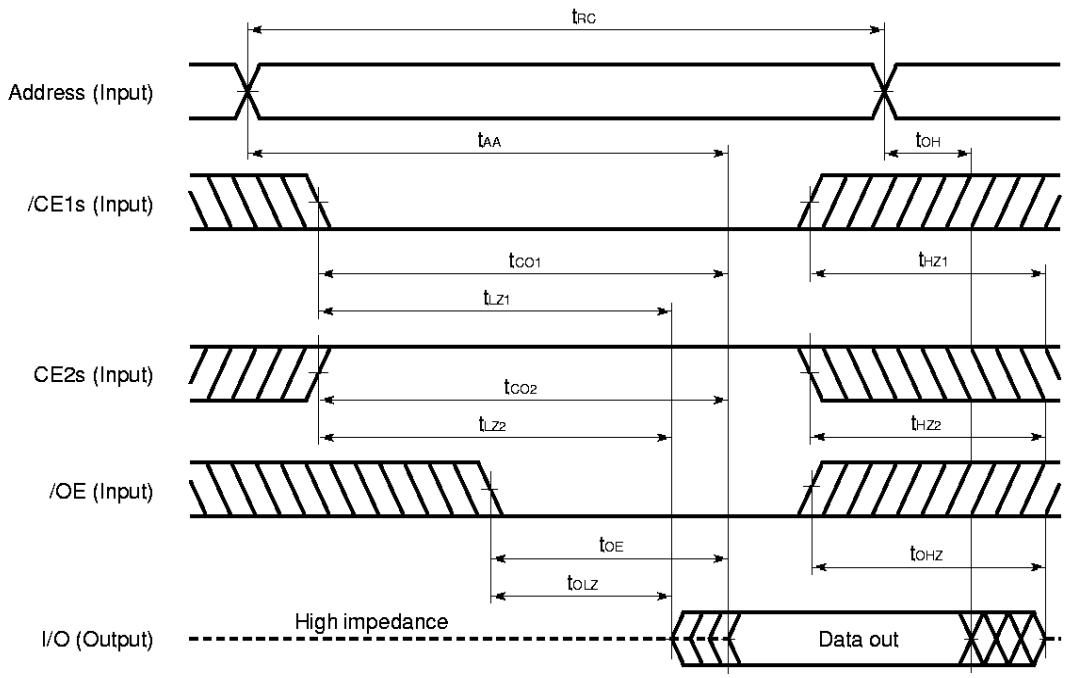

**Remark** SPAX is sector address to be protected.

SPAY is next sector address to be protected.

### Read Cycle (SRAM)

| Parameter | Symbol | MIN. | MAX. | Unit | Notes |
|---|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 100 | | ns | |
| Address access time | $t_{AA}$ | | 100 | ns | |
| /CE1s access time | $t_{CO1}$ | | 100 | ns | |
| CE2s access time | $t_{CO2}$ | | 100 | ns | |
| /OE to output valid | $t_{OE}$ | | 50 | ns | |
| Output hold from address change | $t_{OH}$ | 10 | | ns | |
| /CE1s to output in low impedance | $t_{LZ1}$ | 5 | | ns | |
| CE2s to output in low impedance | $t_{LZ2}$ | 5 | | ns | |
| /OE to output in low impedance | $t_{OLZ}$ | 0 | | ns | |
| /CE1s to output in high impedance | $t_{HZ1}$ | | 40 | ns | |
| CE2s to output in high impedance | $t_{HZ2}$ | | 40 | ns | |
| /OE to output hold in high impedance | $t_{OHZ}$ | | 40 | ns | |

### Read Cycle Timing Chart (SRAM)

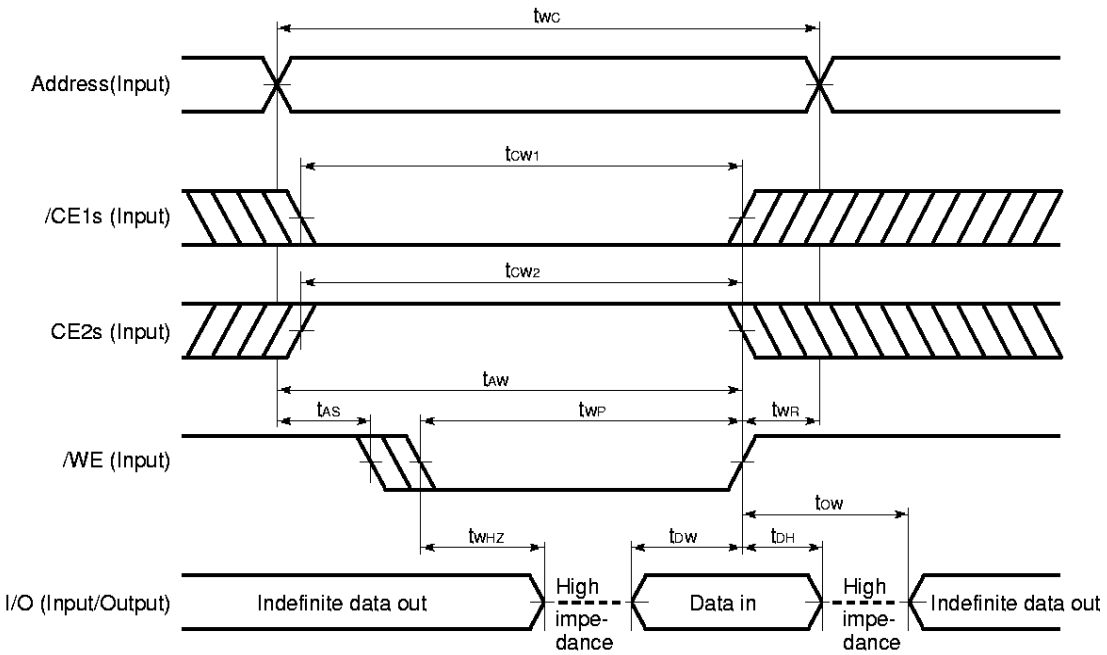



**Remark** In read cycle, /WE should be fixed to high level.

**Write Cycle (SRAM)**

| Parameter | Symbol | MIN. | MAX. | Unit | Notes |
|---|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 100 | | ns | |
| /CE1s to end of write | $t_{CW1}$ | 80 | | ns | |
| CE2s to end of write | $t_{CW2}$ | 80 | | ns | |
| Address valid to end of write | $t_{AW}$ | 80 | | ns | |
| Address setup time | $t_{AS}$ | 0 | | ns | |
| Write pulse width | $t_{WP}$ | 60 | | ns | |
| Write recovery time | $t_{WR}$ | 0 | | ns | |
| Data valid to end of write | $t_{DW}$ | 60 | | ns | |
| Data hold time | $t_{DH}$ | 0 | | ns | |
| /WE to output in high impedance | $t_{WHZ}$ | | 40 | ns | |
| Output active from end of write | $t_{OW}$ | 0 | | ns | |

**Write Cycle Timing Chart (/WE Controlled) (SRAM)**




**Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inacvtivated.**

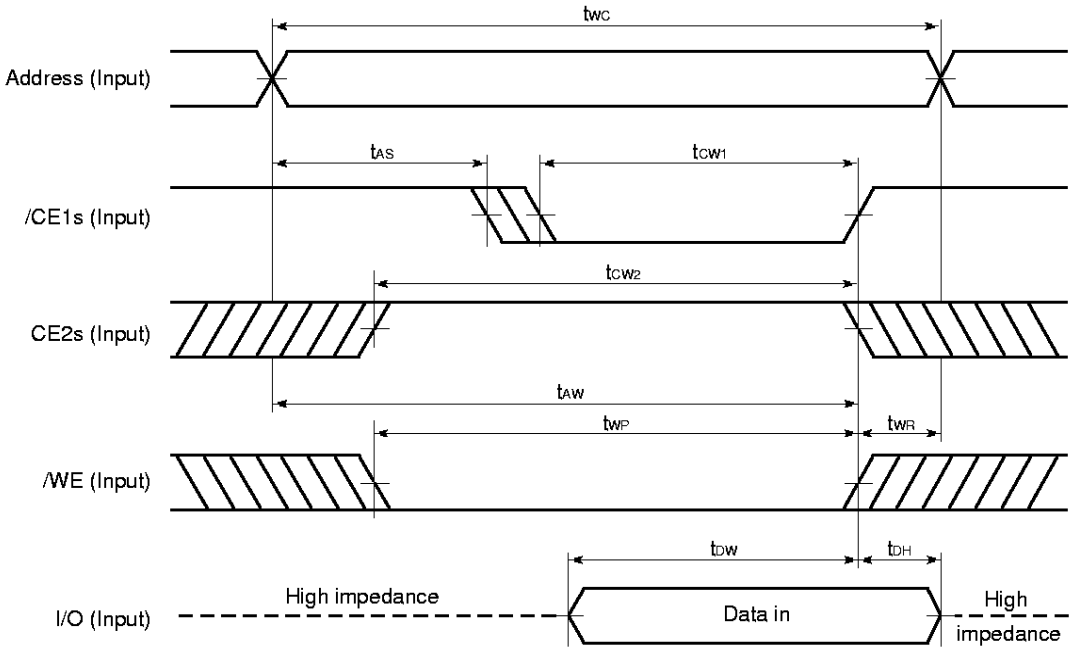
**2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.**

**Remarks 1.** Write operation is done during the overlap time of a low level /CE1s, WE, and a high level CE2s.

**2.** IF /CE1s changes to low level at the same time or after the change of /WE to low level, or if CE2s changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance time.

**3.** When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

**Write Cycle Timing Chart (/CE1s Controlled) (SRAM)**

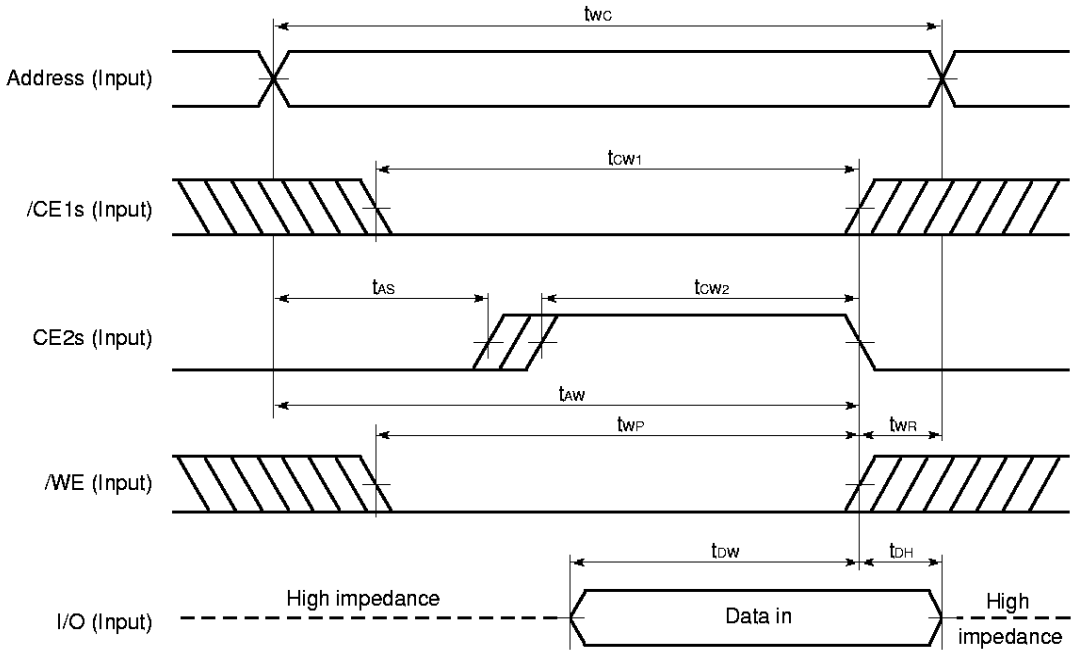



**Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inacvtivated.**

**2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.**

**Remark** Write operation is done during the overlap time of a low level /CE1s, WE, and a high level CE2s.

**Write Cycle Timing Chart (CE2s Controlled) (SRAM)**




**Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inacvtivated.**

**2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.**

**Remark** Write operation is done during the overlap time of a low level /CE1s, WE, and a high level CE2s.

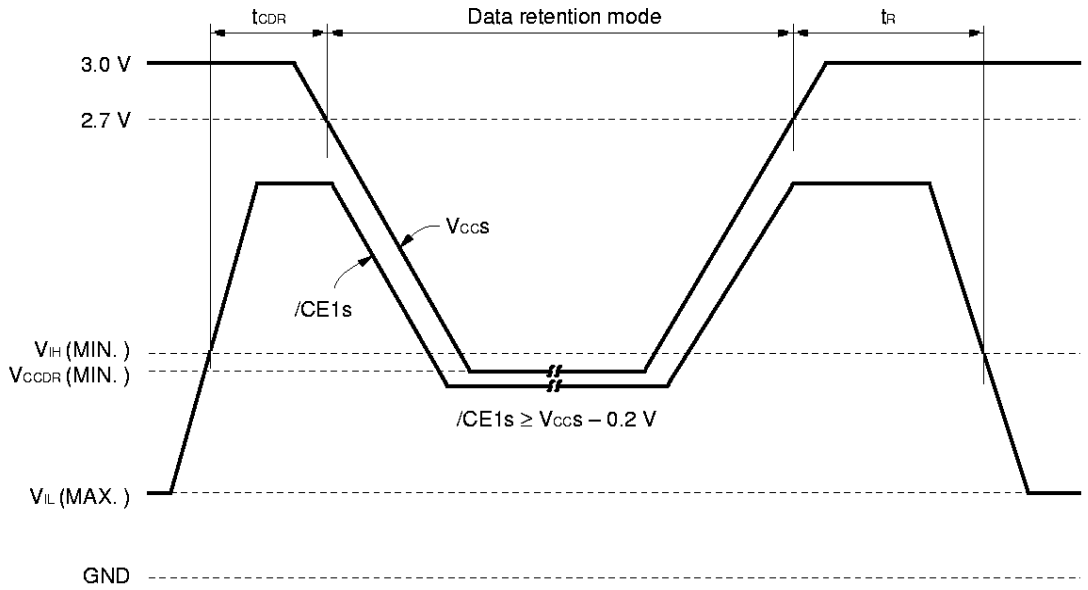
**Low $V_{CC}$ Data Retention Characteristics (SRAM)**

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{CCDR1}$ | /CE1s ≥ $V_{CCS}$ – 0.2 V, CE2s ≥ $V_{CCS}$ – 0.2 V | 2.0 | | 3.6 | V |
| | $V_{CCDR2}$ | CE2s ≤ 0.2 V | | | | |
| Data retention supply current | $I_{CCDR1}$ | $V_{CCS}$ = 3.0 V, /CE1s ≥ $V_{CCS}$ – 0.2 V, CE2s ≥ $V_{CCS}$ – 0.2 V or CE2s ≤ 0.2 V | | 0.5 | 20 Note | μA |
| | $I_{CCDR2}$ | $V_{CCS}$ = 3.0 V, CE2s ≤ 0.2 V | | 0.5 | 20 Note | μA |
| Chip deselection to data retention mode | $t_{CDR}$ | | 0 | | | ns |
| Operation recovery time | $t_R$ | | 5 | | | ms |

**Note** 3 μA (MAX.) ($T_A$ ≤ 40 °C), 1 μA (MAX.) ($T_A$ ≤ 25 °C)

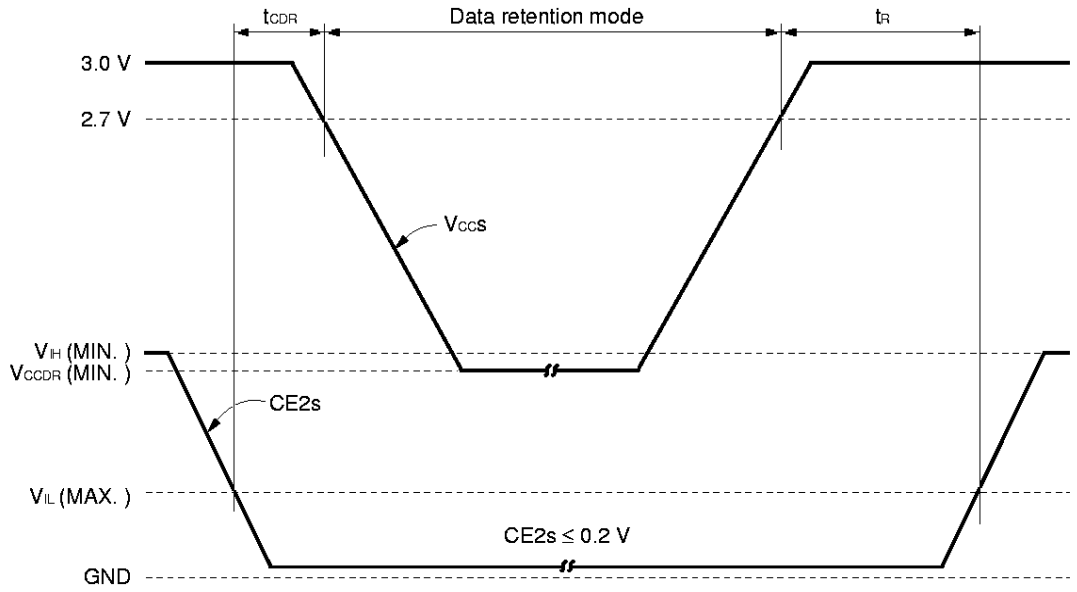
**Data Retention Timing Chart (SRAM)**

**(1) /CE1s Controlled**



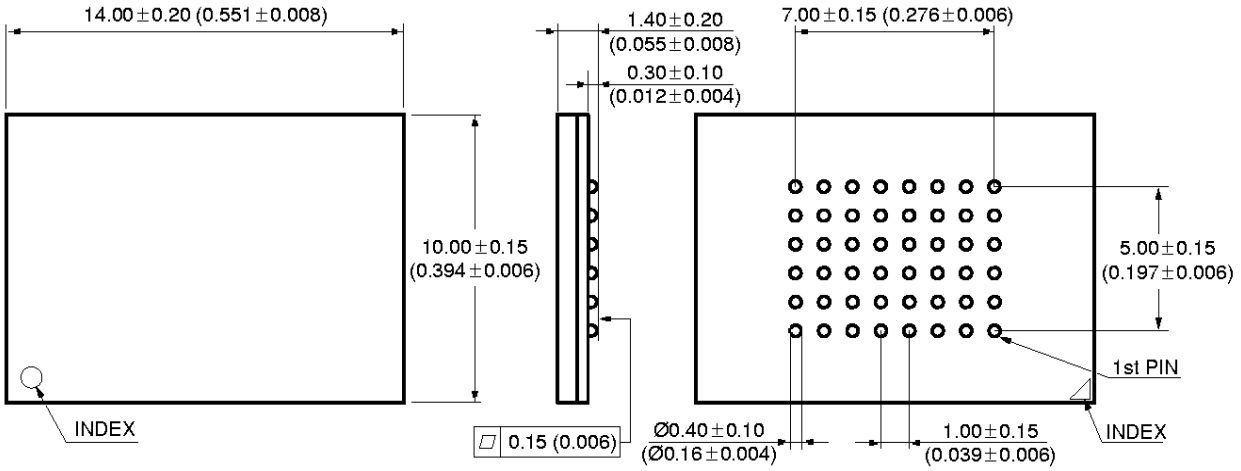

**Remark** On the data retention mode by controlling /CE1s, the input level of CE2s must be CE2s ≥ $V_{CCS}$ – 0.2 V or CE2s ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

**(2) CE2s Controlled**




**Remark** The other pins (/CE1s, Address, I/O, /WE, /OE) can be in high impedance state.

## Package Drawing




## Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the MC-22106.

### Type of Surface Mount Device

MC-22106F1-DE1-B10 : 48-pin plastic BGA (10 × 14 mm)

[ MEMO ]

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed imme-diately after power-on for devices having reset function.

**[MEMO]**



M4 96.5