The Future of Analog IC Technology

3A, 1.3V–6.0V DDR Memory Termination Regulator

DESCRIPTION

The MP2007 integrates the DDR memory termination regulator with the output voltage (VTT) and a buffered VTTREF outputs is a half of VREF.

The VTT-LDO is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost/low-external component count systems, where space is a premium.

The MP2007 maintains a fast transient response only requiring 20uF (2x10uF) of ceramic output capacitance. The MP2007 supports Kelvin sensing functions.

The MP2007 is available in the 8-pin MSOP with Exposed PAD package and is specified from −40°C to 85°C.

FEATURES

- VDDQ Voltage Range: 1.3V to 6.0 V
- Up to 3A Integrated Sink/Source Linear Regulator with Accurate VREF/2 Divider Reference for DDR Termination
- Requires Only 20uF Ceramic Output Capacitance
- Drive Voltage Range: 4.5 V to 5.5 V
- 1.3V Input (VDDQ) Helps Reduce Total Power Dissipation
- Integrated Divider Tracks VREF for VTT and VTTREF
- Kelvin Sensing (VTTSEN)
- ±20mV Accuracy for VTT and VTTREF
- Built-In Soft-Start, UVLO and OCL
- Thermal Shutdown

APPLICATIONS

- Notebook DDR2/3 Memory Supply and Termination Voltage in ACPI Compliant
- Active Termination Busses

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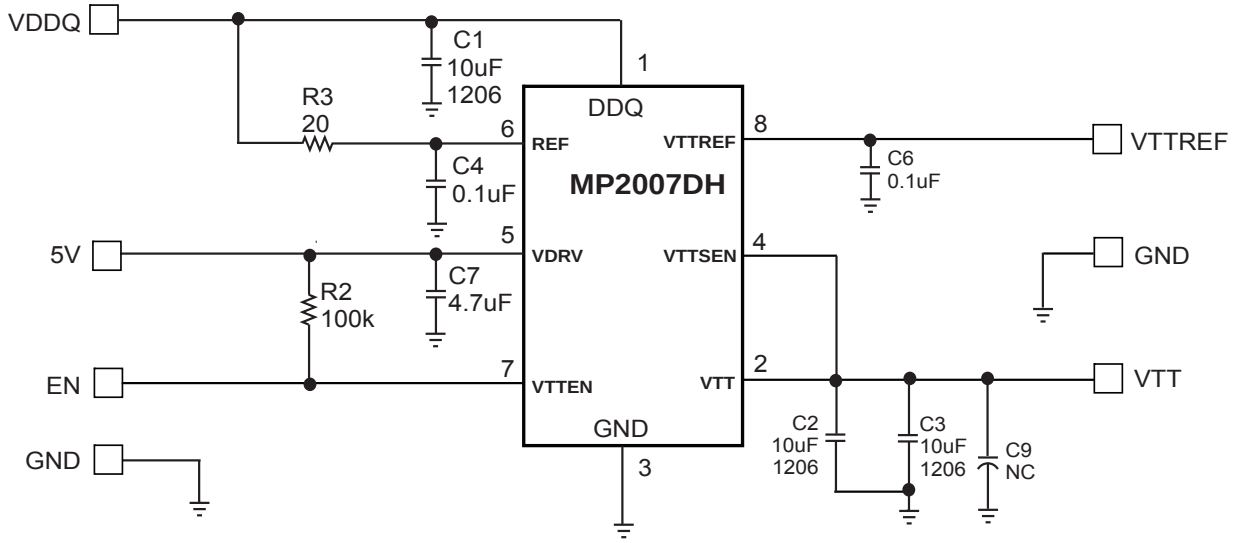
TYPICAL APPLICATION



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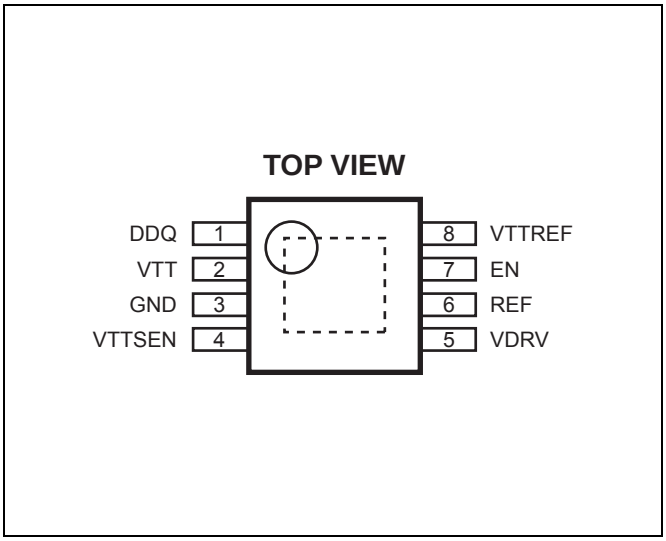
ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP2007DH	MSOP8E	2007D	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2007DH–Z); For RoHS Compliant Packaging, add suffix –LF (e.g. MP2007DH–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DDQ}..... -0.3V to 6.0V
Drive Voltage VDRV..... -0.3V to 6.0V
All Other Pins..... -0.3V to 6.0V
Continuous Power Dissipation (T_A = +25°C)(2) 1.56W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature ..... -50°C to +150°C

Recommended Operating Conditions (3)

Drive Voltage VDRV..... 4.5V to 5.5V
Operating Temperature .....–40°C to +85°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
MSOP8E.....	80.....	12... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{DRV} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Test Condition	Min	Typ	Max	Unit
VDRV Operating Voltage	VDRV	-	4.5	5.0	5.5	V
VDRV Shut down current	IDRV_SD	VDRV = 5.0 V, VDDQ=0V	-	0.2	1.0	μA
VDRV Operation Current	IDRV VEN_H,	VTT=0.75V		1.3	3	mA
VDRV UVLO Upper Threshold	VDRVUV+	Rising Edge	-	4.1	4.4	V
VDRV UVLO Hysteresis	VDRVUVHYS	-	-	0.35	-	V
Thermal Trip Point	TSD		- 150		-	°C
Hysteresis TSDHYS			- 25		-	°C
VDDQ UVLO Upper Threshold	VDDQUV+	Rising Edge; hysteresis = 55mV	-	0.9	1.3	V
VTT with Respect to 1/2VREF	dVTT0	1/2VREF – VTT, VREF = 1.8 V, IVTT = 0 to 3 A (Sink Current) IVTT = 0 to –3 A (Source Current)	-30 -	- -	- 30	mV
		1/2VREF – VTT, VREF = 1.5 V, IVTT = 0 to 3 A (Sink Current) IVTT = 0 to –3 A (Source Current)	-30 -	- -	- 30	mV
REF Input Resistance	REF_R	VREF = 1.8 V	40	55	75	kΩ
Source Current Limit	ILIMVTsrc	-	-	3.5	-	A
Sink Current Limit	ILIMVTsnk	-	-	3.5	-	A
Soft−Start Source Current Limit	ILIMVTSS	-	-	1.0	-	A
Maximum Soft−Start Time	tssvttmax	VREF=1.8V, VDRV=5V	-	9	-	us
		VREF=1.5V, VDRV=5V	-	7	-	
VTTREF Source Current	IVTTR	VREF = 1.8 V or 1.5 V	15	-	-	mA
VTTREF Accuracy Referred to 1/2VREF	dVTTR	1/2VREF – VTTR, VREF = 1.8 V, IVTTR = 0 mA to 15 mA	-18	-	18	mV
		1/2VREF – VTTR, VREF = 1.5 V, IVTTR = 0 mA to 15 mA	-15 -		15	mV
VEN Pin Threshold High	VEN_H	-	1.4	-	-	V
VEN Pin Threshold Low	VEN_L	-	-	-	0.5	V
VEN Pin Input Current	IIN_VEN	VEN = 5.0 V	-	-	1.0	μA

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PIN FUNCTIONS

Pin #	Name	Description
1	DDQ	Power input for VTT regulator. Connect to GND through 10uF ceramic capacitor. It is normally connected to the VDDQ of DDR memory rail.
2	VTT	Power output for the VTT LDO.
3	GND Exposed Pad	The exposed pad and GND pin must be connected to the same ground plane.
4	VTTSEN	Kelvin sensed feedback signal.
5	VDRV	Chip bias Voltage.
6	REF	LDO signal input for generating VDDQ/2 reference.
7	EN	VTT regulator enable input. High to enable the chip.
8	VTTREF	Buffered output for the system. The receiving end of the DDR memory cells needs this signal for their input comparator.

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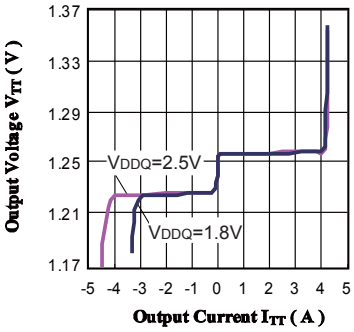
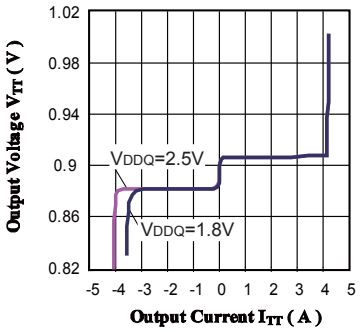
TYPICAL PERFORMANCE CHARACTERISTICS

C1=C2=C3=10uF, C4 =C6=0.1uF, C7=4.7uF, V_{DRV}=5V, T_A=25ºC unless otherwise noted.

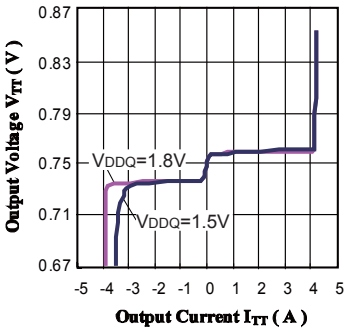
DDR Regulation



DDR2 Regulation

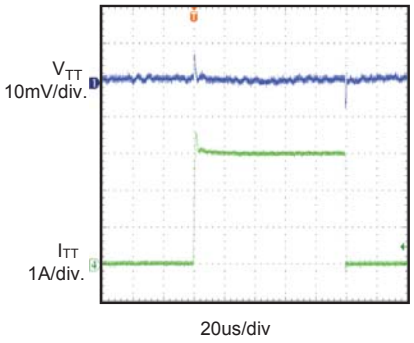


DDR3 Regulation



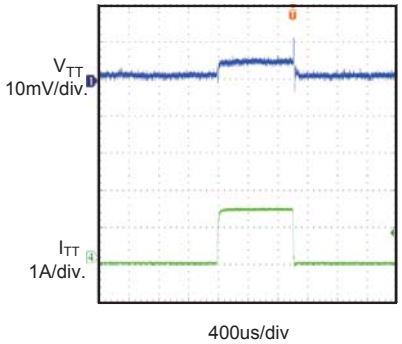
Source Load Transient

V_{DDQ}=V_{REF}=1.8V, V_{TT}=0.9V



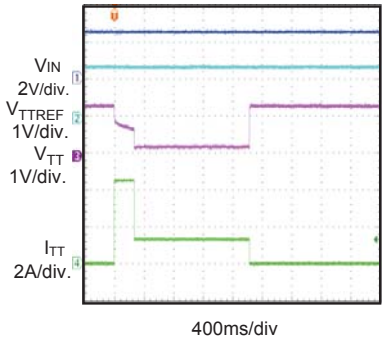
Sink Load Transient

V_{DDQ}=V_{REF}=2.5V, V_{TT}=0.9V, V_{SINK}=1.8V



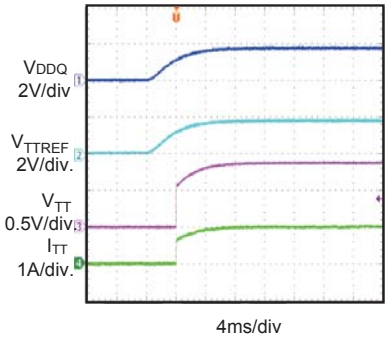
Source Over Current Protection

V_{DDQ}=V_{REF}=2.5V, V_{TT}=1.25V



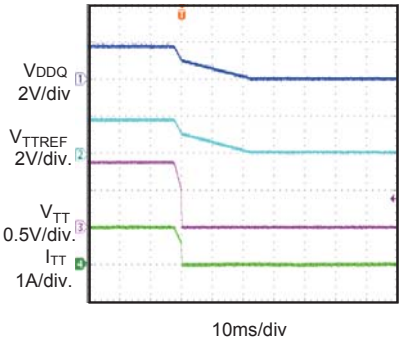
Power Ramp Up

V_{DDQ}=V_{REF}=1.8V, V_{TT}=0.9V



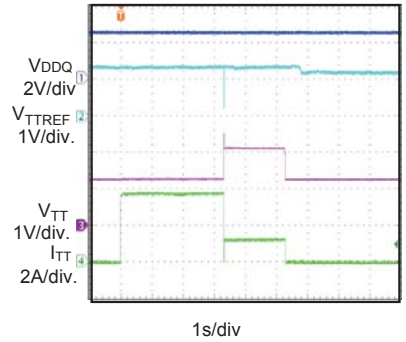
Startup Through Down

V_{DDQ}=V_{REF}=1.8V, V_{TT}=0.9V



Sink Over Current Protection

V_{DDQ}=V_{REF}=2.5V, V_{TT}=1.25V,V_{SINK}=2.5V



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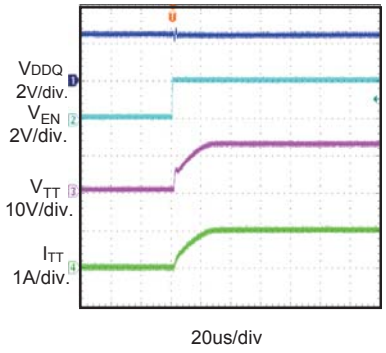
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C1=C2=C3=10uF, C4 =C6=0.1uF, C7=4.7uF, V_{DRV}=5V, T_A=25ºC unless otherwise noted.

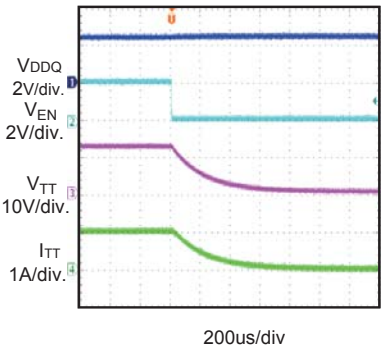
Enable On

V_{DDQ}=V_{REF}=2.5V, V_{TT}=1.25V



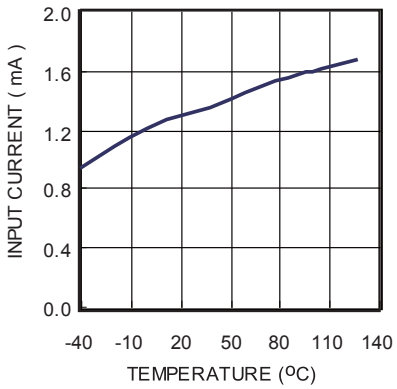
Enable Off

V_{DDQ}=V_{REF}=2.5V, V_{TT}=1.25V



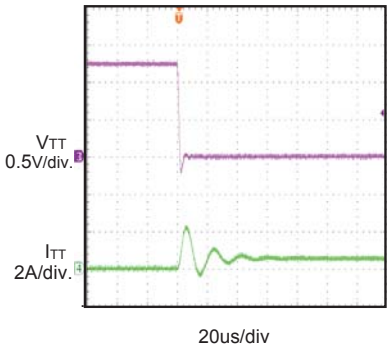
Input Supply Current vs. Temp

V_{DDQ}=V_{REF}=1.8V, V_{TT}=0.9V



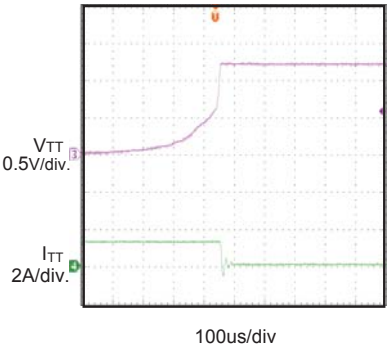
Short Circuit

V_{DDQ}=V_{REF}=2.5V, V_{TT}=1.25V



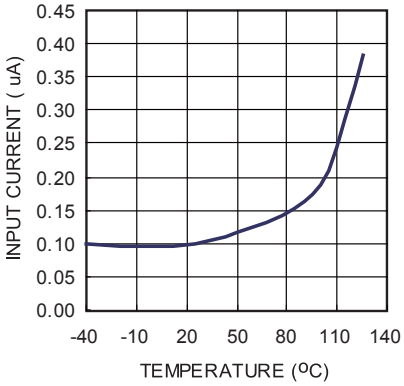
Short Circuit Recovery

V_{DDQ}=V_{REF}=2.5V, V_{TT}=1.25V



Shut Down Input Current vs. Temp

V_{DDQ}=V_{REF}=.8V, V_{TT}=0V



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DETAILED OPERATING DESCRIPTION

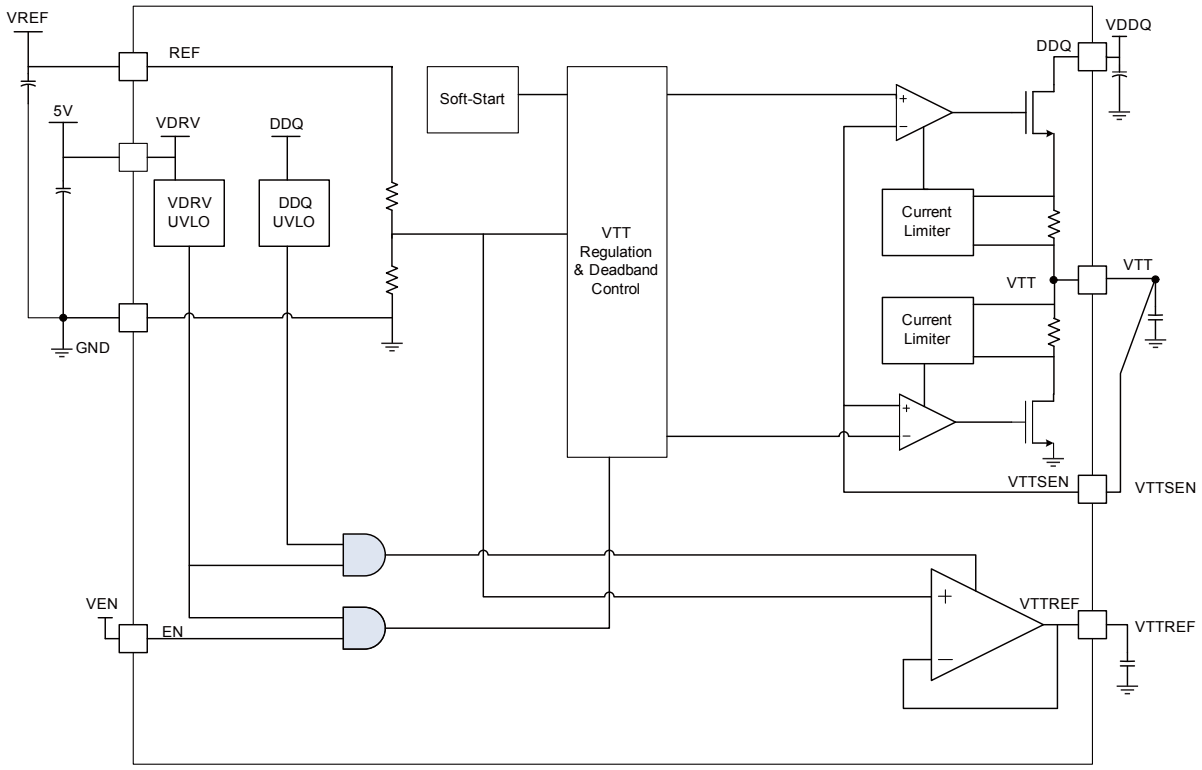

Figure 1—Functional Block Diagram

Control Logic

The internal control logic is powered by VDRV. The IC is enabled whenever both VDDQ UVLO and VDRV UVLO are pulled low. VTTREF output begins to track VREF/2. When the VTTEN pin is high, the VTT regulator is activated.

VTTREF Output

The VTTREF output tracks VREF/2 with ±2% accuracy. It has source current capability of up to 15 mA. VTTREF should be bypassed to analog ground of the device by 1.0 μF ceramic capacitor for stable operation.

The VTTREF is turned on as long as both VDDQ and VDRV are higher the UVLO threshold.

VTTREF features a soft-start and tracks VREF/2.

Output Voltages Sensing

The VTT output voltage is sensed across the VTTSEN and GND pins. The VTTSEN should be connected to the VTT regulation point, which is usually the VTT local bypass capacitor, via a direct sense trace. The GND should be connected via a direct sense trace to the ground of the VTT local bypass capacitor for load.

VDDQ UVLO Protection

For VDDQ undervoltage lockout (UVLO) protection, the MP2007 monitors VDDQ voltage. When the VDDQ voltage is lower than UVLO threshold voltage, the VTT regulator is shut off.

Current Protection of VTT Active Terminator

To provide protection for the internal FETs, over current limit(OCL) of 3A is implemented.

The LDO has a constant overcurrent limit (OCL) at 3.5 A. This trip point is reduced to 1.0 A if the output voltage drops below 1/3 of the target voltage.

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Thermal Consideration of VTT Active Terminator

The VTT terminator is designed to handle large transient output currents. If large currents are required for very long duration, then care should be taken to ensure the maximum junction temperature is not exceeded. The 8-pin MSOP with ExposedPAD has a thermal resistance of 50°C/W (dependent on air flow, and PCB design).

In order to take full advantage of the thermal capability of this package, the exposed pad should be soldered directly onto the PCB ground layer to allow good thermal contact. It is recommended that the PCB should have 10 to 15 vias with 0.3mm drill size underneath the exposed thermal pad connecting all the ground layers

Supply Voltage Undervoltage Monitor

The IC continuously monitors VDRV. If VDRV is set higher than its preset threshold and VTTEN is high too, the IC will start up.

Thermal Shutdown

When the chip junction temperature exceeds **150°C**, the entire IC is shutdown. The IC resumes normal operation only after the junction temperature dropping below **125°C**.

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APPLICATION INFORMATION

Input Capacitor

Depending on the trace impedance from the power supply to the part, transient increase of source current is supplied mostly by the charge from the VDDQ input capacitor. Use a 10 µF (or more) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT. In general, use 1/2 COUT for input.

Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal or greater than 20µF. Attach two 10 µF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If the ESR is greater than 10mΩ, insert an R-C filter between the output and the VTTSEN input to achieve loop stability. The R-C filter time constant should be almost the same or slightly lower than the time constant of the output capacitor and its ESR.

VDRV Capacitor

Add a ceramic capacitor with a value between 1.0µF and 4.7 µF placed close to the VDRV pin, to stabilize 5V from any parasitic impedance from the supply.

Thermal design

As the MP2007 is a linear regulator, the VTT current flow in both source and sink direction generate power dissipation from the device.
In the source phase, the potential difference between VDDQ and VTT times VTT current becomes the power dissipation,
Psource=(VDDQ-VTT) x Isource

In this case, if VDDQ is connected to an alternative power supply lower than VDDQ voltage, power loss can be decreased.

For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation Psink is:

Psink=VTT x Isink

The device does not sink and source the current at the same time and source/sink current varies rapidly with time. The actual power dissipation to be considered for thermal design is an average of the above values over time.

Another power consumption is the current used for internal control circuitry from VDDQ supply. This power needs to be effectively dissipated from the package.

PCB Layout Guidelines

Good PCB layout design is critical to ensure high performance and stable operation of the DDR power controller. The following items must be considered when preparing PCB layout:

1. All high−current traces must be kept as short and wide as possible to reduce power loss.

High−current traces are the trace from the input voltage terminal to VDDQ pin, the trace from the VTT output terminal to the load, the trace from the input ground terminal to the VTT output ground terminal, and the trace from VTT output ground terminal to the GND pin.

Power handling and heaksinking of high−current traces can be improved by also routing the same high−current traces in the other layers by the same path and joining them together with multiple vias.

2. To ensure the proper function of the device, separated ground connections should be used for different parts of the application circuit according to their functions.

The VTT output capacitor ground should be connected to the GND pin first with a short trace, it is then connected to the ground plane of GND. The input capacitor ground, the VTT output capacitor ground, the VDDQ decoupling capacitor ground should be connected to the GND plane.

3. The thermal pad of the 8-pin MSOP package should to be connected to GND for better thermal performance. It is recommended to use a PCB with 1 oz or 2oz copper foil.

4. A separate sense trace should be used to connect the VTT point of regulation, which is usually the local bypass capacitor for load, to the VTTSEN pin.

5. Separate sense trace should be used to connect the VREF point of regulation to the VTTREF pin to ensure the accuracy of the reference voltage to VTT.

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6. VDDQ should be connected to VREF Input with wide and short trace if VDDQ is used as the sourcing supply for VTT. An input capacitor of at least 10μF should be added close to the VDDQ pin and bypassed to GND if external voltage supply is used as the VTT sourcing supply.

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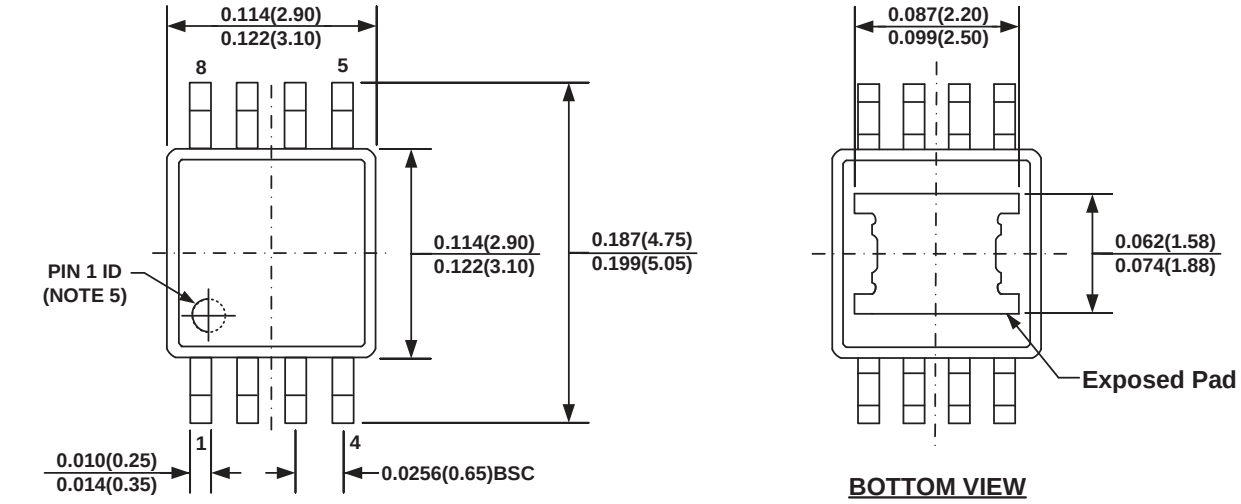
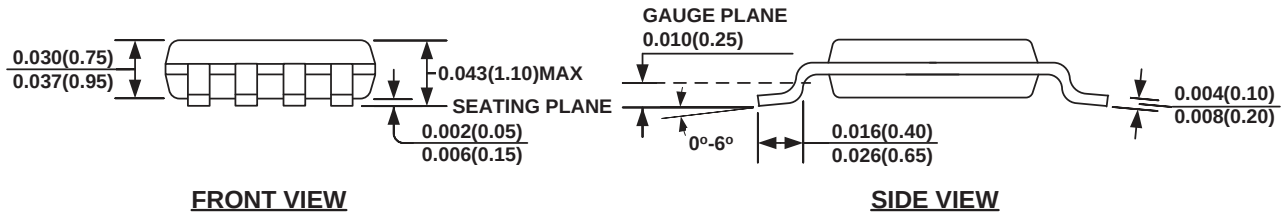
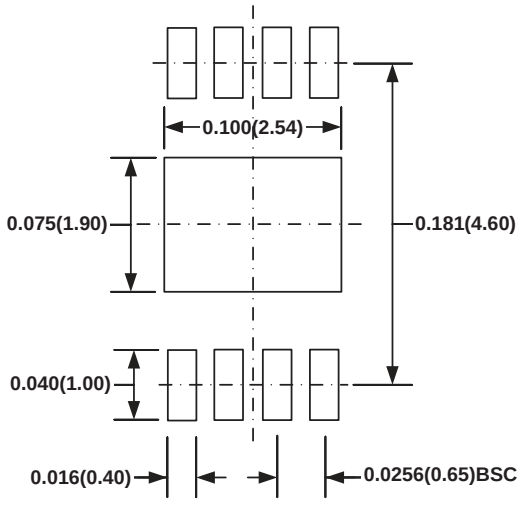
PACKAGE INFORMATION

MSOP8E (EXPOSED PAD)







NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
7) DRAWING IS NOT TO SCALE.

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