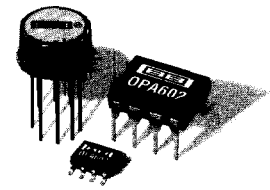
BURR - BROWN®



OPA602

www.burr-brown.com/databook/OPA602.html

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/µs
- LOW OFFSET: ±250µV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING TIME: 1µs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

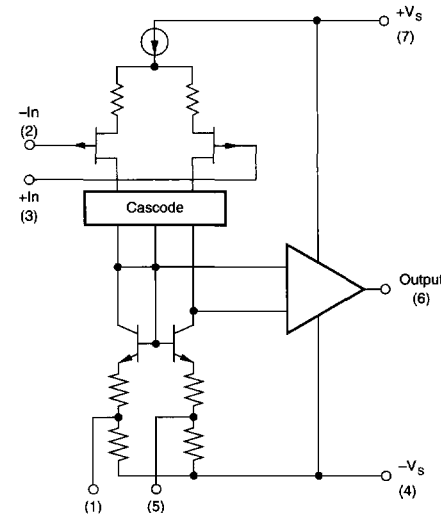
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic ***Difet*** (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. ***Difet*** construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_S = ±15VDC and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM, AP, AU			OPA602BM, SM, BP			OPA602CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage: f_O = 10Hz			*			23			*		nV/√Hz
f_O = 100Hz			*			19			*		nV/√Hz
f_O = 1kHz			*			13			*		nV/√Hz
f_O = 10kHz			*			12			*		nV/√Hz
f_B = 10Hz to 10kHz			*			1.4			*		µVrms
f_B = 0.1Hz to 10Hz			*			0.95			*		µVp-p
Current: f_B = 0.1Hz to 10Hz			*			12			*		fAp-p
f_O = 0.1Hz to 20kHz			*			0.6			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage:											
M Package	V_{CM} = 0VDC		±300	±1000		±150	±500		±100	±250	µV
P Package			1	2		0.5	1				mV
U Package			1	3							mV
Over Specified Temperature											
M Package			±550			±250	±1000		±200	±500	µV
P, U Packages			±1.5			±0.75	±1.5				mV
Average Drift	T_A = T_{MIN} to T_{MAX}		*	±15		±3	±5		*	±2	µV/°C
Supply Rejection	±V_S = 12V to 18V	70	*		80	100		86	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±2	±10		±1	±2		±0.5	±1	pA
Over Specified Temperature			±20	±500		±20	±200		±10	±100	pA
SM Grade						±200	±2000				pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		1	10		0.5	2		0.5	1	pA
Over Specified Temperature			20	500		20	200		10	100	pA
SM Grade						200	1000				pA
INPUT IMPEDANCE											
Differential			*			10^{13} || 1			*		Ω || pF
Common-Mode			*			10^{14} || 3			*		Ω || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		*	*		±10.2	+13, −11		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	75	*		88	100		92	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 1kΩ	75	*		88	100		92	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	3.5	*		4	6.5		5	*		MHz
Full Power Response	20Vp-p, R_L = 1kΩ		*			570			*		kHz
Slew Rate	V_O = ±10V, R_L = 1kΩ	20	*		24	35		28	*		V/µs
Settling Time: 0.1%	Gain = −1, R_L = 1kΩ		*			0.6			*		µs
0.01%	C_L = 500pF, 10V Step		*			1.0			*		µs
RATED OUTPUT											
Voltage Output	R_L = 1kΩ	±11	*		±11.5	+12.9, −13.8		*	*		V
Current Output	V_O = ±10VDC	*	*		±15	±20		*	*		mA
Output Resistance	1MHz, Open Loop		*			80			*		Ω
Load Capacitance Stability	Gain = +1		*			1500			*		pF
Short Circuit Current		±25	*		±30	±50		*	*		mA
POWER SUPPLY											
Rated Voltage			*			±15			*		VDC
Voltage Range,											
Derated Performance		*		*	±5		±18	*		*	VDC
Current, Quiescent	I_O = 0mADC		*	*		3	4		*	*	mA
Over Specified Temperature			*	*		3.5	4.5		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	*		*	−25		+85	*		*	°C
SM Grade					−55		+125				°C
Operating: M Package	Ambient Temperature	*		*	−55		+125	*		*	°C
P, U Packages		−25		+85	−25		+85				°C
Storage: M Package	Ambient Temperature	*		*	−65		+150	*		*	°C
P, U Packages		−40		+125	−40		+125				°C
θ_{JA}			*			200			*		°C/W

* Same specifications as OPA602BM.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	
M Package	–65°C to +150°C
P and U Packages	–40°C to +125°C
Operating Temperature Range	
M Package	–55°C to +125°C
P and U Packages	–25°C to + 85°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its

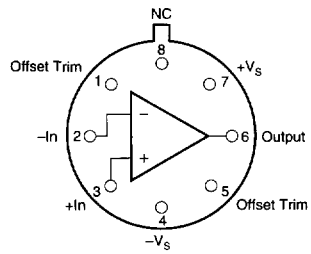
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (µV) AT 25°C
OPA602AM	TO-99	001	–25°C to +85°C	±1000
OPA602BM	TO-99	001	–25°C to +85°C	±500
OPA602CM	TO-99	001	–25°C to +85°C	±250
OPA602SM	TO-99	001	–55°C to +125°C	±500
OPA602AP	Plastic DIP	006	–25°C to +85°C	±2000
OPA602BP	Plastic DIP	006	–25°C to +85°C	±1000
OPA602AU	Plastic SOIC	182	–25°C to +85°C	±3000

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

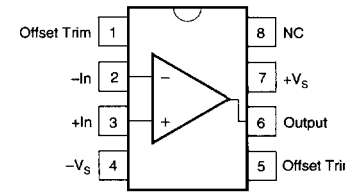
PIN CONFIGURATIONS

Top View — TO-99



Case Connected to $+V_S$.

Top View — DIP



Top View — SOIC