NEC

MOS INTEGRATED CIRCUIT

μPD780001

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780001 is a product of the 78K/0 Series of microcontrollers, and features internal 8-bit resolution A/D converters, timers, serial interface units, interrupt controllers, and many other incorporated peripheral hardware.

A one-time PROM or EPROM version (μPD78P018F) and various development tools for the μPD780001 are available. The μPD78P018F is capable of operating in the same power supply voltage range as the μPD780001.

Functions are described in detail in the following User's Manuals. They should be read before starting design.

μPD780001 User's Manual : In preparation
78K/0 Series User's Manual—Instruction : IEU-1372

FEATURES

- Internal ROM and RAM
  - Internal ROM : 8 Kbytes
  - Internal high-speed RAM : 192 bytes
- Two types of packages are provided:
  - 64-pin plastic shrink DIP (750 mil)
  - 64-pin plastic QFP (14 × 14 mm)
- Instruction execution time can be varied from high-speed (0.4 μs) to low-speed (6.4 μs)
- I/O ports : 39
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 1 channel
  - 3-wire serial I/O mode : 1 channel
- Timer : 3 channels
- Supply voltage : V_{DD} = 2.7 to 5.5 V

APPLICATIONS

Telephones, VCRs, audio equipment, cameras, air conditioners, home appliances, pagers, etc.

ORDERING INFORMATION

Part Number	Package
μPD780001CW-xxx	64-pin plastic shrink DIP (750 mil)
μPD780001GC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)

Remark xxx indicates ROM code suffix.

The information in this document is subject to change without notice.

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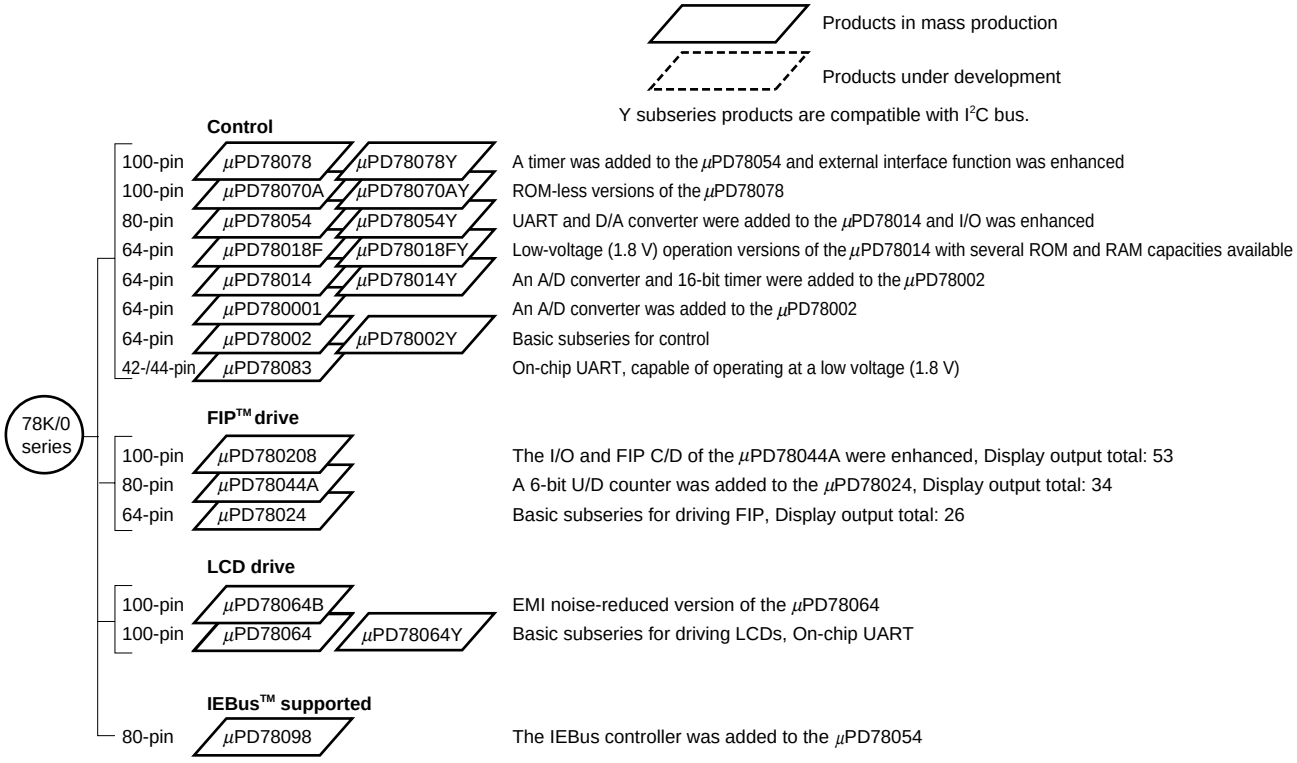
The mark ✱ shows major revised points.

✱ 78K/0 Series Development

The following shows the 78K/0 series products development. Subseries names are shown inside frames.



The following table shows the differences among subseries functions.

Part Number \ Function		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78078	32 K-60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	Available
	μPD78070A	–								61	2.7 V	
	μPD78054	16 K-60 K	2ch							69	2.0 V	
	μPD78018F	8 K-60 K						–	2ch	53	1.8 V	
	μPD78014	8 K-32 K									2.7 V	
	μPD780001	8 K		–	–				1ch	39		Not available
	μPD78002	8 K-16 K			1ch		–			53		Available
	μPD78083				–		8ch		1ch (UART: 1ch)	33	1.8 V	Not available
FIP drive	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	74	2.7 V	Not available
	μPD78044A	16 K-40 K								68		
	μPD78024	24 K-32 K								54		
LCD drive	μPD78064B	32 K	2ch	1ch	1ch	1ch	8ch	–	2ch (UART: 1ch)	57	2.0 V	Not available
	μPD78064	16 K-32 K										
IEBus supported	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	Available

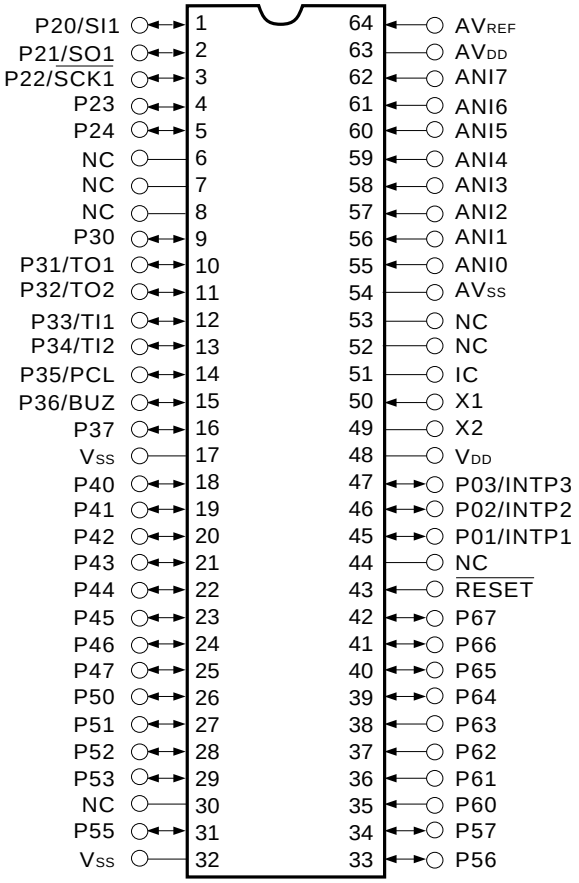
FUNCTION DESCRIPTION

Item		Function
Internal memory	ROM	8 Kbytes
	Internal high-speed RAM	192 bytes
Memory space		64 Kbytes
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycles		Instruction execution time variable function is integrated. 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 10.0 MHz operation with main system clock)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total : 39 • CMOS input : 4 • CMOS input/output : 35
A/D converter		• 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: V_{DD} = 2.7 to 5.5 V
Serial interface		3-wire serial I/O mode: 1 channel
Timer		• 8-bit timer/event counter: 2 channels • Watchdog timer: 1 channel
Timer output		2
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (@ 10.0 MHz operation with main system clock)
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (@ 10.0 MHz operation with main system clock)
Vectored interrupts	Maskable interrupts	Internal: 5, External: 3
	Non-Maskable interrupt	Internal: 1
	Software interrupt	Internal: 1
Test input		External: 1
Supply voltage		V_{DD} = 2.7 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm)

CONTENTS

1. PIN CONFIGURATION (Top View)

- **64-Pin Plastic Shrink DIP (750 mil)**
  μPD780001CW-xxx



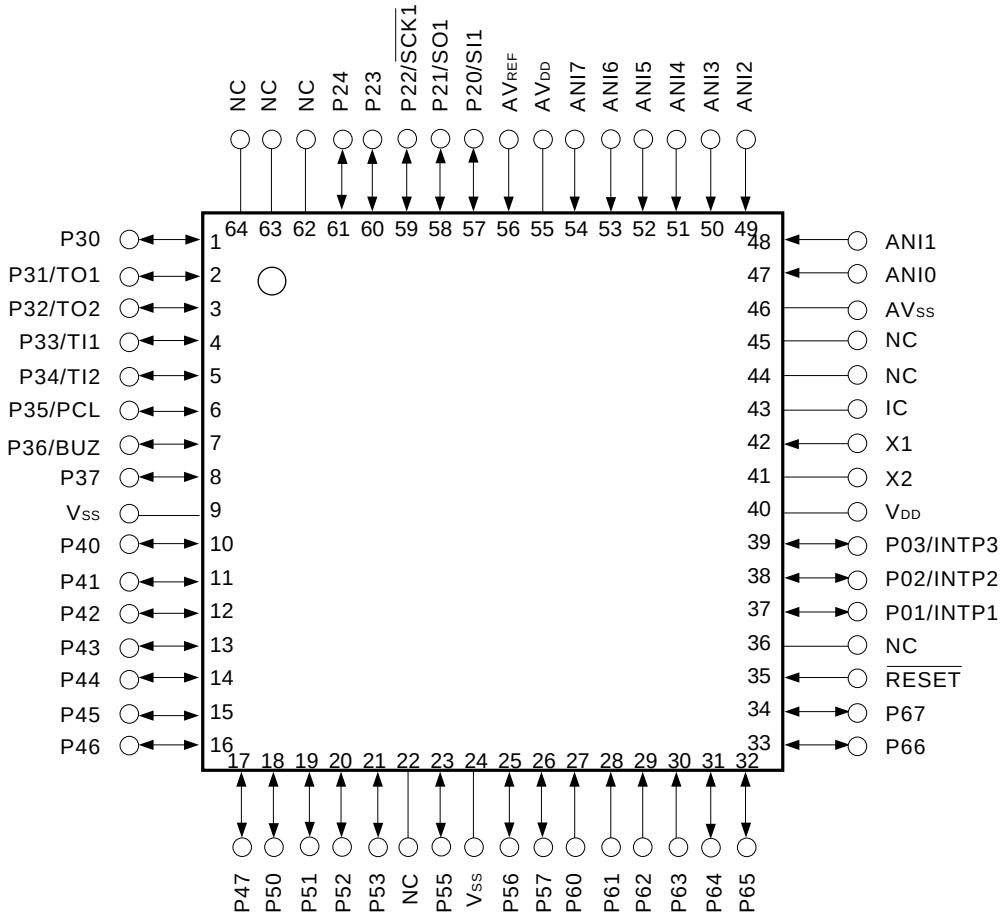
Cautions 1. Always connect the IC (Internally Connected) pin to V_{SS} directly.

2. Always connect the NC (Non-connection) pin to V_{SS} (However, can also be left open).

3. Always connect the AV_{DD} pin to V_{DD}.

4. Always connect the AV_{SS} pin to V_{SS}.

- **64-Pin Plastic QFP (14 x 14 mm)**
  μPD780001GC-xxx-AB8



Cautions 1. Always connect the IC (Internally Connected) pin to V_{SS} directly.

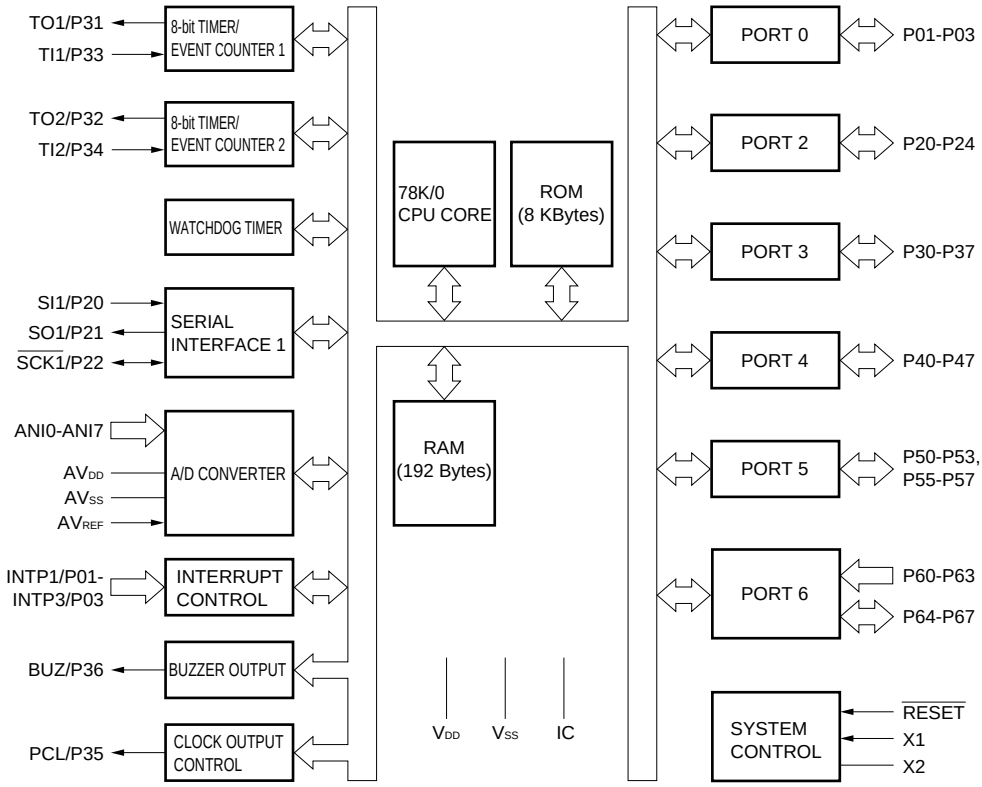
2. Always connect the NC (Non-connection) pin to V_{SS} (However, can also be left open).

3. Always connect the AV_{DD} pin to V_{DD}.

4. Always connect the AV_{SS} pin to V_{SS}.

P01-P03	: Port 0	PCL	: Programmable Clock
P20-P24	: Port 2	BUZ	: Buzzer Clock
P30-P37	: Port 3	X1, X2	: Crystal
P40-P47	: Port 4	$\overline{\text{RESET}}$	: Reset
P50-P53, P55-P57	: Port 5	ANI0-ANI7	: Analog Input
P60-P67	: Port 6	AV_{DD}	: Analog Power Supply
INTP1-INTP3	: Interrupt from Peripherals	AV_{SS}	: Analog Ground
TI1, TI2	: Timer Input	AV_{REF}	: Analog Reference Voltage
TO1, TO2	: Timer Output	V_{DD}	: Power Supply
SI1	: Serial Input	V_{SS}	: Ground
SO1	: Serial Output	IC	: Internally Connected
$\overline{\text{SCK1}}$	: Serial Clock	NC	: Non-Connection

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function		After Reset	Alternate Function
P01-P03	Input/ output	Port 0 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	INTP1-INTP3
P20	Input/ output	Port 2 5-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23, 24					—
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	—
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40-P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50-P53, P55-P57	Input/ output	Port 5 7-bit input/output port. LEDs can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	—
P60-P63	Input	Port 6	Input only.	Input	—
P64-P67	Input/ output	8-bit input/output port.	Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	—

3.2 Non-port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP1	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P01
INTP2				P02
INTP3		Falling edge detection external interrupt input.		P03
SI1	Input	Serial interface serial data input.	Input	P20
SO1	Output	Serial interface serial data output.	Input	P21
$\overline{SCK1}$	Input/ output	Serial interface serial clock input/output.	Input	P22
TI1	Input	External count clock input to 8-bit timer (TM1).	Input	P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO1	Output	8-bit timer output.	Input	P31
TO2				P32
PCL	Output	Clock output (for main system clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
ANI0-ANI7	Input	A/D converter analog input.	Input	—
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internally connected. Connected to V_{SS} directly.	—	—
NC	—	Not internally connected. Connected to V_{SS} (Also can be left open).	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

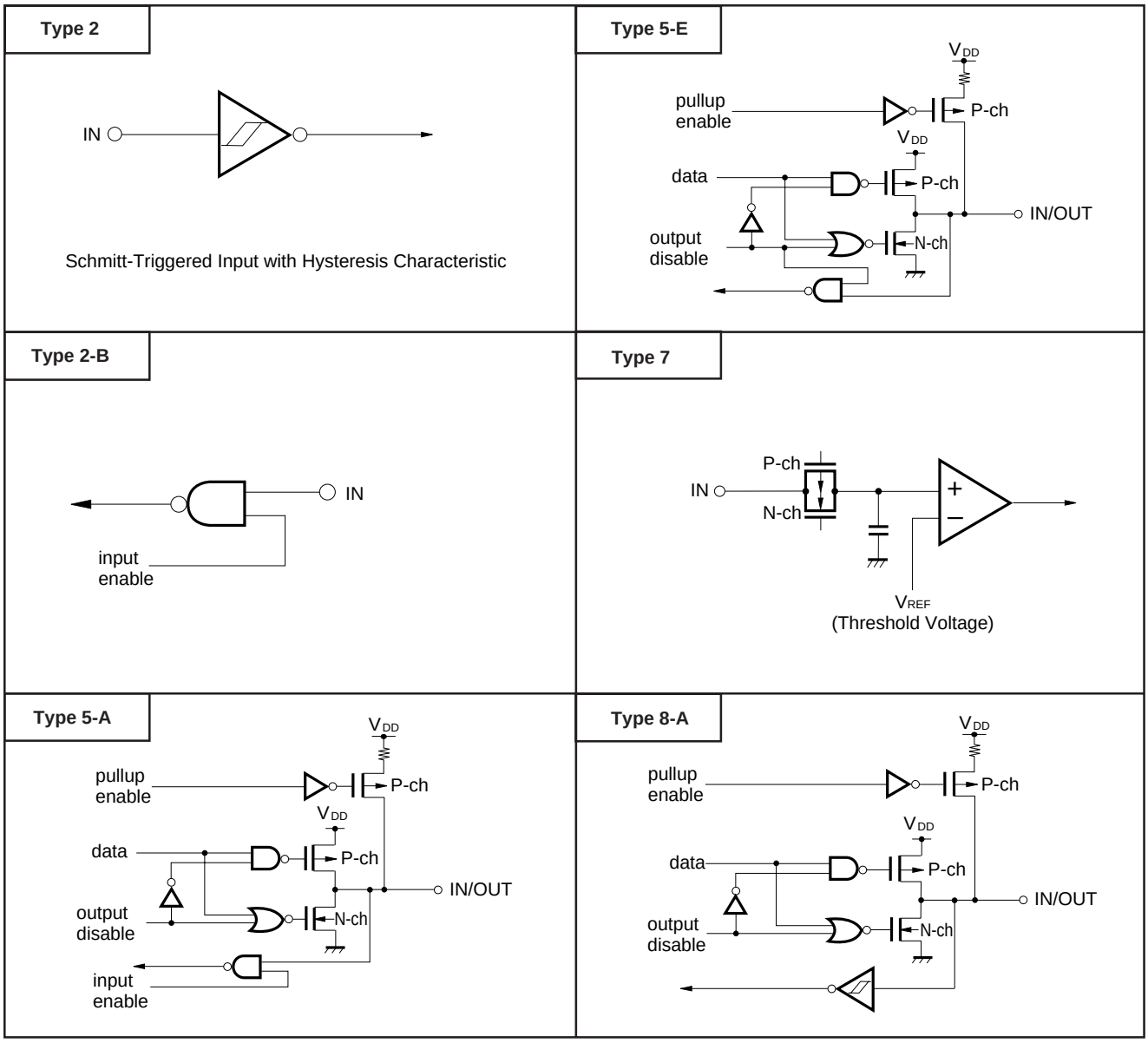
The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuit

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection when Not Used
P01/INTP1	8-A	Input/output	Independently connected to V_{SS} through resistor.
P02/INTP2			
P03/INTP3			
ANI0-ANI7	7	Input	Connected to V_{DD} or V_{SS}.
P20/SI1	8-A	Input/output	Independently connected to V_{DD} or V_{SS} through resistor.
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23	5-A		
P24	8-A		
P30	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40-P47	5-E	Input/output	Independently connected to V_{DD} through resistor.
P50-P53	5-A	Input/output	Independently connected to V_{DD} or V_{SS} through resistor.
P55-P57			
P60-P63	2-B	Input	Connected to V_{DD} or V_{SS}.
P64-P67	5-A	Input/output	Independently connected to V_{DD} or V_{SS} through resistor.
$\overline{RESET}$	2	Input	—
AV_{REF}	—	—	Connected to V_{SS}.
AV_{DD}			Connected to V_{DD}.
AV_{SS}			Connected to V_{SS}.
IC			Connected to V_{SS} directly.
NC			Connected to V_{SS} (Also can be left open).

Caution The connection of the NC pin differs from that of the PROM version (μPD78P018F).

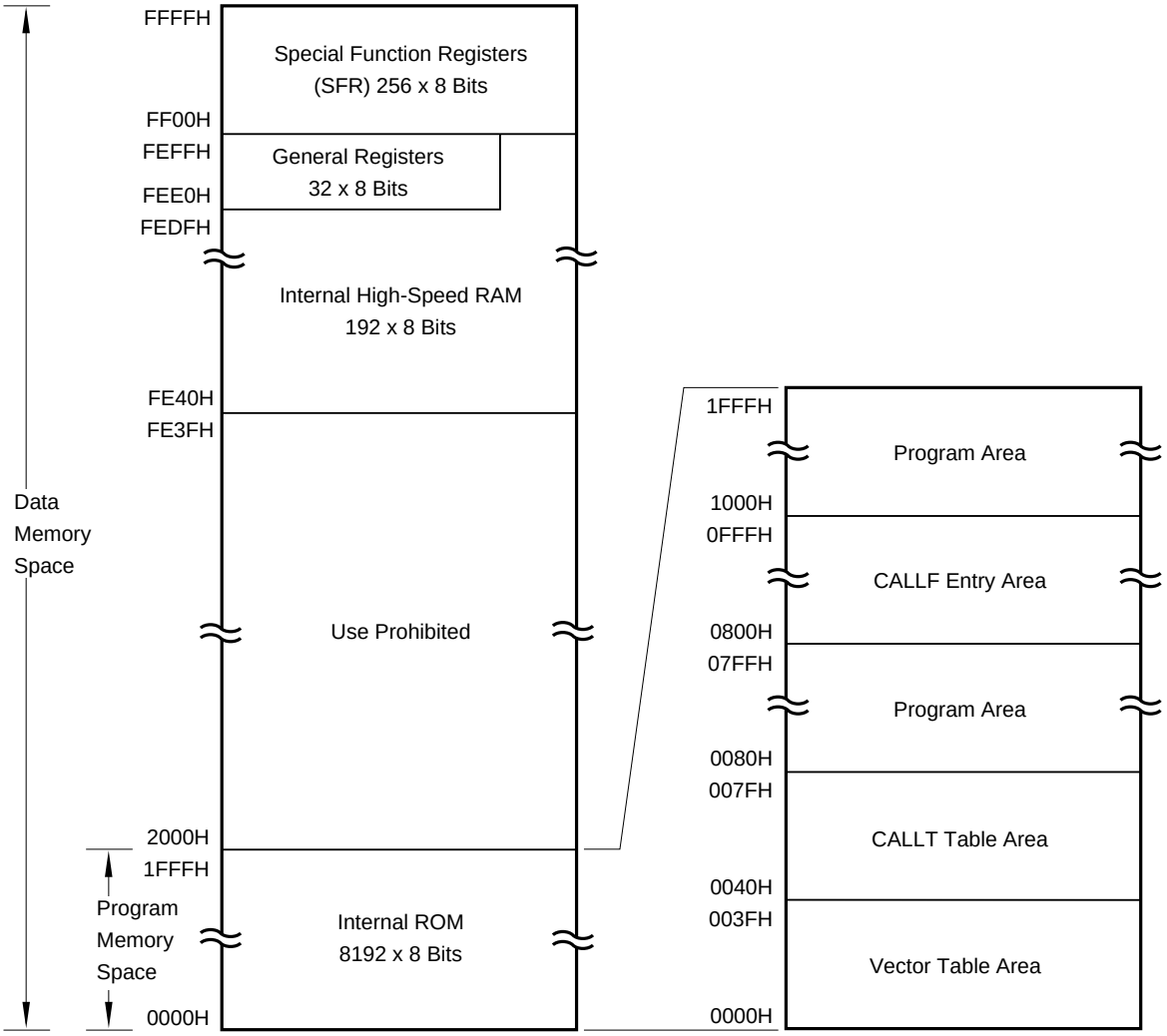
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of the μPD780001 is shown in Figure 4-1.

Figure 4-1. Memory Map



5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following two types of I/O ports are provided.

- CMOS input (P60-P63) : 4
- CMOS input/output (port 0, port 2-port 5, P64-P67) : 35

Total : 39

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P01-P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 2	P20-P24	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 3	P30-P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 4	P40-P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, on-chip pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50-P53, P55-P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software. LEDs can be driven directly.
Port 6	P60-P63	Input-only port.
	P64-P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.

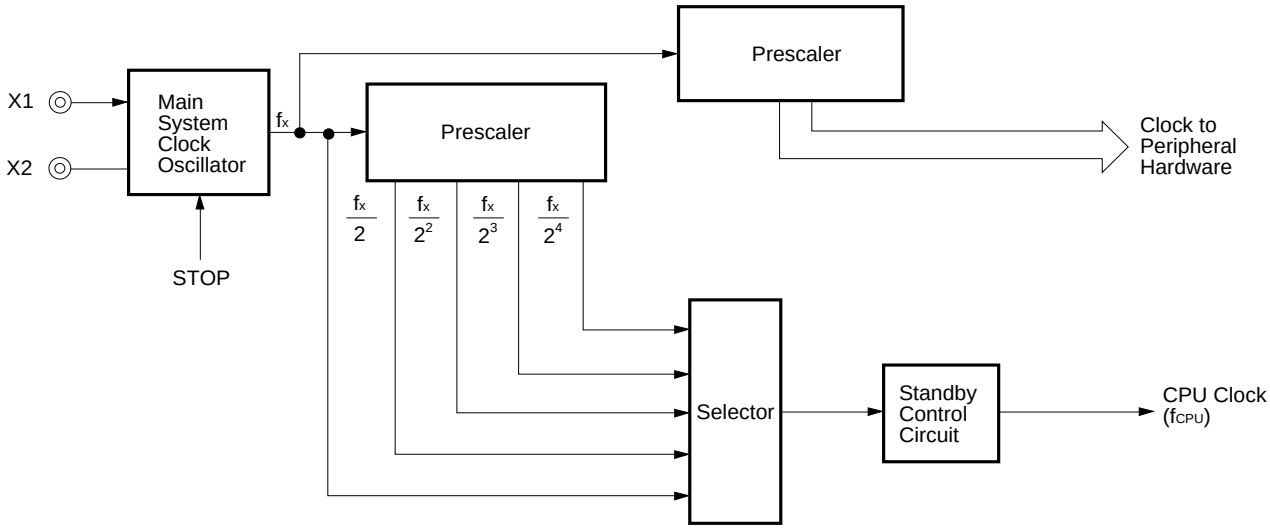
5.2 Clock Generator

An on-chip main system clock generator is provided.

The instruction exection time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (Main system clock: at 10.0-MHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

The following three channels are incorporated in the timer/event counter.

- 8-bit timer/event counter : 2 channels
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counter

		8-bit Timer/Event Counter	Watchdog Timer
Type	Interval timer	2 channels	1 channel
	External event counter	2 channels	–
Functions	Timer output	2 outputs	–
	Square wave output	2 outputs	–
	Interrupt request	2	1

Figure 5-2. 8-bit Timer/Event Counter Block Diagram *

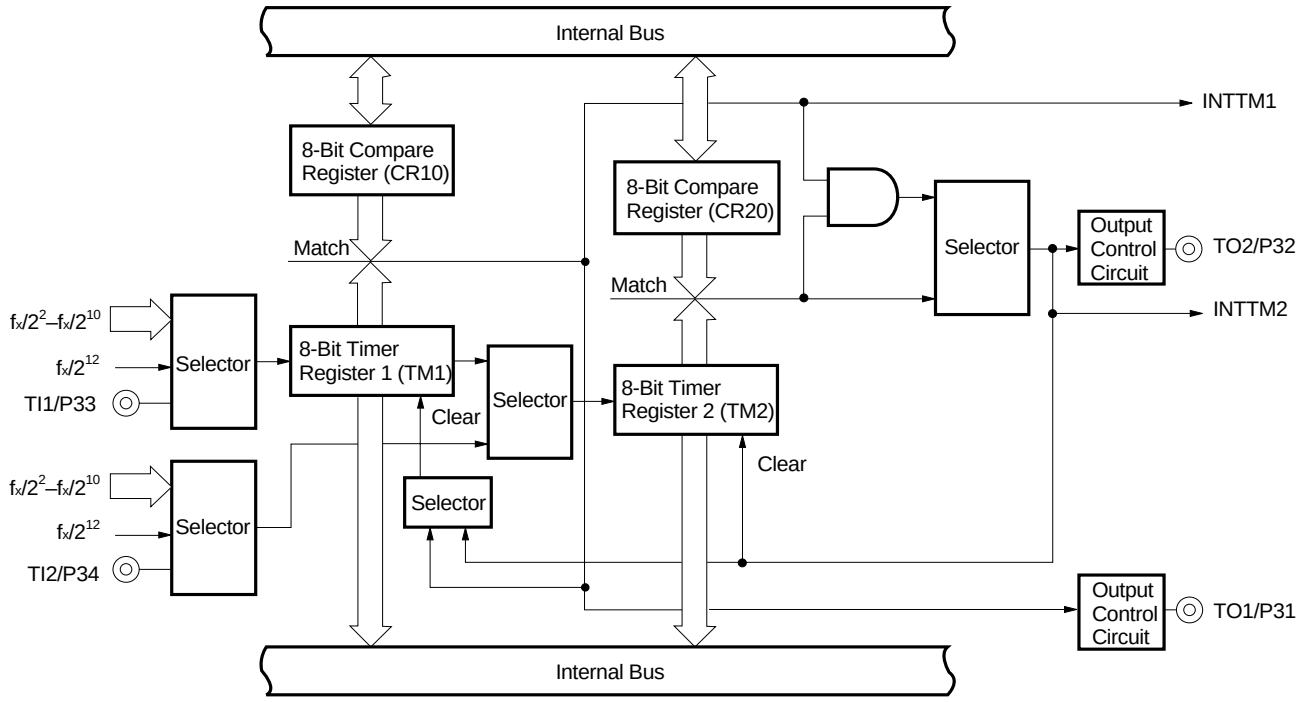
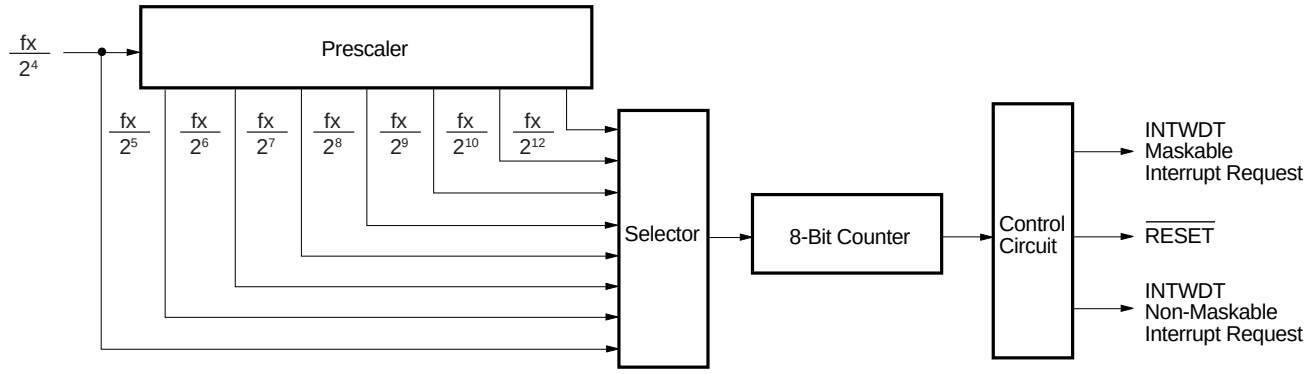


Figure 5-3. Watchdog Timer Block Diagram

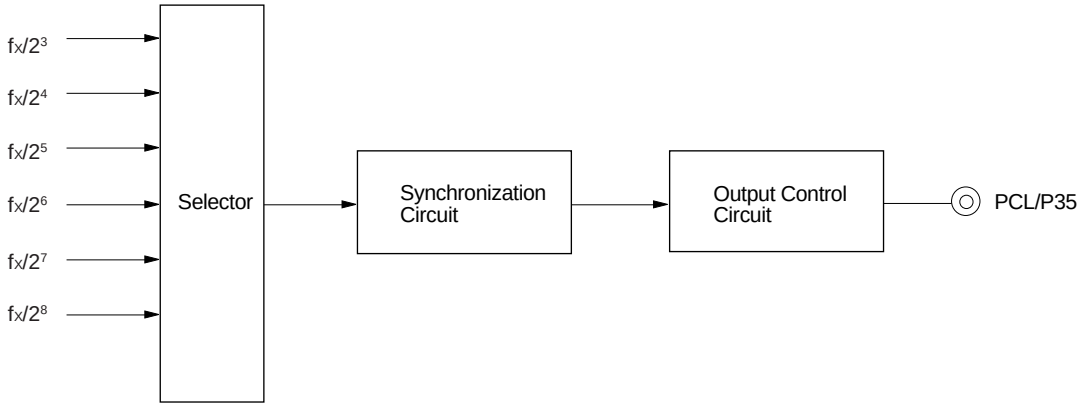


5.4 Clock Output Control Circuit

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0-MHz operation)

Figure 5-4. Clock Output Control Circuit Block Diagram

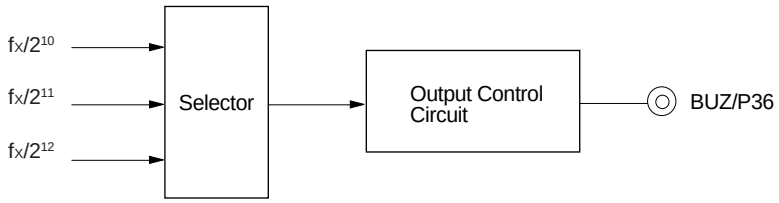


5.5 Buzzer Output Control Circuit

A clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0-MHz operation)

Figure 5-5. Buzzer Output Control Circuit Block Diagram



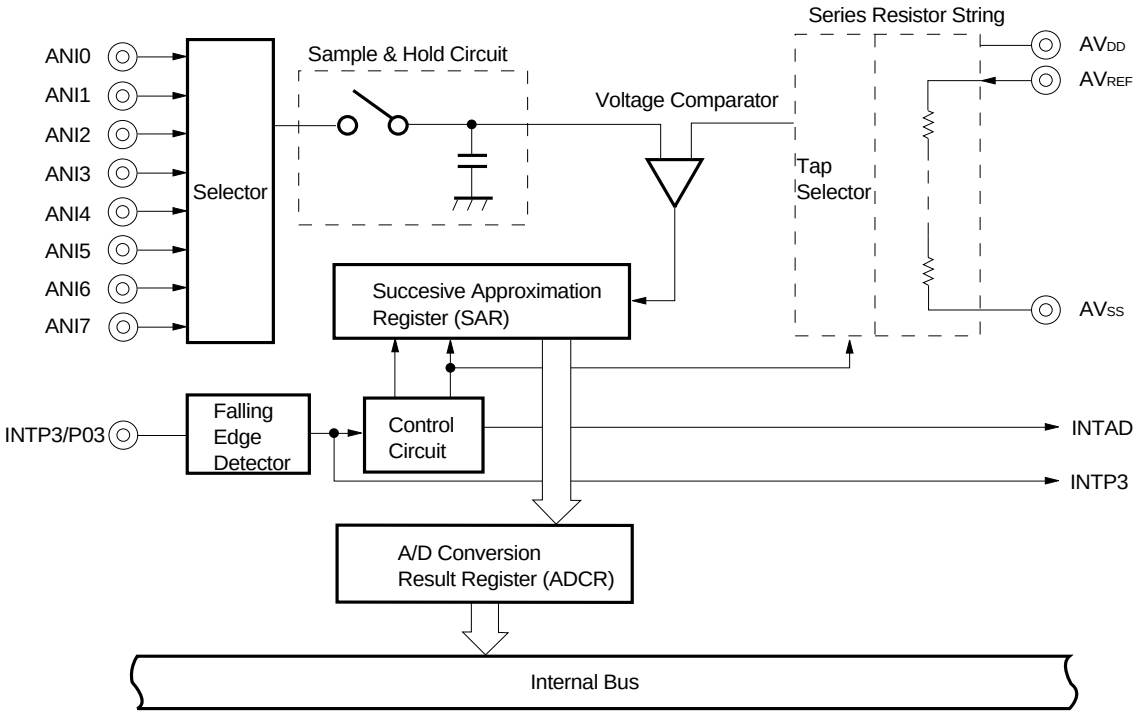
5.6 A/D Converter

The A/D converter has on-chip eight 8-bit resolution channels.

There are the following two methods to start A/D conversion.

- Hardware starting
- Software starting

Figure 5-6. A/D Converter Block Diagram

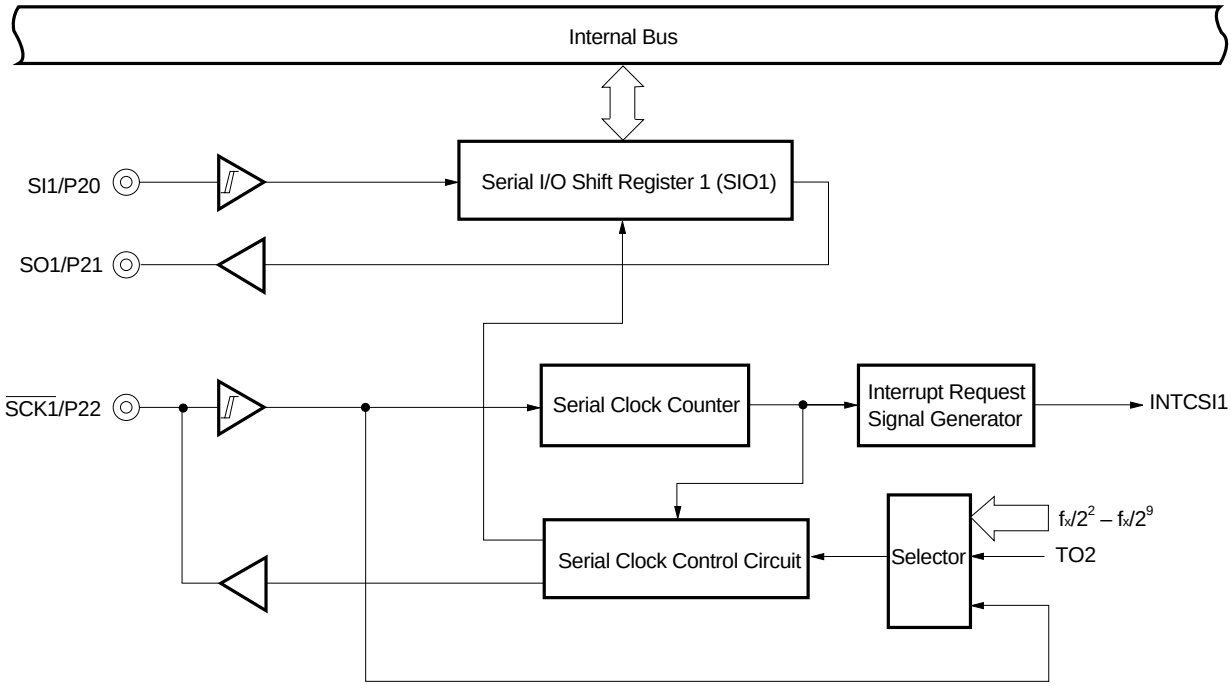


5.7 Serial Interface

One on-chip clocked serial interface is provided.

Serial interface channel 1 operates in MSB/LSB-first switchable 3-wire serial I/O mode.

Figure 5-7. Serial Interface Channel 1 Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTION

6.1 Interrupt Functions

There are 10 interrupt functions of 3 different kinds as shown below.

- Non-maskable interrupt : 1
- Maskable interrupts : 8
- Software interrupt : 1

Table 6-1. Interrupt Source List

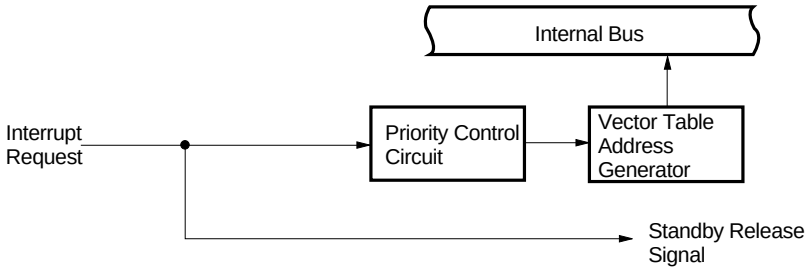
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic[Note 2] Configuration Type
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP1	Pin input edge detection	External	0008H	(C)
	2	INTP2			000AH	
	3	INTP3			000CH	
	4	INTCSI1	Serial interface channel 1 transfer end	Internal	0010H	(B)
	5	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
	6	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
	7	INTAD	A/D converter conversion end		001AH	
Software	—	BRK	BRK instruction execution	Internal	003EH	(D)

Notes 1. The default priority is the priority applicable when more than one maskable interrupt is generated. 0 is the highest priority and 7, the lowest.

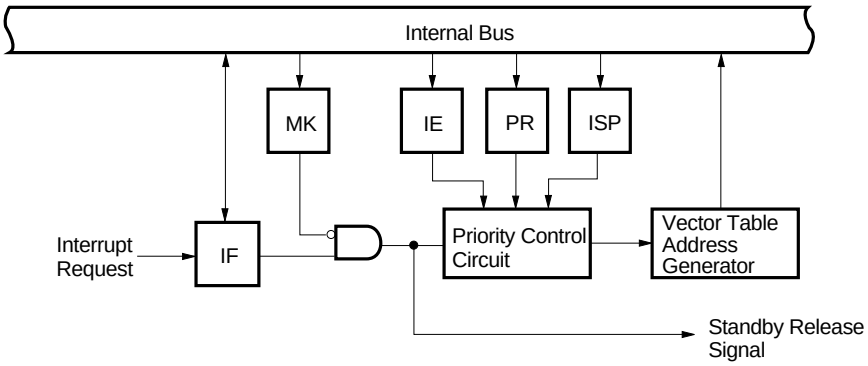
2. Basic configuration types (A) - (D) correspond to those on Figure 6-1.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt

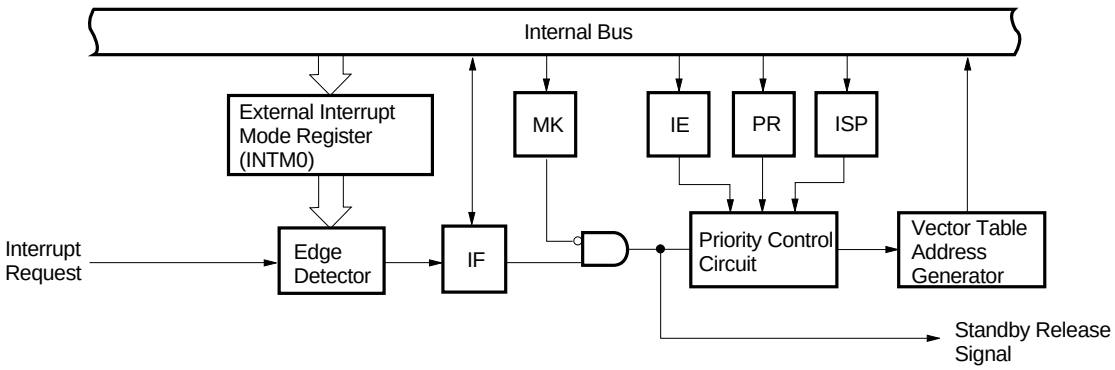
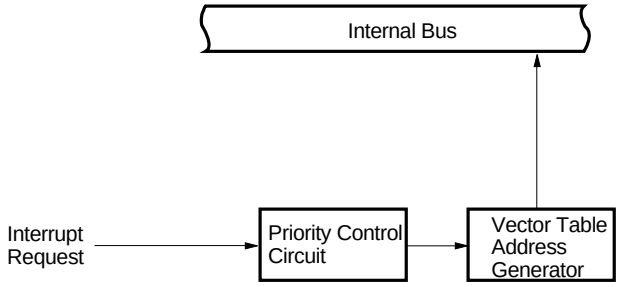


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) Software Interrupt



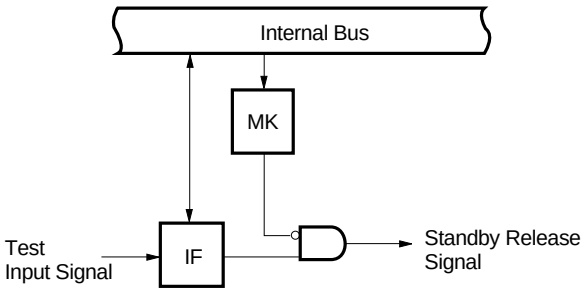
IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority spcification flag

6.2 Test Function

The following one test function is provided.

Test Source		Internal/External
Name	Trigger	
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
MK : Test mask flag

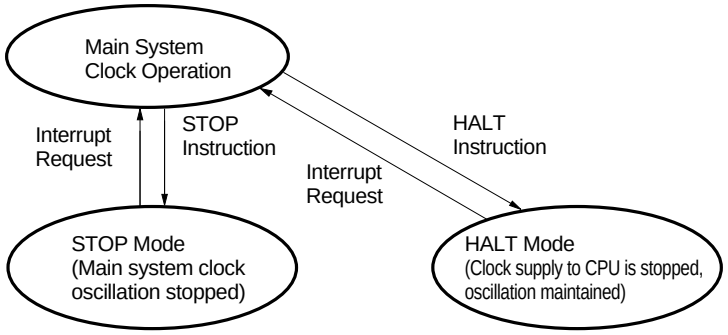
7. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current consumption.

- HALT mode : The CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation in combination with the normal operating mode.

- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power dissipation.

Figure 7-1. Standby Functions



8. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin.
- Internal reset by watchdog timer runaway time detection.

9. INSTRUCTION SET

(1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r=A

(2) 16-Bit Instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp=BC, DE, HL.

(3) Bit Manipulation Instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call Instruction/Branch Instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF, BTCLR, DBNZ

(5) Other Instruction

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS *

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions			Ratings	Unit
Supply voltage	V_{DD}				–0.3 to +7.0	V
	AV_{DD}				–0.3 to V_{DD} +0.3	V
	AV_{REF}				–0.3 to V_{DD} +0.3	V
	AV_{SS}				–0.3 to +0.3	V
Input voltage	V_I	P01-P03, P20-P24, P30-P37, P40-P47, P50-P53, P55-P57, P60-P67, X1, X2			–0.3 to V_{DD} +0.3	V
Output voltage	V_O				–0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AN}	ANI0-ANI7	Analog input pins		AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	Per pin			–10	mA
		Total for P20-P24, P30-P37			–15	mA
		Total for P01-P03, P40-P47, P50-P53, P55-P57, P64-P67			–15	mA
Output current, low	I_{OL} Note	Per pin		Peak value	30	mA
				r.m.s. value	15	mA
		Total for P40-P47, P50-P53, P55		Peak value	100	mA
				r.m.s. value	70	mA
		Total for P01-P03, P56, P57, P64-P67		Peak value	100	mA
				r.m.s. value	70	mA
		Total for P01-P03, P64-P67		Peak value	50	mA
				r.m.s. value	20	mA
		Total for P20-P24, P30-P37		Peak value	50	mA
				r.m.s. value	20	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{opt}				–65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] $\times \sqrt{\text{Duty}}$

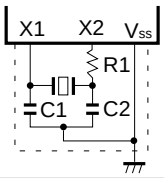
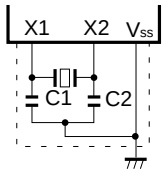
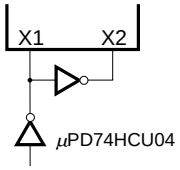
Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz, unmeasured pins returned to 0 V.	P01-P03, P20-P24, P30-P37, P40-P47, P50-P53, P55-P57, P64-P67			15	pF

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	1		10	MHz
		Oscillation stabilization time Note 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1	8.38	10	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		10.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		42.5		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to AC Characteristics.

2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the power source to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P21, P23, P30-P32, P35-P37, P40-P47, P50-P53, P55-57, P60-P67		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P01-P03, P20, P22, P24, P33, P34, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD}–0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P21, P23, P30-P32, P35-P37, P40-P47, P50-P53, P55-P57, P60-P67		0		0.3V_{DD}	V
	V_{IL2}	P01-P03, P20, P22, P24, P33, P34, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = –100 μA		V_{DD}–0.5			V
Output voltage, low	V_{OL1}	P50-P53, P55-P57	V_{DD} = 4.5 to 5.5 V, I_{OH} = 15 mA		0.4	2.0	V
		P01-P03, P20-24, P30-P37, P40-P47, P64-P67	V_{DD} = 4.5 to 5.5 V, I_{OH} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LH1}	V_{IN} = V_{DD}	P01-P03, P20-24, P30-P37, P40-P47, P50-P53, P55-P57, P60-P67, ANI0-ANI7, $\overline{\text{RESET}}$			3	μA
	I_{LH2}		X1, X2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P01-P03, P20-24, P30-P37, P40-P47, P50-P53, P55-P57, P60-P67, ANI0-ANI7, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistance	R	V_{IN} = 0 V, P20-P24, P30-P37, P40-P47, P50-P53, P55-P57, P64-P67	4.5 ≤ V_{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 ≤ V_{DD} < 4.5 V	20		500	kΩ

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	8.38-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10% [Note 2]		6.5	19.5	mA
			V_{DD} = 3.0 V ± 10% [Note 3]		0.7	2.1	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10%		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10%		550	1650	μA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ± 10%		0.1	20	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA

Notes 1. Not including AV_{REF} current and port current.

2. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

3. Low-speed mode operation (when PCC is set to 04H).

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

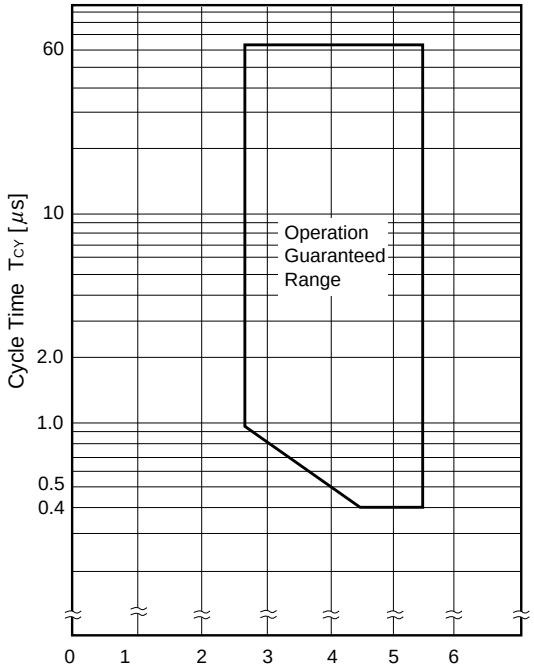
AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(1) Basic Operation

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 4.5 to 5.5 V	0.4		64	μs
			0.96		64	μs
TI1, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 5.5 V	0		4	MHz
			0		275	kHz
TI1, TI2 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 5.5 V	100			ns
			1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP1-INTP3	10			μs
		KR0-KR7	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

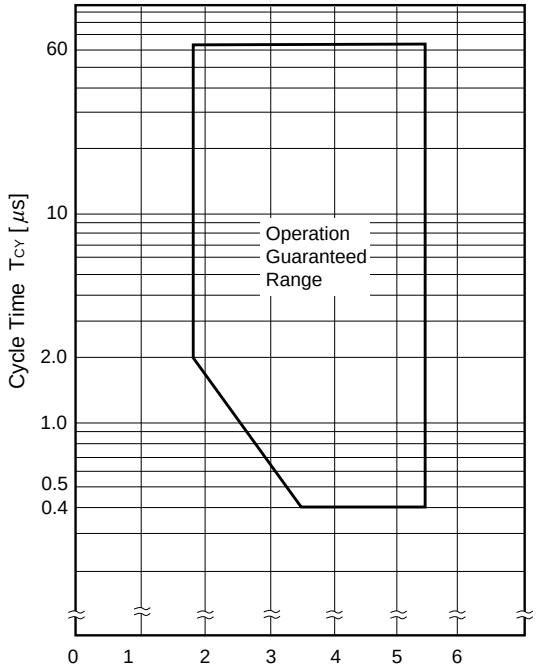
μPD780001

T_{CY} vs V_{DD} (Main System Clock Operation)



μPD78P018F (Reference)

T_{CY} vs V_{DD} (Main System Clock Operation)



Caution The operation guaranteed range of the μPD780001 is different from that of the μPD78P018F.

(2) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1},	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
	t_{KL1}		100			ns
SI1 setup time	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
(to $\overline{SCK1}$ ↑)			150			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI1}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO1}	C = 100 pF[Note]			300	ns

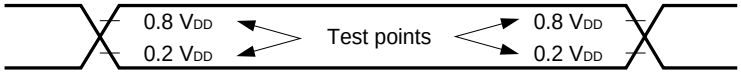
Note C is the SO1 output line load capacitance.

(b) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

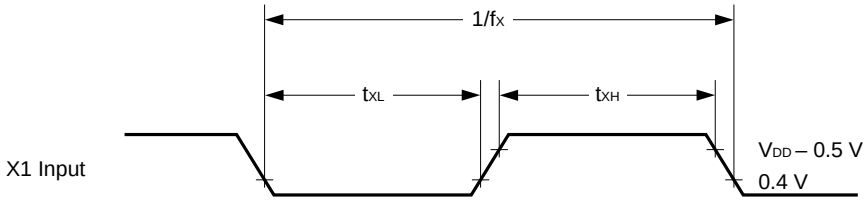
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL2}		800			ns
SI1 setup time	t_{SIK2}		100			ns
(to $\overline{SCK1}$ ↑)						ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI2}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_R, t_F	V_{DD} = 4.5 to 5.5 V			1000	ns

Note C is the SO1 output line load capacitance.

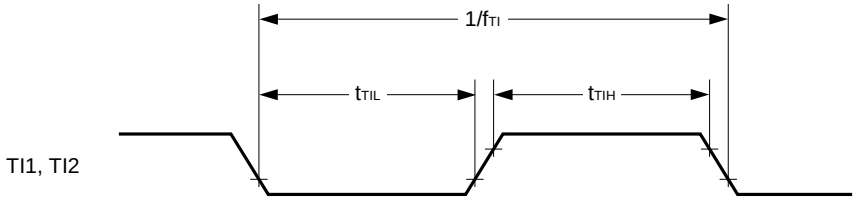
AC Timing Test Point (Excluding X1 Input)



Clock Timing

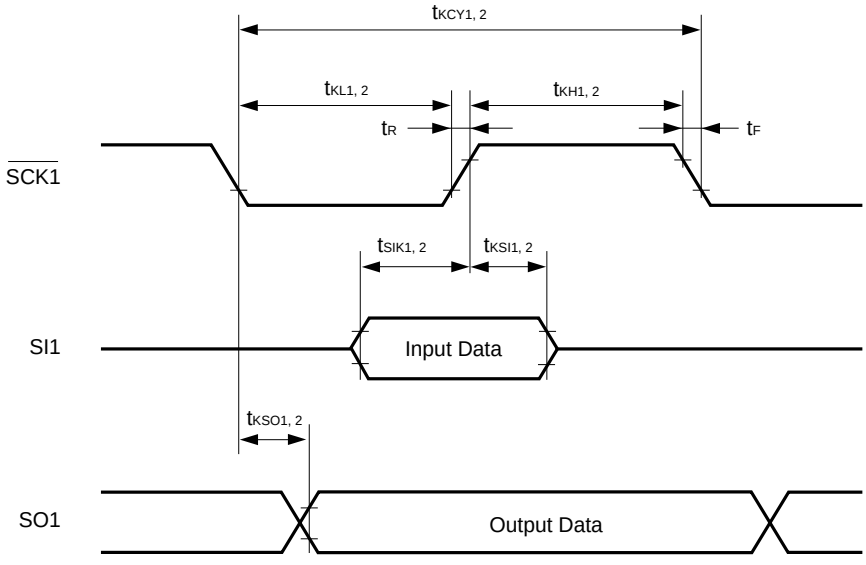


TI Timing



Serial Transfer Timing

3-wire serial I/O mode:



A/D Converter Characteristics (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 4.2 to 5.5 V, AV_{SS} = V_{SS} = 0 V)
(T_A = –10 to +85 °C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error Note					0.6	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		24/f_x			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{AIREF}		4	14		kΩ

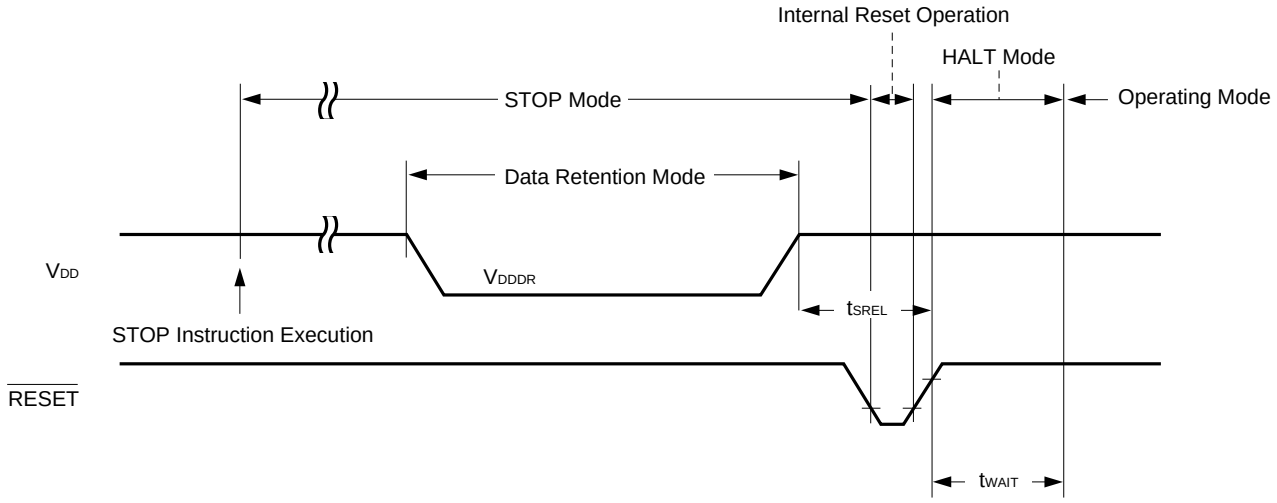
Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

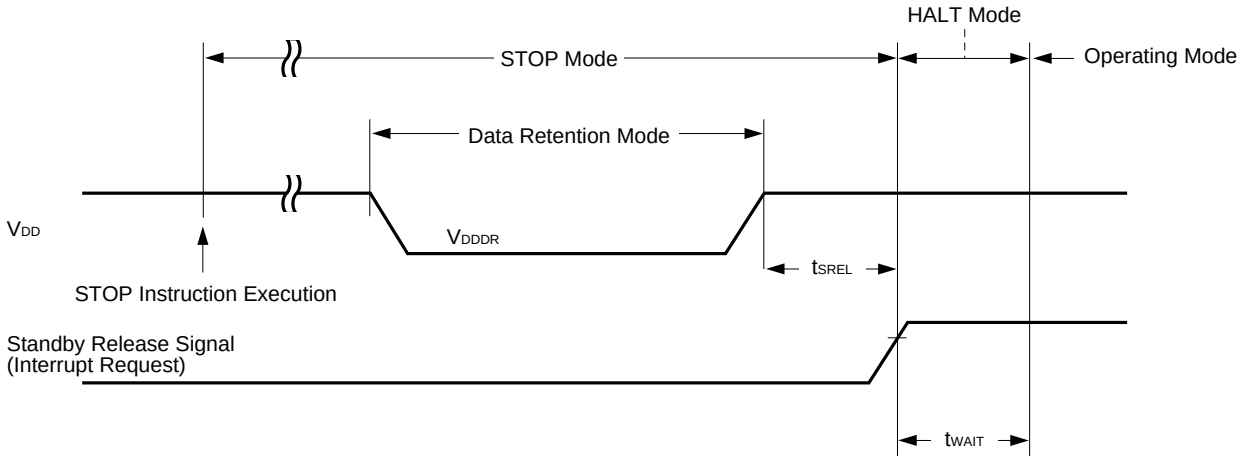
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{18}/f_x$		ms
		Release by interrupt		**Note**		ms

Note $2^{13}/f_x$ or $2^{15}/f_x$-$2^{18}/f_x$ can be selected by bit 0-bit 2 (OSTS0-OSTS2) of oscillation stabilization time selection register (OSTS).

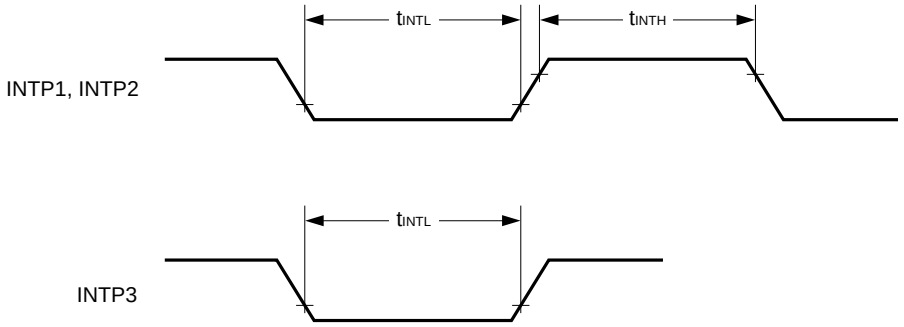
Data Retention Timing (STOP mode released by $\overline{RESET}$)



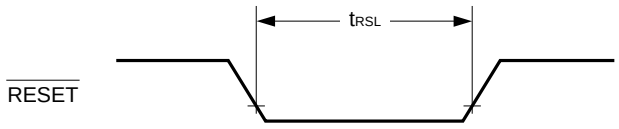
Data Retention Timing (Standby release signal: STOP mode released by interrupt signal)



Interrupt Input Timing

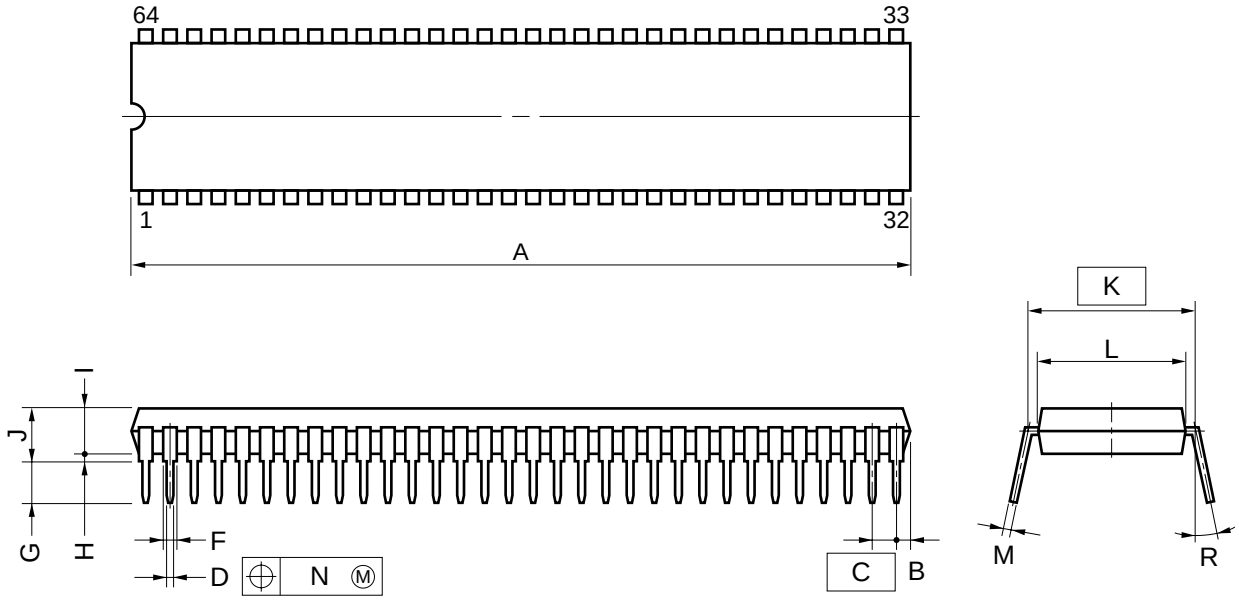


$\overline{\text{RESET}}$ Input Timing



11. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

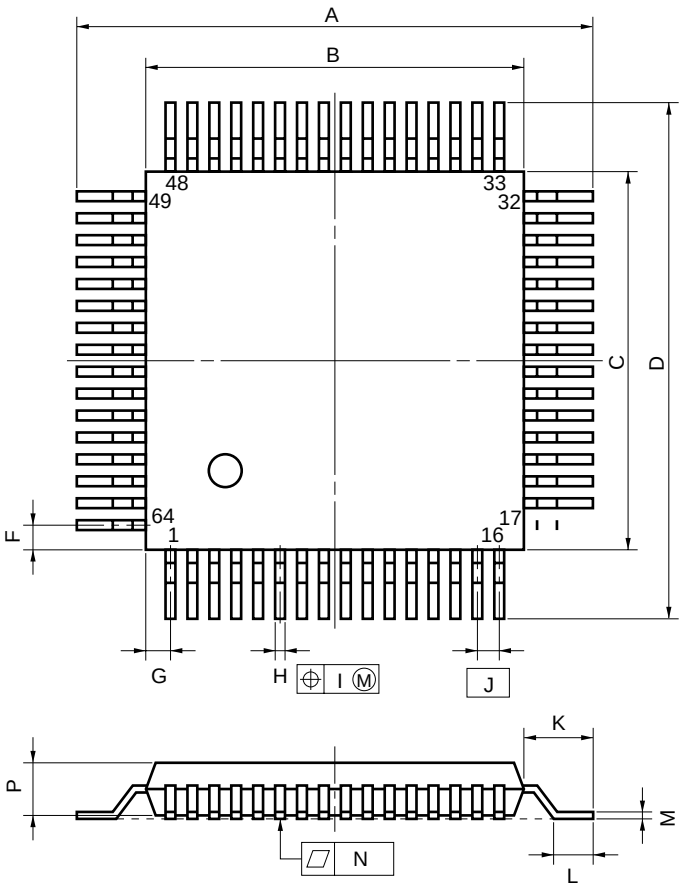
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

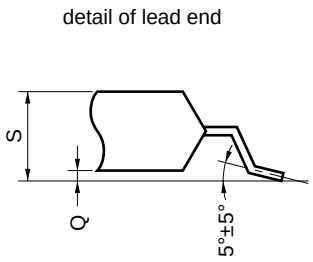
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

Remark The shape and material of the ES product is the same as those of the mass-produced product.

64 PIN PLASTIC QFP (□14)





P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Remark The shape and material of the ES product is the same as those of the mass-produced product.

* 12. RECOMMENDED SOLDERING CONDITIONS

It is recommended that the μPD780001 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended, please contact an NEC sales representative.

Table 12-1. Surface Mount Type Soldering Conditions

μPD780001GC-XXX-AB8: 64-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max. < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 2 max. < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-00-2
Wave soldering	Solder temperature: 260°C max., Time: 10 seconds max., Number of times: 1, Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Time: 3 seconds max. (per device side)	—

Caution Do not use different soldering methods together (except for partial heating method).

Table 12-2. Through-Hole Type Soldering Conditions

μPD780001CW-XXX: 64-pin plastic shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin)

Caution Apply wave soldering only to the pins and be careful so as not to bring solder into direct contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780001.

Language Processing Software

RA78K/0[Notes 1, 2, 3]	Assembler package common to the 78K/0 series
CC78K/0[Notes 1, 2, 3]	C compiler package common to the 78K/0 series
DF780001[Notes 1, 2, 3]	μPD780001 device file *
CC78K/0-L[Notes 1, 2, 3]	C compiler library source file common to the 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P018CW PA-78P018GC PA-78P018KK-S	Programmer adapter connected to the PG-1500
PG-1500 Controller[Notes 1, 2]	Control program used for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 series
IE-78000-R-BK	Break board common to the 78K/0 series
IE-78014-R-EM-A	Emulation board common to the μPD78018F subseries, etc.
EP-78240CW-R EP-78240GC-R	Emulation probe common to the μPD78244 subseries
EV-9200GC-64	Socket to be mounted on user system board created for the 64-pin plastic QFP
SM78K0[Notes 4, 5]	System simulator common to the 78K/0 series
SD78K/0[Notes 1, 2]	IE-78000-R screen debugger
DF780001[Notes 1, 2, 4, 5]	μPD780001 device file *

Real-Time OS

MX78K0[Notes 1, 2, 3]	78K/0 series OS

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 5]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Notes 1, 2]	Fuzzy inference module
FD78K0[Notes 1, 2]	Fuzzy inference debugger

Notes 1. Based on PC-9800 series (MS-DOS™)

2. Based on IBM PC/AT™ (PC DOS™)

3. Based on HP9000 series 300™, HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™), and EWS-4800 series (EWS-UX/V)

4. Based on PC-9800 series (MS-DOS + Windows™)

5. Based on IBM PC/AT (PC DOS + Windows)

Remark RA78K/0, CC78K/0, SM78K0, and SD78K/0 are used in combination with the DF780001.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD780001 User's Manual	In preparation	Planned
78K/0 Series User's Manual—Instructions	IEU-849	IEU-1372
78K/0 Series Instruction Table	IEM-5522	—
78K/0 Series Instruction Set	IEM-5521	—
μPD780001 Special Function Register Table	Planned	—

Documents Related to Development Tools (User's Manual)

Document Name		Document No.		
		Japanese	English	
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399	
	Language	EEU-815	EEU-1404	
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402	
CC78K Series C Compiler	Operation	EEU-656	EEU-1280	
	Language	EEU-655	EEU-1284	
CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	Planned	*
CC78K Series Library Source File		EEU-777	—	
PG-1500 PROM Programmer		EEU-651	EEU-1335	
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	Planned	
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	EEU-1291	
IE-78000-R		EEU-810	EEU-1398	
IE-78000-R-BK		EEU-867	EEU-1427	
IE-78014-R-EM-A		EEU-962	EEU-1487	
EP-78240		EEU-986	EEU-1513	
SM78K0 System Simulator	Reference	EEU-5002	Planned	
SM78K Series System Simulator	External parts user open interface specification	U10092J	Planned	*
SD78K/0 Screen Debugger	Introduction	EEU-852	—	
PC-9800 Series (MS-DOS) Based	Reference	EEU-816	—	
SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414	
IBM PC/AT (PC DOS) Based	Reference	EEU-993	EEU-1413	

Caution The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series OS MX78K0	Basic	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System–Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name	Document No.	
	Japanese	English
Semiconductor Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcontroller-Related Product Guide – Third Party Products –	MEI-604	—

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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