NEC

MOS INTEGRATED CIRCUIT

μPD9992

RING TONE GENERATOR LSI (WITH SURROUND SOUND) FOR MOBILE PHONES

DESCRIPTION

The μPD9992 is a mobile phone ring tone generator LSI that includes an on-chip surround sound function.

FEATURES

- PCM sound generation method provides realistic sound reproduction
- Up to 68 (= 64 polyphonic + 4 ADPCM) tones can be played at the same time, so an abundant variety of tunes can be generated and played
- Implements ADPCM decode functions. Simultaneous playback with MIDI is also enabled.
- Includes a high-performance D/A converter with 16-bit resolution
- Supports five sampling frequency modes: 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz (ASI only)
- Provides audio serial I/O interface (16 bits).
  The serial data input frequency is variable between 32 fs and 64 fs (during slave mode).
  Supported formats are right-justified, left-justified, and IIS.
- Includes function for mixing PCM sound source output signals and audio serial input signals (only fs = 32 kHz sampling is supported).
- Includes a surround function that uses real-time processing (to produce surround effects based on real-time processing for all sources including PCM sound sources and audio serial input).
- Host CPU is connected via an 8-bit parallel interface when PS = 0.
- Host CPU is connected via a 3-wire or 4-wire Serial Peripheral Interface (SPI) when PS = 1.
- Includes output control functions for vibrator and LED
- PLL is built-in, so various types of input clocks can be supported.
- Digital I/O supports EV_{DD} = 3 V and 1.8 V.
- Power supply voltages: DV_{DD}: 1.425 to 1.575 V, EV_{DD}: 1.71 to 3.3 V, AV_{DD}: 2.85 to 3.15 V, AV_{DD}_P: 2.85 to 3.15 V
- 65-pin tape FBGA package (6 × 6 mm body size, 0.5 ball pitch)

ORDERING INFORMATION

Part number	Package
★ μPD9992F9-BA1-A	65-pin tape FBGA (6 × 6)

Remark A Lead free product.

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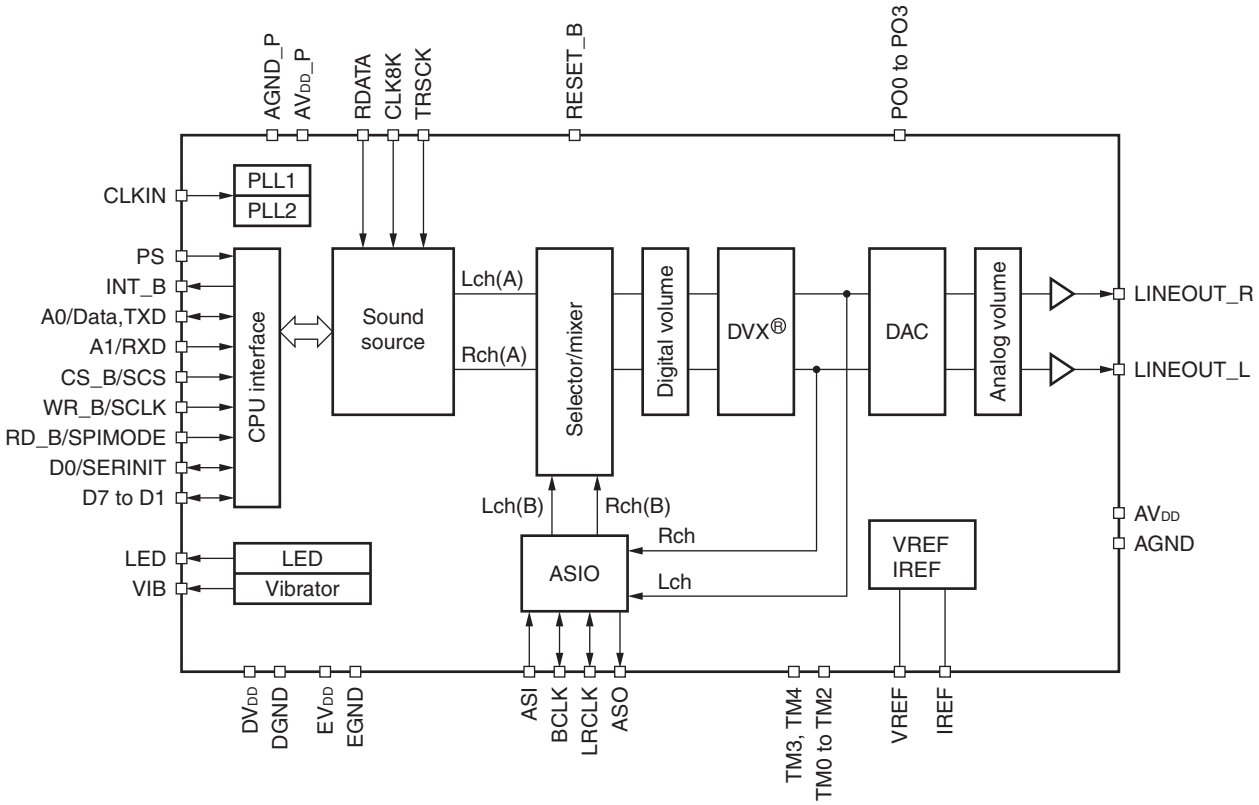
The mark ★ shows major revised points.

BLOCK DIAGRAM

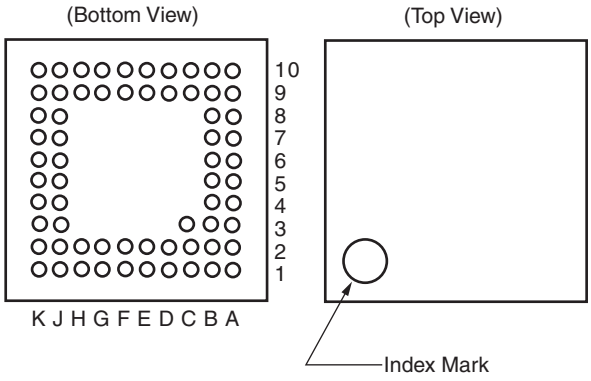


Remark DVX: DiMAGIC Virtualizer X®

PIN CONFIGURATION

- 65-pin tape FBGA (6 × 6)

★ μPD9992F9-BA1-A



Pin No.	Pin Name
1A	Shorted with 1K pin
1B	N.C
1C	LINEOUT_L
1D	AGND
1E	AV_{DD}
1F	LINEOUT_R
1G	AGND
1H	AGND_P
1J	N.C
1K	Shorted with 1A pin
2A	N.C
2B	N.C
2C	TM0
2D	IREF
2E	VREF
2F	TM1
2G	AV_{DD}_P

Pin No.	Pin Name
2H	CLKIN
2J	N.C
2K	N.C
3A	TM3
3B	TM2
3C	N.C
3J	PO1
3K	PO0
4A	RDATA
4B	TM4
4J	PO3
4K	PO2
5A	TRSCK
5B	CLK8K
5J	A1/RXD
5K	DGND

Pin No.	Pin Name
6A	EGND
6B	PS
6J	CS_B/SCS
6K	A0/Data,TXD
7A	ASI
7B	ASO
7J	RD_B/SPIMODE
7K	WR_B/SCLK
8A	LRCLK
8B	BCLK
8J	D1
8K	D0/SERINIT
9A	DV_{DD}
9B	N.C
9C	EV_{DD}
9D	VIB

Pin No.	Pin Name
9E	RESET_B
9F	D7
9G	D5
9H	D3
9J	N.C
9K	DV_{DD}
10A	Shorted with 10K pin
10B	N.C
10C	LED
10D	DV_{DD}
10E	INT_B
10F	D6
10G	D4
10H	D2
10J	DGND
10K	Shorted with 10A pin

Remark N.C: Reserved for future use. Leave this pin open.

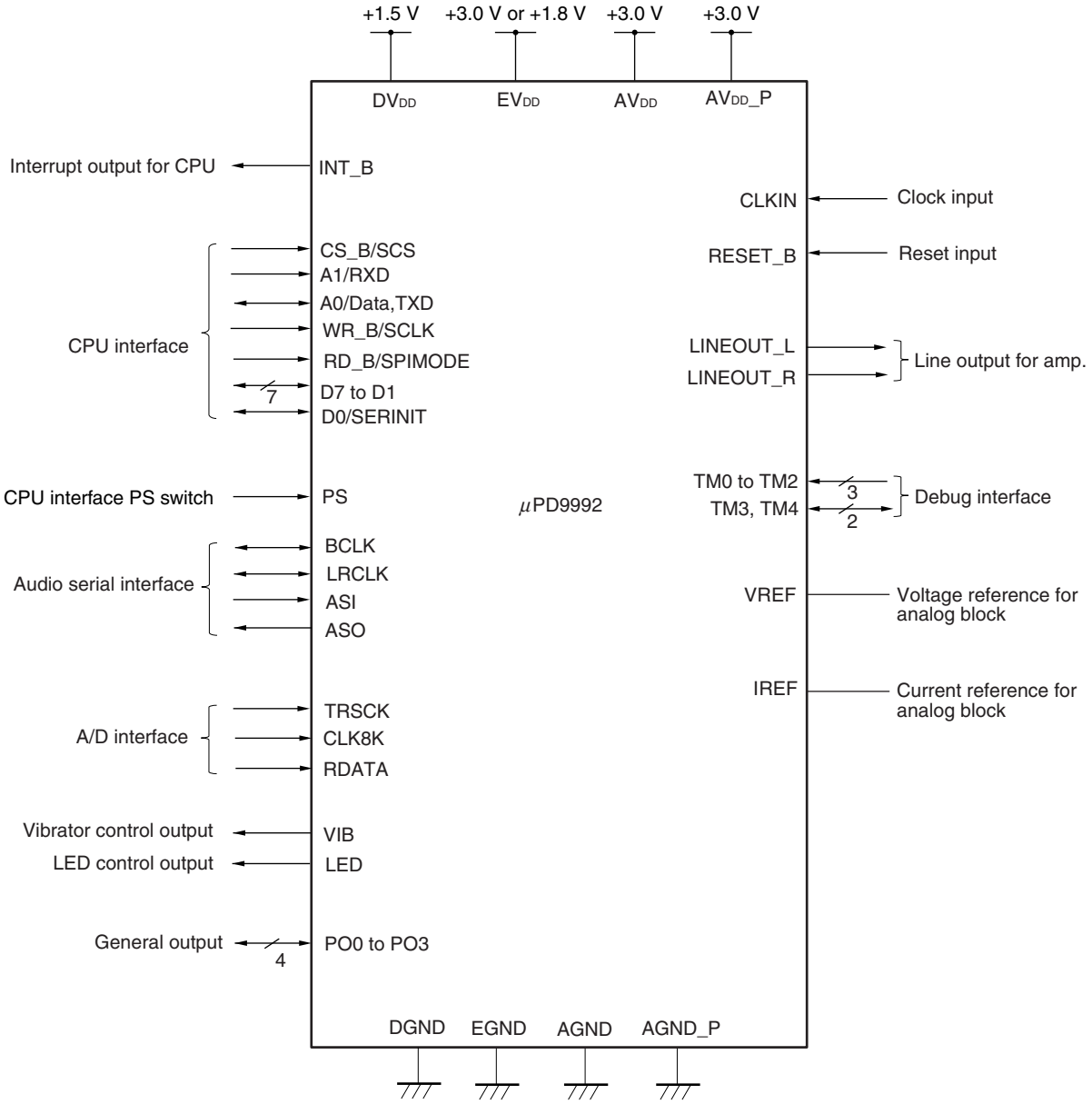
PIN NAME

A0, A1:	Address
AGND:	Ground for analog block
AGND_P:	Ground for PLL
ASI:	Audio serial data input
ASO:	Audio serial data output
AV_{DD}:	Power supply for analog block
AV_{DD}_P:	Power supply for PLL
BCLK:	Bit clock input/output
CS_B:	Chip select
CLK8K:	Sync clock input for RDATA
CLKIN:	Clock input
D0 to D7:	Data bus
Data:	Data
DV_{DD}:	Power supply for digital block
DGND:	Ground for digital block
EV_{DD}:	Power supply for I/O pins
EGND:	Ground for I/O pins
INT_B:	Interruption
IREF:	Current reference for Analog Block
LED:	LED control output
LINEOUT_L:	Line out (L ch)
LINEOUT_R:	Line out (R ch)
LRCLK:	Left right clock input/output
PO0 to PO3:	Peripheral output
PS:	Parallel serial select
RD_B:	Read
RDATA:	Record data
RESET_B:	Reset
RXD:	RX serial data input
SCLK:	Clock for serial I/F
SCS:	Chip select input for serial I/F
SERINIT:	Initialization signal for serial I/F
SPIMODE:	SPI mode select
TM0 to TM2:	Test mode input
TM3,TM4:	Test mode I/O
TRSCK:	Clock input for RDATA
TXD:	TX serial data output
VIB:	Vibration control output
VREF:	Voltage reference for Analog Block
WR_B:	Write

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Configuration



1.2 Explanation of Pin Functions

(1) Power supply pins

Pin Name	Pin No.	I/O	Function
DV_{DD}	9A, 9K, 10D	–	Power supply (1.5 V) for digital block Be sure to connect a 0.1 μF capacitor between this pin and DGND.
DGND	5K, 10J	–	Ground for digital block
EV_{DD}	9C	–	Power supply (3 V or 1.8 V) for I/O Be sure to connect a 0.1 μF capacitor between this pin and EGND. Use a different power supply to the analog power supply.
EGND	6A	–	Ground for I/O
AV_{DD}	1E	–	Power supply (3 V) for analog Be sure to connect a 0.1 μF capacitor between this pin and AGND.
AGND	1D, 1G	–	Ground for analog block
AV_{DD}_P	2G	–	Power supply (3 V) for PLL Be sure to connect a 0.1 μF capacitor between this pin and AGND_P.
AGND_P	1H	–	Ground for PLL block
VREF	2E	–	Reference voltage for analog block Be sure to connect a 0.22 μF capacitor between this pin and AGND.
IREF	2D	–	Reference current for analog block Be sure to connect a 56 kΩ resistor between this pin and AGND.

(2) Clock and system control pins

Pin Name	Serial No.	I/O	Function
CLKIN	2H	Input	Clock input This is the reference clock input that is used to generate the internal master clock. Be sure to input using capacitive coupling (1000 pF).
RESET_B	9E	Input	Hardware reset input signal. This resets the μPD9992. Registers are initialized to their initial values after a reset.

(3) Host interface pins **(1/2)**

Pin Name	Pin No.	I/O	Function
A0/Data,TXD	6K	I/O	1. Parallel I/F mode (when PS = 0) Host interface address A0 signal input This input pin indicates the internal register address or data during host CPU access. 1: When transferring data 0: When setting address of internal register to be accessed
			2. Serial I/F mode (when PS = 1) • Bidirectional TX/RX serial data input/output (when PS = 1 and RD_B = 0) In this state, this pin is used in 3-wire SPI mode. • TX serial data output (when PS = 1 and RD_B = 1) In this state, this pin is used in 4-wire SPI mode.
A1/RXD	5J	Input	1. Parallel I/F mode (when PS = 1) Host interface address A1 signal input This input pin selects the access destination register during host CPU access. 1: Sound source block register 0 : Other block register
			2. Serial I/F mode (when PS = 1) RX serial data input (when PS = 1 and RD_B= 1) In this state, this pin is used in 4-wire SPI mode.
CS_B/SCS	6J	Input	1. Parallel I/F mode (when PS =0) Chip select input for parallel I/F This is the input pin for the host interface select signal. This pin is set as active (low) while the host CPU accesses the μPD9992.
			2. Serial I/F mode (when PS = 1) Chip select input for serial I/F
RD_B/SPIMODE	7J	Input	1. Parallel I/F mode (when PS =0) Host read input This pin is set as active (low) while the host CPU reads data of the μPD9992. Do not set this pin and the WR_B pin as active at the same time.
			2. Serial I/F mode (when PS = 1) 3-wire/4-wire SPI mode select 1: 4-wire SPI mode 0: 3-wire SPI mode
WR_B/SCLK	7K	Input	1. Parallel I/F mode (when PS =0) Host write input This pin is set as active (low) while the host CPU writes data to the μPD9992. Do not set this pin and the RD_B pin as active at the same time.
			2. Serial I/F mode (when PS = 1) Clock for serial I/F

(3) Host interface pins **(2/2)**

Pin Name	Pin No.	I/O	Function
D0/SERINIT	8K	I/O	1. Parallel I/F mode (when PS =0) Bit 0 for 8-bit host data bus When the host CPU accesses the μPD9992, resister addresses and data are input/output. When the CS_B signal is inactive (high), this pin is set to high impedance.
			2. Serial I/F mode (when PS = 1) Initialization signal for serial I/F
D1 to D7	8J, 10H, 9H, 10G, 9G, 10F, 9F	I/O	1. Parallel I/F mode (when PS =0) Bits 7-0 for 8-bit host data bus When the host CPU accesses the μPD9992, register addresses and data are input/output. When the CS_B signal is inactive (high), this bus is set to high impedance.
			2. Serial I/F mode (when PS = 1) This bus is always set to high impedance.
INT_B	10E	Output	Host interrupt output This interrupt signal is transmitted from the μPD9992 to the host CPU. This is used when requesting transmit/receive signals during data transfer or internal status notification.
PS	6B	Input	Parallel/serial I/F mode setting 1: Serial I/F mode 0: Parallel I/F mode Pull-down is performed internally.

(4) External LED, motor control output pins

Pin Name	Pin No.	I/O	Function
LED	10C	Output	External LED control output (drive output: See **12.4 DC Characteristics**) This is the port output pin. Settings are entered by writing values to the port setting register from the host CPU. Leave this pin open when not used.
VIB	9D	Output	External motor control output (drive output: See **12.4 DC Characteristics**) This is the port output pin. Settings are entered by writing values to the port setting register from the host CPU. Leave this pin open when not used.

(5) Audio serial interface pins

Pin Name	Pin No.	I/O	Function
BCLK	8B	I/O	Bit synchronization clock I/O for audio serial This pin is used to input or output a clock that is 64 times the sampling frequency (8 kHz, 16 kHz, 32 kHz, 44.1 kHz, or 48 kHz) that has been set as the clock for serial transfers. Connect this pin to GND when not used.
LRCLK	8A	I/O	Audio serial frame synchronization clock I/O This pin is used to input or output a frame sync signal for serial transfers. Connect this pin to GND when not used.
ASO	7B	Output	Audio serial data output The audio serial data's frame size is set via registers. During master mode, either 64 bits or 32 bits can be selected. During slave mode, selections can be made in 2-bit steps within a range from 32 to 64 bits. Leave this pin open when not used.
ASI	7A	Input	Audio serial data input The audio serial data's frame size is set via registers. During master mode, either 64 bits or 32 bits can be selected. During slave mode, selections can be made in 2-bit steps within a range from 32 to 64 bits. Leave this pin open when not used. Pull-down is performed internally.

(6) ADPCM interface pins

Pin Name	Pin No.	I/O	Function
TRSCK	5A	Input	Serial clock input for ADPCM recording Pull-down is performed internally. Leave this pin open when not used.
CLK8K	5B	Input	Synchronization clock input for ADPCM recording Pull-down is performed internally. Leave this pin open when not used.
RDATA	4A	Input	Data input for ADPCM recording Pull-down is performed internally. Leave this pin open when not used.

(7) DAC, line out output pins

Pin Name	Pin No.	I/O	Function
LINEOUT_L	1C	Output	Line out (L ch) output This pin outputs the left-channel analog signal for the line out function.
LINEOUT_R	1F	Output	Line out (R ch) output This pin outputs the right-channel analog signal for the line out function.

(8) General-purpose external output pins

Pin Name	Pin No.	I/O	Function
PO0 to PO3	3K, 3J, 4K, 4J	I/O	General-purpose external output pins This is the port output pin. Settings are entered by writing values to the port setting register from the host CPU. Leave this pin open when not used. These can be used as input pins in the test mode.

(9) Test pins

Pin Name	Pin No.	I/O	Function
TM0 to TM2	2C, 2F, 3B	Input	Input for test Leave open or connect to GND. Pull-down is performed internally.
TM3, TM4	3A, 4B	I/O	I/O for test Leave open.

(10) Others

Pin Name	Pin No.	I/O	Function
N.C	1B, 1J, 2A, 2B, 2J, 2K, 3C, 9B, 9J, 10B	–	Reserved pin for compatibility with future products. Leave this pin open.

1.3 Connection of Unused Pins

It is recommended to connect the unused pins as shown in the table below.

Pin Name	I/O	Recommended Connection
VIB	Output	Leave open.
LED	Output	Leave open.
LRCLK	I/O	Connect to GND.
BCLK	I/O	Connect to GND.
ASI	Input	Leave open.
ASO	Output	Leave open.
TM0 to TM2	Input	Leave open or connect to GND.
TM3, TM4	I/O	Leave open.
TRSCK	Input	Leave open.
CLK8K	Input	Leave open.
RDATA	Input	Leave open.
PO0 to PO3	I/O	Leave open.
★ D1 to D7	I/O	Connect to GND when SPI mode is selected (PS = 1).

1.4 Initial State of Pins

Pin Name	I/O	During Reset	After Reset
VIB	Output	Undefined	Low-level output
LED	Output	Undefined	Low-level output
INT_B	Output	High-level output	High-level output
ASO	Output	Hi-Z	Hi-Z
BCLK	I/O	Hi-Z	Input
LRCLK	I/O	Hi-Z	Input
TM3, TM4	I/O	Hi-Z	Low-level output
PO0 to PO3	I/O	Undefined	Low-level output
D7 to D0	I/O	Hi-Z	Input

1.5 Pin Status

The μPD9992's pin status table is shown below.

(1/2)

Pin No.	I/O	Analog/ Digital	Pin Name	Standby Status		Reset Status (RESET_B = Low)		After Reset
				Control Signal	Pin Status	Control Signal	Pin Status	
2F	Input	Digital	TM1	None	Input	None	Input	Input
2C	Input	Digital	TM0	None	Input	None	Input	Input
1C	Output	Analog	LINEOUT_L	STDAC	Hi-Z	STDAC	Hi-Z	Hi-Z
1D	–	Analog	AGND	–	–	–	–	–
2D	–	Analog	IREF	STREF	Hi-Z	STREF	Hi-Z	Hi-Z
2E	–	Analog	VREF	STERF	Hi-Z	STERF	Hi-Z	Hi-Z
1E	–	Analog	AV_{DD}	–	–	–	–	–
1F	Output	Analog	LINEOUT_R	STDAC	Hi-Z	STDAC	Hi-Z	Hi-Z
1G	–	Analog	AGND	–	–	–	–	–
1H	–	Analog	AGND_P	–	–	–	–	–
2H	Input	Analog	CLKIN	STPLL1&2	Hi-Z	STPLL1&2	Hi-Z	Hi-Z
2G	–	Analog	AV_{DD}_P	–	–	–	–	–
3K	I/O	Digital	PO0	None	**Note 1**	RESET_B	Undefined	Low output[Note2]
3J	I/O	Digital	PO1	None	**Note 1**	RESET_B	Undefined	Low output[Note2]
4K	I/O	Digital	PO2	None	**Note 1**	RESET_B	Undefined	Low output[Note2]
4J	I/O	Digital	PO3	None	**Note 1**	RESET_B	Undefined	Low output[Note2]
5K	–	Digital	DGND	–	–	–	–	–
5J	Input	Digital	A1	None	Input	None	Input	Input
6K	I/O	Digital	A0/Data, TXD	None	Input	None	Input	Input
9K	–	Digital	DV_{DD}	–	–	–	–	–
6J	Input	Digital	CS_B/SCS	None	Input	None	Input	Input
7K	Input	Digital	WR_B/SCLK	None	Input	None	Input	Input
7J	Input	Digital	RD_B/ SPIMODE	None	Input	None	Input	Input
8K	I/O	Digital	D0/SERINIT	None	Input	RESET_B	Hi-Z	Input
8J	I/O	Digital	D1	None	Input	RESET_B	Hi-Z	Input
10H	I/O	Digital	D2	None	Input	RESET_B	Hi-Z	Input
9H	I/O	Digital	D3	None	Input	RESET_B	Hi-Z	Input
10G	I/O	Digital	D4	None	Input	RESET_B	Hi-Z	Input
9G	I/O	Digital	D5	None	Input	RESET_B	Hi-Z	Input
10F	I/O	Digital	D6	None	Input	RESET_B	Hi-Z	Input
9F	I/O	Digital	D7	None	Input	RESET_B	Hi-Z	Input
10J	–	Digital	DGND	–	–	–	–	–
10E	Output	Digital	INT_B	None	Output	RESET_B	High output	High output
9E	Input	Digital	RESET_B	None	Input	None	Input	Input
10D	–	Digital	DV_{DD}	–	–	–	–	–
9D	Output	Digital	VIB	None	**Note 3**	RESET_B	Undefined	Low output[Note2]
10C	Output	Digital	LED	None	**Note 3**	RESET_B	Undefined	Low output[Note2]

Notes 1. Differs according to register setting. See **6.14 Setting of General-Purpose Output Pins (POUT)**.

2. Registers are reset to initial values, so signals with levels corresponding to initial values are output.

3. Differs according to register setting. See **6.13 VIB and LED Settings (VIB)**.

(2/2)

Pin No.	I/O	Analog/ Digital	Pin Name	Standby Status		Reset Status (RESET_B = Low)		After Reset
				Control Signal	Pin Status	Control Signal	Pin Status	
9C	–	Digital	EV_{DD}	–	–	–	–	–
8A	I/O	Digital	LRCLK	STASI, STASO	**Note**	RESET_B	Hi-Z	Input
8B	I/O	Digital	BCLK	STASI, STASO	**Note**	RESET_B	Hi-Z	Input
7A	Input	Digital	ASI	STASI, STASO	**Note**	None	Input	Input
7B	Output	Digital	ASO	STASI, STASO	**Note**	RESET_B	Hi-Z	Hi-Z
6A	–	Digital	EGND	–	–	–	–	–
9A	–	Digital	DV_{DD}	–	–	–	–	–
6B	Input	Digital	PS	None	Input	None	Input	Input
5A	Input	Digital	TRSCK	None	Input	None	Input	Input
5B	Input	Digital	CLK8K	None	Input	None	Input	Input
4A	Input	Digital	RDATA	None	Input	None	Input	Input
4B	I/O	Digital	TM4	STDIG	Low output	RESET_B	Hi-Z	Low output
3A	I/O	Digital	TM3	STDIG	Low output	RESET_B	Hi-Z	Low output
3B	Input	Digital	TM2	None	Input	None	Input	Input

Note For description of the status of the LRCLK, BCLK, ASI, and ASO pins during standby mode, see **Table 1-1**.

Table 1-1. Pin Status in ASIO Block

Pin No.	I/O	Analog/ Digital	Pin Name	MS = 0 (Slave)				MS = 1 (Master)			
				[STASI, STASO]				[STASI, STASO]			
				[0, 0]	[0, 1]	[1, 0]	[1, 1]	[0, 0]	[0, 1]	[1, 0]	[1, 1]
8A	I/O	Digital	LRCLK	Input[Note]	Input	Input	Input	Fixed to low	Output	Output	Output
8B	I/O	Digital	BCLK	Input[Note]	Input	Input	Input	Fixed to low	Output	Output	Output
7A	Input	Digital	ASI	Invalid	Invalid	Input	Input	Invalid	Invalid	Input	Input
7B	Output	Digital	ASO	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output

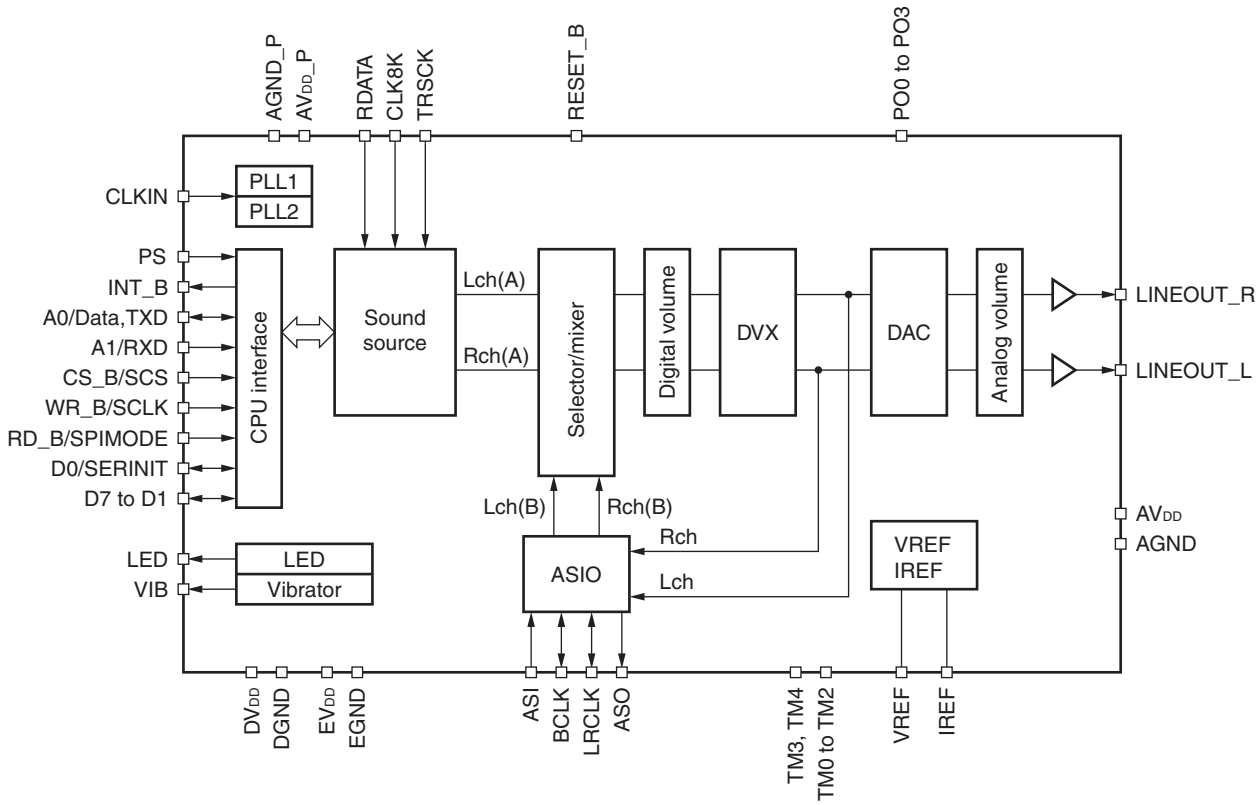
Note Fixed to low level internally

Remarks 1. MS is bit D2 in the SLASI register (08H). See **6.8 ASIO Mode Setting (SLASI)**.

2. STASI and STASO are bits D4 and D3 in the STNBY register (00H). See **6.3 Standby Setting (STNBY)**.

2. GENERAL DESCRIPTION

Figure 2-1. Block Diagram



(1) PLL1, PLL2 (CLKIN pin)

Clock input in the range from 2.688 to 16.128 MHz is supported.

In this block, when a clock with a frequency in this range is input, it is multiplied by the PLL to generate the fixed frequency clock that is required internally. PLL1 generates the clock signals required by all blocks except for the sound source block, and PLL2 generates the clock signal for the sound source block.

(2) CPU interface

This connects to the host CPU via an 8-bit parallel interface or 3/4-wire serial peripheral interface (SPI).

(3) Vibrator, LED control output port

This is an output port for the LEDs and vibrator.

(4) PCM sound source block

A PCM sound source for generation of up to 64 simultaneous tones is on chip, along with a sequencer. The sampling frequency is 32 kHz. The ADPCM's playback function is also on chip. The sampling frequency options are 8 kHz × 4 channels, 16 kHz × 2 channels, and 32 kHz × 1 channel.

(5) Audio serial I/O interface

This is an I/O interface for external audio data.

Five sampling frequency modes are supported: 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz (initial value is 32 kHz).

The serial data input frequency is variable between 32 fs and 64 fs (during slave mode).

(6) Selector/mixer

This block is used to switch among or mix sound sources and audio serial input.

(7) DVX (surround)

This block performs real-time surround processing.

(8) DAC

This block converts digital signals (from sound sources or audio serial input) to analog signals. This DAC (D/A converter) is a high-performance stereo DAC with 16-bit resolution.

3. HOST CPU INTERFACE

Two I/F modes are available: parallel I/F mode and serial I/F mode. The access methods from the host CPU interface are described below.

3.1 Parallel I/F Mode

The parallel I/F mode is entered by setting the PS pin to low level.

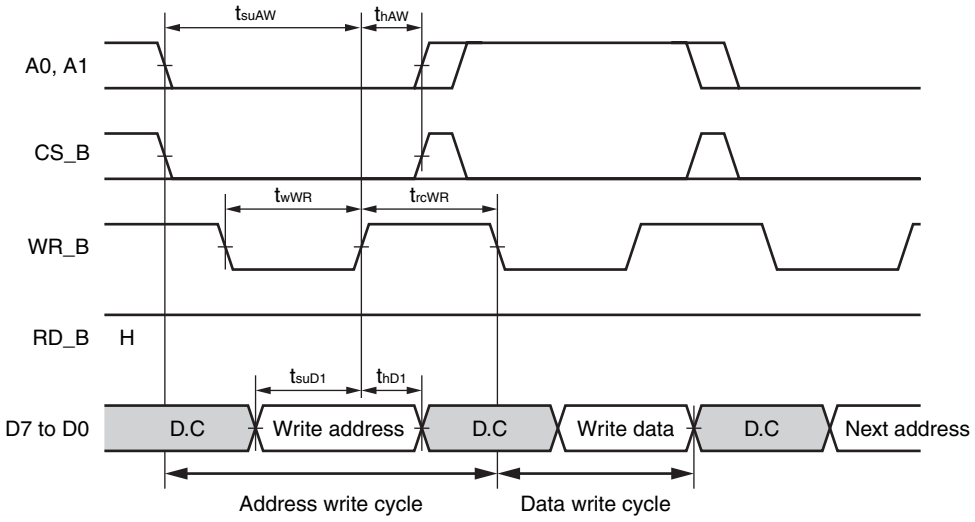
3.1.1 Write access

During write access, data is written to the μPD9992 from the system. The write access timing is shown in Figures 3-1 and 3-2.

- A0 is used to distinguish between address write cycles and data write cycles.
- A1 is used to distinguish between register access for sound sources and register access for other purposes (0: Other than sound source, 1: Sound source).
- In the address write cycle, the data write address is assigned to bits D7 to D0.
- Operation is based on detection of the rising edge of WR_B by the system clock.

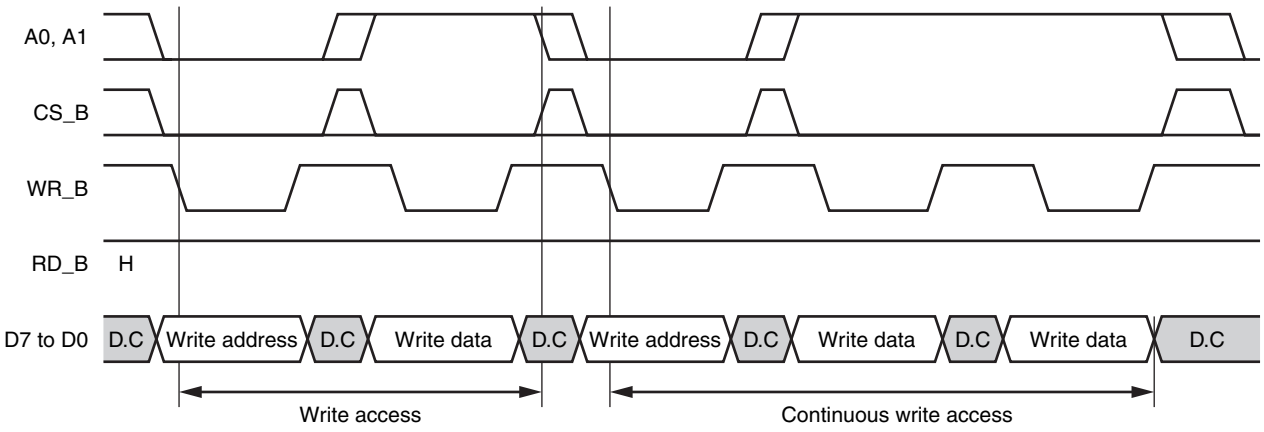
Caution Be sure to fix the RD_B pin to high level during address write cycles and data write cycles.

Figure 3-1. Write Access (Single Access)



Remark Set the CS_B pin to low level during the write period. It is not necessary to always set the CS_B pin to low level during continuous write access.
D.C: Don't care

Figure 3-2. Write Access (Continuous Access)



Remark Set the CS_B pin to low level during the write period. It is not necessary to always set the CS_B pin to low level during continuous write access.
D.C: Don't care

3.1.2 Read Access

During read access, data is read from the system by the μPD9992. The read access timing is shown below.

- A0 is used to distinguish between address write cycles and data read cycles.
- A1 is used to distinguish between register access for sound sources and register access for other purposes (0: Other than sound source, 1: Sound source).
- Operation is based on detection of the rising edge of WR_B and RD_B by the system clock.
- In the address write cycle, the data write address is assigned to bits D7 to D0.

Figure 3-3. Read Access (Single Access)

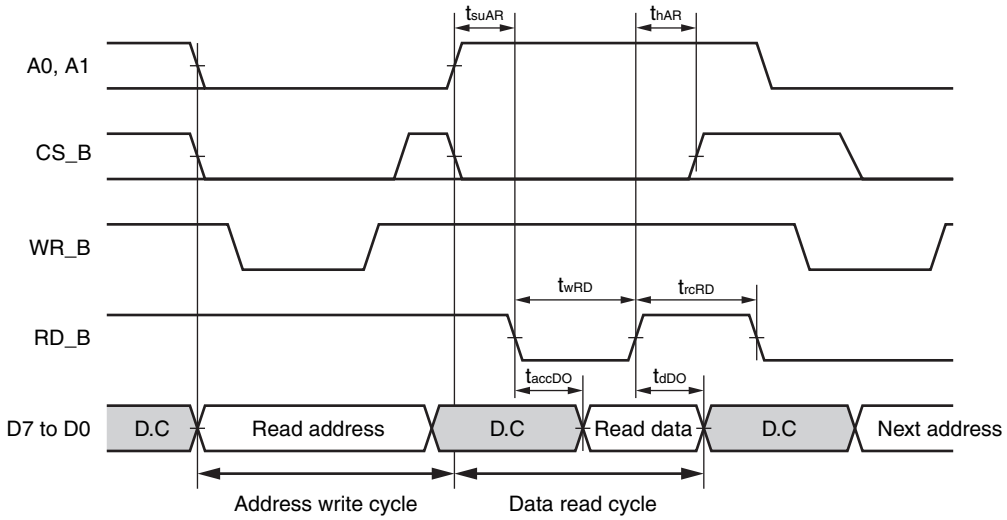
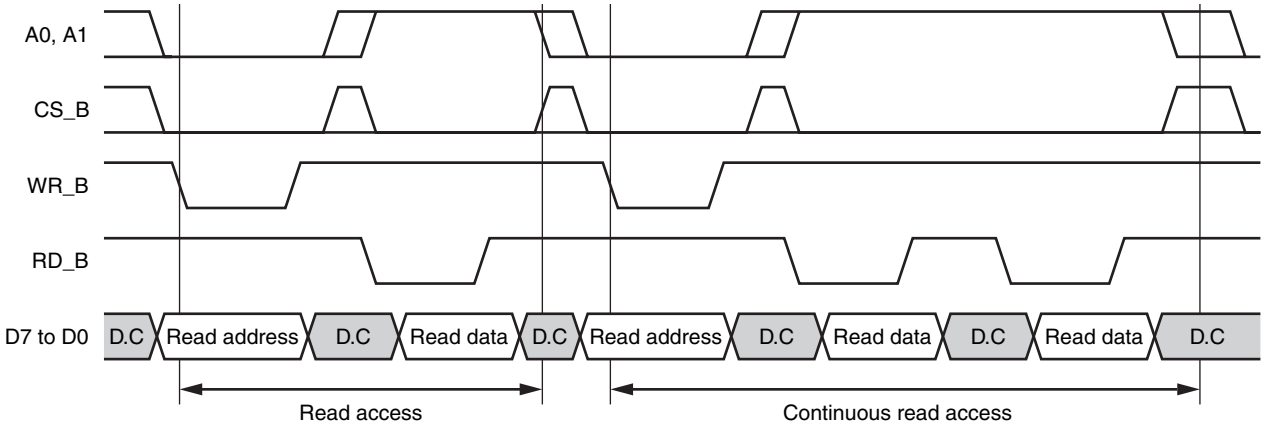


Figure 3-4. Read Access (Continuous Access)



Remark Set the CS_B pin to low level during the read period. It is not necessary to always set the CS_B pin to low level during continuous read access.
D.C: Don't care

3.2 Serial I/F Mode

The serial I/F mode is entered by setting the PS pin to high level. In this mode, there are two communication methods: 3-wire SPI mode and 4-wire SPI mode. The SPIMODE (RD_B) pin is used to switch the SPI modes.

3.2.1 Pin functions

Pin Name	Function	I/O
PS	Selects host CPU interface mode (0: Parallel, 1: Serial)	I
SPIMODE(RD_B)	Selects SPI mode (0: 3-wire SPI mode, 1: 4-wire SPI mode)	I
SCLK (WR_B)	Clock of serial data Maximum frequency is 10 MHz	I
SCS (CS_B)	Chip select signal from host CPU	I
Data,TXD (A0)	Serial TX/RX data from/to host CPU When SPIMODE (RD_B) = 0, this pin is bidirectional. When SPIMODE (RD_B) = 1, this pin is the TXD output.	I/O
RXD (A1)	Serial RX data from host CPU When RD_B = 1, this pin is the RXD input.	I
SERINIT(D0)	Initialization signal for serial I/F When SCS (CS_B) = 1, the serial I/F is asynchronously initialized when SERINIT (D0) = 1. (The initializing condition is SCS = 1 and SERINIT = 1.)	I

Remark ( ) means the pin name in parallel I/F mode.
To use serial interface mode, the PS pin must be high level.
When the SCS pin is high level, the Data,TXD pin will go into a high-impedance state.

3.2.2 Format of serial host CPU interface

Read/Write Control	1 bit	(High: Write access, Low: Read access)
Address	7 bits	
Data	8 bits	
Total	16 bits	

(1) Register area

The μPD9992 has 2 register banks. One is for the wave table synthesizer (Sound Register Bank), and the other is for chip control (Control Register Bank).
Switching is performed by writing a value to a certain specific address (4FH: BANK register).

(2) Access format

- Normal write access
- Normal read access
- Continuous access (1)
- Continuous access (2) for FIFO and DVX RAM

3.2.3 Access format in 3-wire SPI mode

Figure 3-5. Format of Host CPU Access (Period of Read/Write Access)

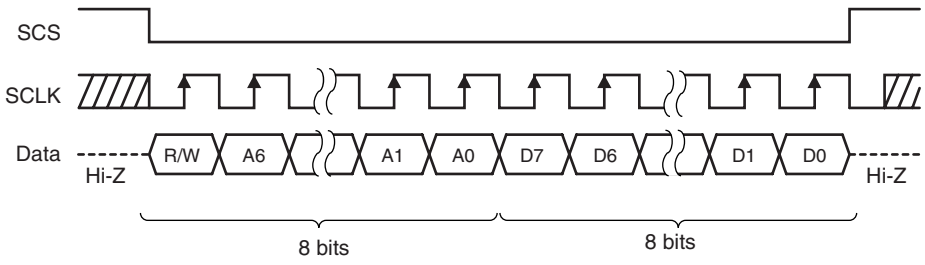
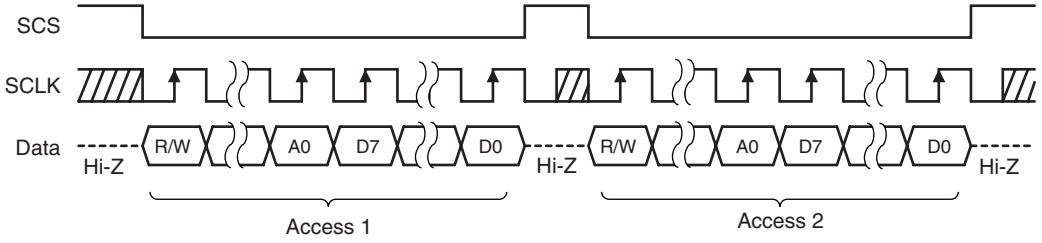
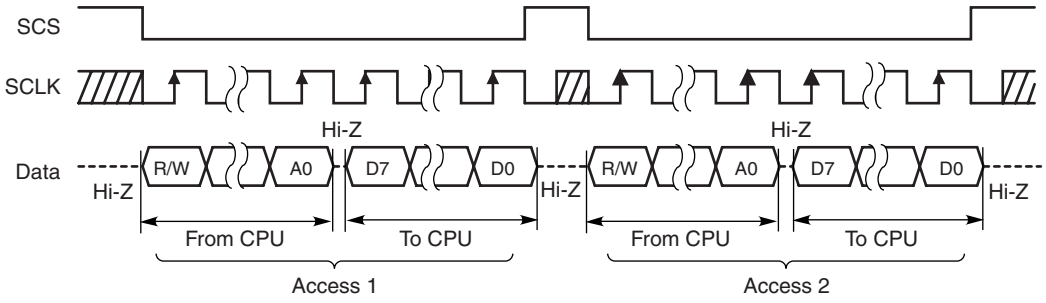


Figure 3-6. Format of Host CPU Access - Continuous Access (1)

(a) Write access

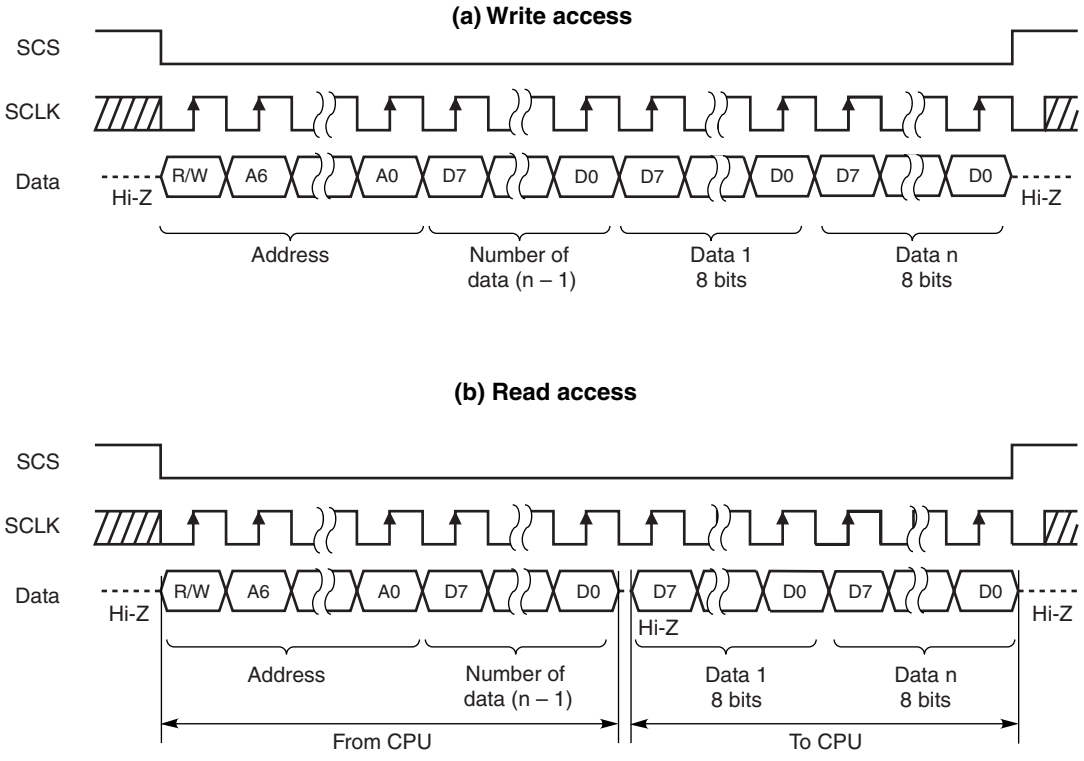


(b) Read access



Remark The above formats are used except when accessing FIFOs in the PCM sound source block and DVX.

Figure 3-7. Format of Host CPU Access - Continuous Access (2)



Remark The above formats are only used to access FIFOs in the PCM sound block and DVX RAM.

3.2.4 Access format in 4-wire SPI mode

Figure 3-8. Format of Host CPU Access (A period of read/write access)

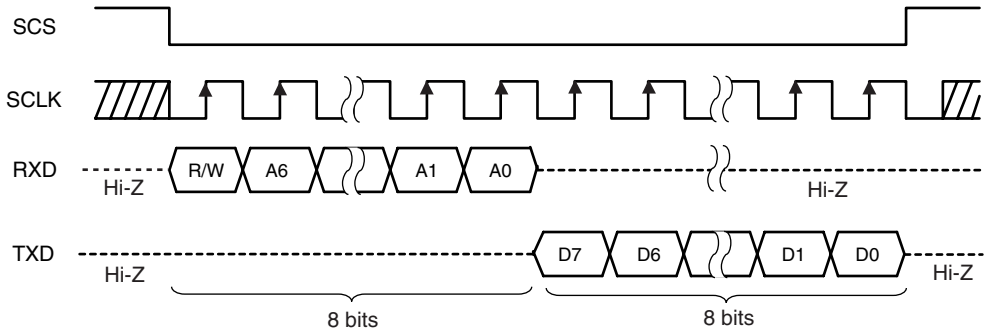
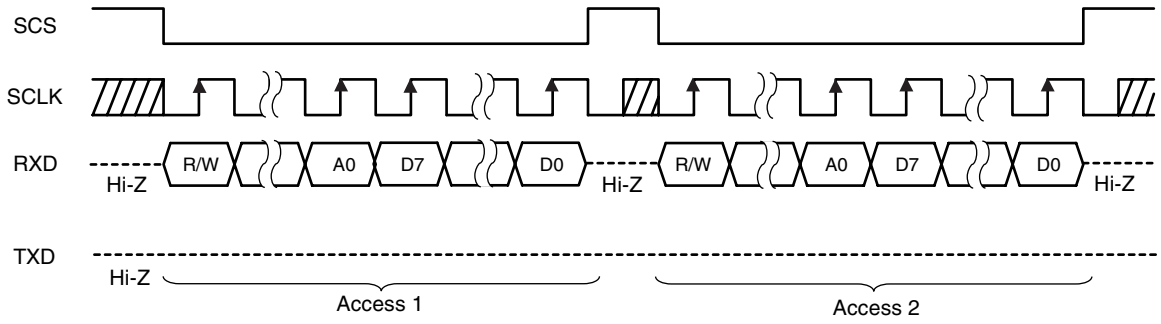
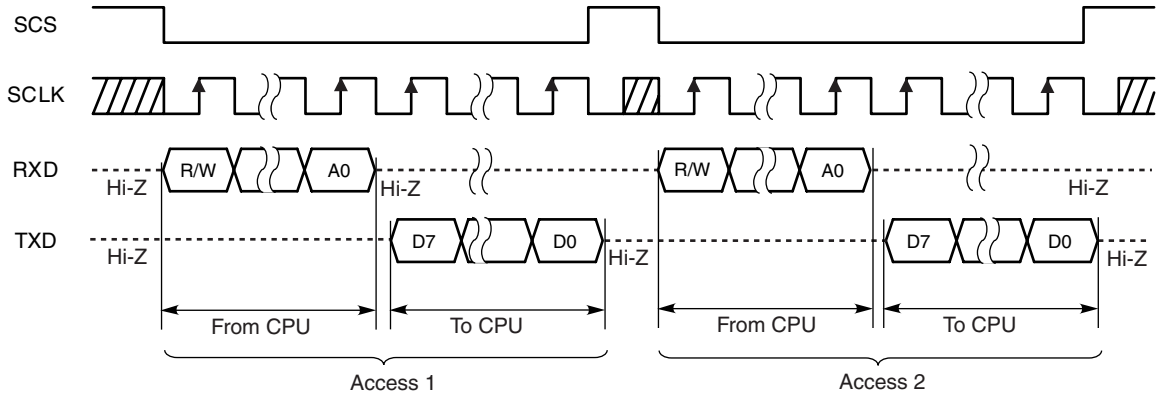


Figure 3-9. Format of Host CPU Access - Continuous Access (1)

(a) Write access



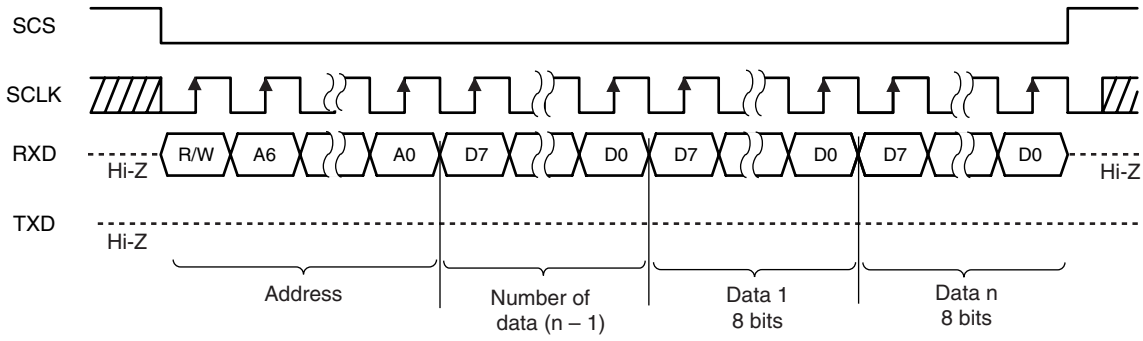
(b) Read access



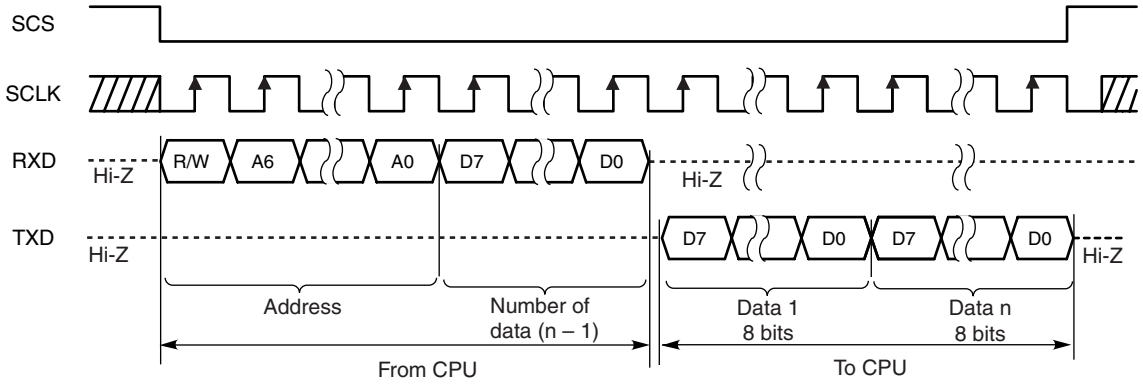
Remark The above formats are used in except when accessing FIFOs in the PCM sound source block and DVX.

Figure 3-10. Format of Host CPU Access - Continuous Access (2)

(a) Write access



(b) Read access



Remark The above formats are only used to access FIFOs in the PCM block and DVX RAM.

3.2.5 Initialization signal for serial I/F

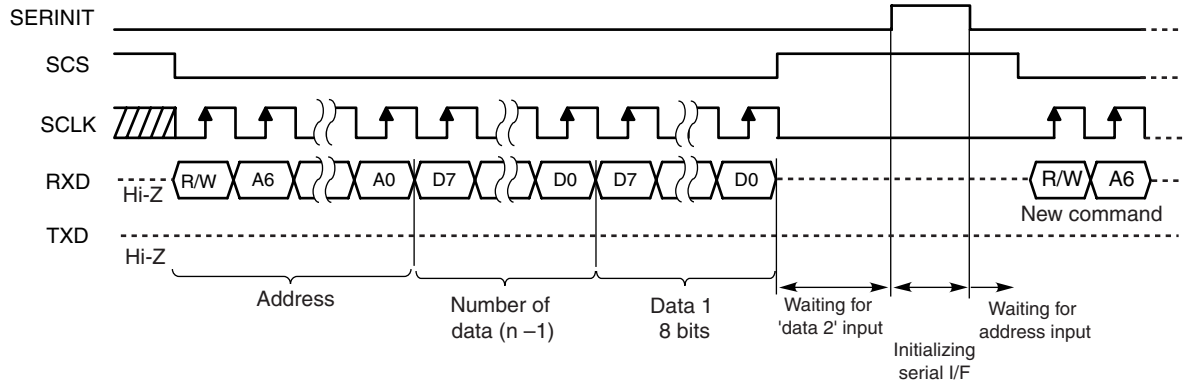
The SERINIT(D0) pin is an initialization signal for the serial I/F and is used for compulsory initialization of serial I/F during write/read continuous access (therefore, this pin is normally used at low level if compulsory initialization is unnecessary).

Compulsory initialization operates only on the serial I/F and is asynchronously performed by setting SCS = 1 and SERINIT = 0. On the other hand, the registers in the Sound Register Bank and the Control Register Bank are not initialized. Therefore the serial I/F waits for a new address to be input after the initialization.

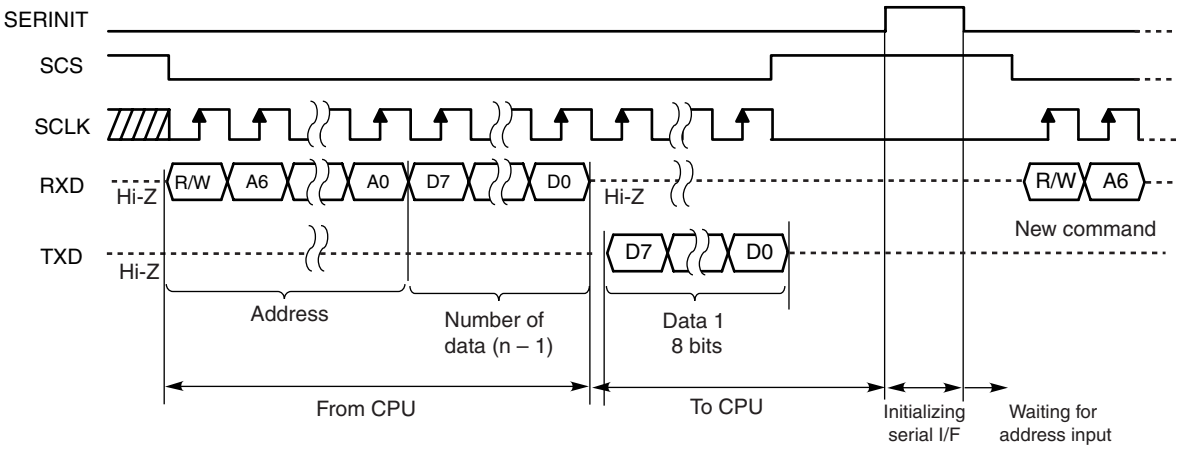
An example of this initialization signal is shown below.

Figure 3-11. Canceling Continuous Access Using SERINIT (D0) Pin

(a) Write access



(b) Read access



Remark The initialization conditions in 3/4-wire mode are the same.

4. AUDIO SERIAL INTERFACE

When LRCLK = 0 in the SLASI register (08H), L-ch data is assigned during the high-level period of LRCLK and R-ch data is assigned during the low-level period of LRCLK. For IIS format, this is reversed, in which case LRCLK = 1 should be set.

Within each of these periods, the format can be switched among right-justified, left-justified, and IIS format. Selection of master mode or slave mode is also enabled. The number of data bits per frame can be set via the BFS[4:0] bits in the SFSL register (07H). The serial input/output timing is shown in Figures 4-1 to 4-3.

Figure 4-1. Right-justified Format

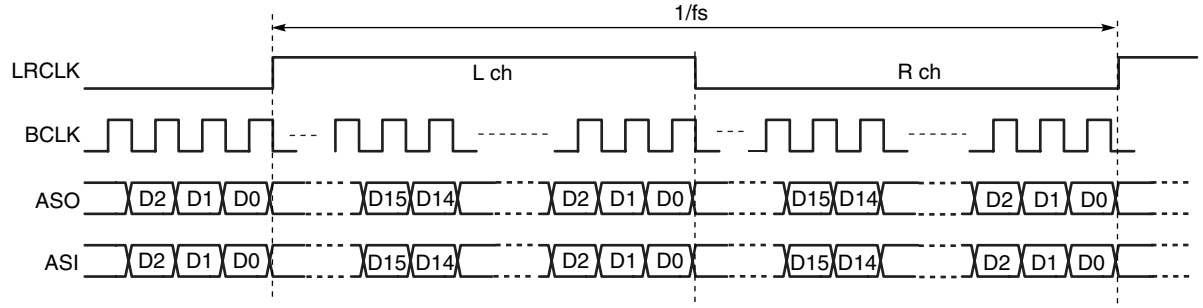


Figure 4-2. Left-justified Format

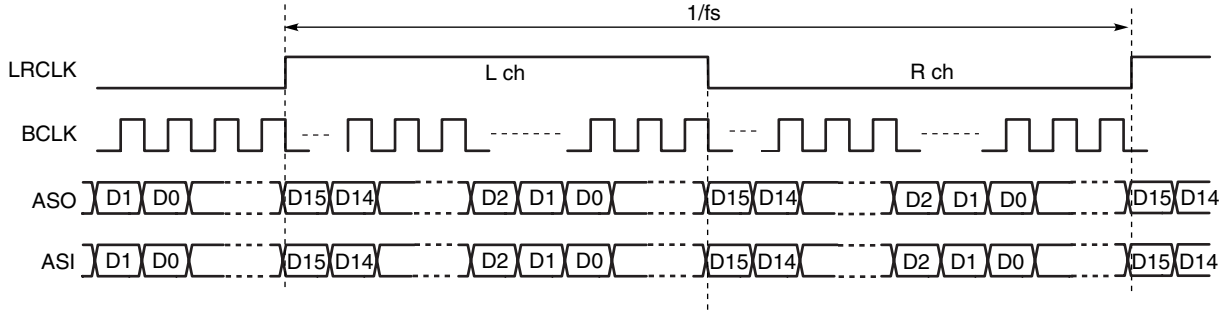
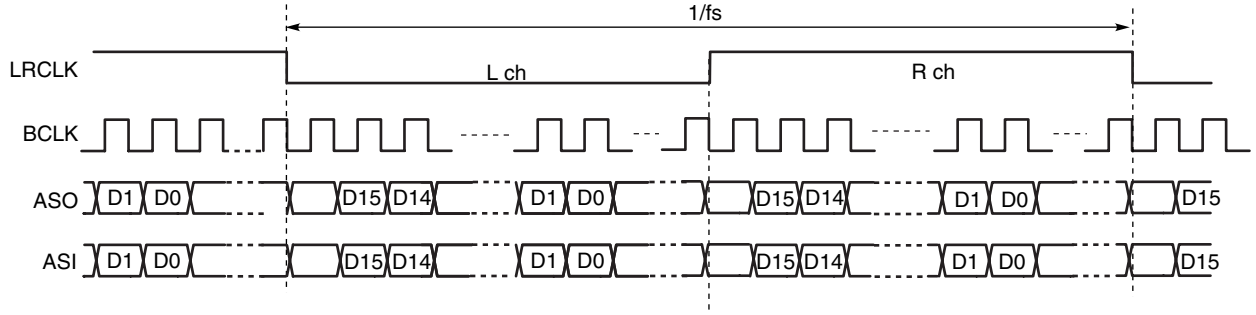


Figure 4-3. IIS Format



Remarks 1. The IIS format is left-justified with one empty bit and sets L-ch to low level and R-ch to high level. Do not specify other settings when selecting IIS mode (ASIM = 1 in SLASI register (08H)). When selecting LR mode (ASIM = 0 in SLASI register (08H)), left or right justification can be selected in combination with normal or reversed left-right format. In both master mode and slave mode, only 64 bits (64 fs) can be selected.

2. When the right-justified format or left-justified format is selected, the number of data bits per frame can be set via the BFS[4:0] bits in the SFSL register (07H).

During master mode, either 64 bits or 32 bits can be selected. During slave mode, any value between 32 bits and 64 bits can be selected in two-bit increments. After a reset is cleared, the default frame configuration setting is 64 bits total (32 bits for L-ch and 32 bits for R-ch).

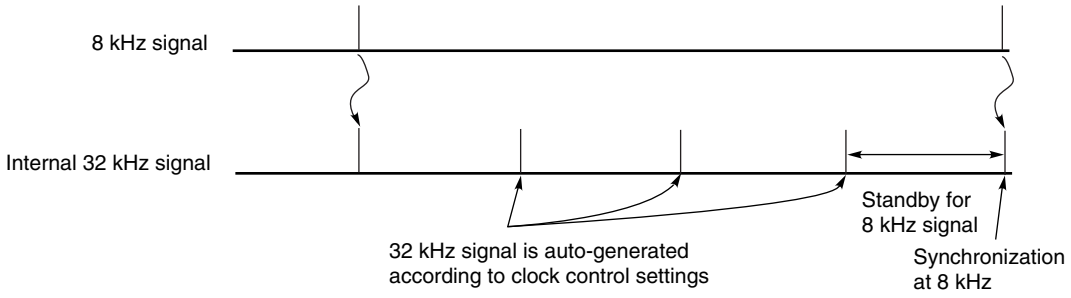
5. ADPCM INPUT INTERFACE

5.1 CLK8K

This is the input pin for the clock signal used for external 8 kHz synchronization when recording. During playback, this clock signal is generated based on a 32 kHz signal generated in the μPD9992, and during recording this signal is generated based on an 8 kHz clock signal input from an external source.

Caution If an 8 kHz synchronization clock signal is not being input from an external source during recording, the recorded data cannot be saved.

Figure 5-1. Synchronization During ADPCM Recording



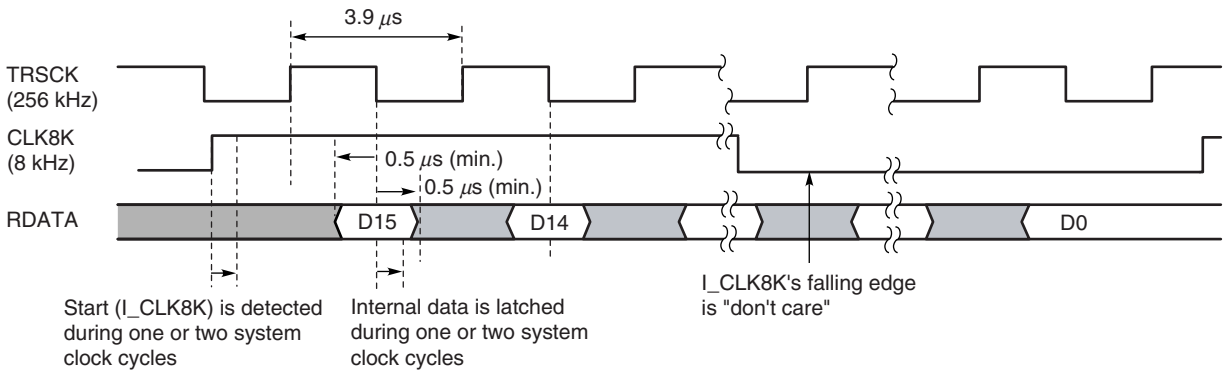
5.2 TRSCK and RDATA

The ADPCM input interface is an external synchronous serial interface used for input and output of linear PCM data.

5.2.1 Serial recording interface

The timing of the external synchronous serial interface is shown below.

Figure 5-2. Timing of External Synchronous Serial Interface



Transfer of ADPCM recorded data is performed in synchronization with an external 8 kHz sync signal and an external serial clock. Latching of data is performed at the falling edge of the serial clock and data is latched MSB first in 16-bit segments. In the case of 16-bit linear PCM data (two's complement format), all 16 bits are valid, but in the case of μ-law 8-bit PCM data, the higher 8 bits are ignored and only the lower 8 bits contain valid data.

Caution Input to the CLK8K pin is detected only at the rising edge.

6. REGISTERS (OTHER THAN SOUND SOURCE REGISTERS)

Registers other than sound source registers are described below.

Caution Information on sound source registers will be disclosed only to parties that have signed an NDA (Non Disclosure Agreement).

6.1 Parallel I/F Mode

The parallel I/F mode is entered when the PS pin is low level.

Table 6-1. List of Control Registers

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H	R/W	STDIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STDAC	STREF	00H	LSI standby setting	STNBY
01H	R/W	0	MCLK1A[6:0]							1CH	Master clock setting 1	MCLK1A
02H	R/W	MCLK1B[7:0]								80H	Master clock setting 1	MCLK1B
03H	R/W	0	0	0	MCLK2A[4:0]					02H	Master clock setting 2	MCLK2A
04H	R/W	MCLK2B[7:0]								29H	Master clock setting 2	MCLK2B
05H	R/W	0	0	0	0	0	0	MIX	SLSORCE	00H	Source input and mixing settings	SLSORCE
06H	R/W	0	0	0	0	0	0	ENSRD[1:0]		00H	Surround	ENSRD
07H	R/W	BFS[4:0]					FS[2:0]			00H	Frequency switching and ASIO BCLK setting	SLFS
08H	R/W	0	0	0	0	SLR	MS	ASIM	LRCLK	00H	ASI setting	SLASI
09H	R/W	0	0	0	DAULGA[4:0]					02H	Digital Volume (L) set value	DAULGA
0AH	R/W	0	0	0	DAURGA[4:0]					02H	Digital Volume (R) set value	DAURGA
0BH	R/W	0	0	0	AAULGA[4:0]					1FH	Analog Volume (L) set value	AAULGA
0CH	R/W	0	0	0	AAURGA[4:0]					1FH	Analog Volume (R) set value	AAURGA
0DH	R/W	0	0	0	0	0	0	VIB	LED	00H	LED and VIB output settings	VIB
0EH	R/W	0	0	0	0	POUT3	POUT2	POUT1	POUT0	00H	User port output setting	POUT
3FH	R	VER[7:0]								**Note**	LSI version	VER
40H	W	SPSRDW1[7:0]								Undefined	SP surround coefficient 1	SPSRDW1
41H	W	SPSRDW2[7:0]								Undefined	SP surround coefficient 2	SPSRDW2
42H	W	HPSRDW1[7:0]								Undefined	HP surround coefficient 1	HPSRDW1
43H	W	HPSRDW2[7:0]								Undefined	HP surround coefficient 2	HPSRDW2
44H	R	SPSRDR1[7:0]								Undefined	SP surround coefficient 1	SPSRDR1
45H	R	SPSRDR2[7:0]								Undefined	SP surround coefficient 2	SPSRDR2
46H	R	HPSRDR1[7:0]								Undefined	HP surround coefficient 1	HPSRDR1
47H	R	HPSRDR2[7:0]								Undefined	HP surround coefficient 2	HPSRDR2
48H	R/W	SRDRA[7:0]								00H	Surround mode setting	SRDRA

Note Differs according to the LSI version.

Caution Do not access addresses other than those listed in Table 6-1.

6.2 Serial I/F Mode

The serial I/F mode is entered when the PS pin is high level.

6.2.1 Sound register bank

The register map is as follows when the BANK register is 00H.

Table 6-2. Sound Register Bank

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H : 4EH	**Register for Sound Source**											
4FH	R/W	0	0	0	0	0	0	0	BANK	01H	BANK register	BANK
50H : 7FH	**Register for Sound Source**											

6.2.2 Control register bank

The register map is as follows when the BANK register is 01H.

Table 6-3. Control Register Bank

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H	R/W	STDIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STDAC	STREF	00H	LSI standby setting	STNBY
01H	R/W	0	MCLK1A[6:0]							1CH	Master clock setting 1	MCLK1A
02H	R/W	MCLK1B[7:0]								80H	Master clock setting 1	MCLK1B
03H	R/W	0	0	0	MCLK2A[4:0]					02H	Master clock setting 2	MCLK2A
04H	R/W	MCLK2B[7:0]								29H	Master clock setting 2	MCLK2B
05H	R/W	0	0	0	0	0	0	MIX	SLSORCE	00H	Source input and mixing settings	SLSORCE
06H	R/W	0	0	0	0	0	0	ENSRD[1:0]		00H	Surround	ENSRD
07H	R/W	BFS[4:0]					FS[2:0]			00H	Frequency switching and ASIO BCLK setting	SLFS
08H	R/W	0	0	0	0	SLR	MS	ASIM	LRCLK	00H	ASI setting	SLASI
09H	R/W	0	0	0	DAULGA[4:0]					02H	Digital volume (L) set value	DAULGA
0AH	R/W	0	0	0	DAURGA[4:0]					02H	Digital volume (R) set value	DAURGA
0BH	R/W	0	0	0	AAULGA[4:0]					1FH	Analog volume (L) set value	AAULGA
0CH	R/W	0	0	0	AAURGA[4:0]					1FH	Analog volume (R) set value	AAURGA
0DH	R/W	0	0	0	0	0	0	VIB	LED	00H	LED and VIB output settings	VIB
0EH	R/W	0	0	0	0	POUT3	POUT2	POUT1	POUT0	00H	User port output setting	POUT
3FH	R	VER[7:0]								**Note**	LSI version	VER
40H	W	SPSRDW1[7:0]								Undefined	SP surround coefficient 1	SPSRDW1
41H	W	SPSRDW2[7:0]								Undefined	SP surround coefficient 2	SPSRDW2
42H	W	HPSRDW1[7:0]								Undefined	HP surround coefficient 1	HPSRDW1
43H	W	HPSRDW2[7:0]								Undefined	HP surround coefficient 2	HPSRDW2
44H	R	SPSRDR1[7:0]								Undefined	SP surround coefficient 1	SPSRDR1
45H	R	SPSRDR2[7:0]								Undefined	SP surround coefficient 2	SPSRDR2
46H	R	HPSRDR1[7:0]								Undefined	HP surround coefficient 1	HPSRDR1
47H	R	HPSRDR2[7:0]								Undefined	HP surround coefficient 2	HPSRDR2
48H	R/W	SRDRA[7:0]								00H	Surround mode setting	SRDRA
:												
4FH	R/W	0	0	0	0	0	0	0	BANK	01H	BANK register	BANK
50H	–	Reserved										
:												
7FH	–											

Note Differs according to the LSI version.

Caution Do not access addresses other than those listed in Table 6-3.

6.3 Standby Setting (STNBY)

This register sets standby mode.

Address: 00H, register name: STNBY, block: general, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
STDIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STDAC	STREF

6.3.1 STDIG

Data	Mode	Initial Value	Description
0	Standby	0	Standby for digital block
1	ON		Normal operation

6.3.2 STPLL2

Data	Mode	Initial Value	Description
0	Standby	0	Standby for PLL2
1	ON		Normal operation

Remark During PLL2 standby mode (power down), the PLL2 output clock is stopped.

6.3.3 STPLL1

Data	Mode	Initial Value	Description
0	Standby	0	Standby for PLL1
1	ON		Normal operation

Remark During PLL1 standby mode (power down), the PLL1 output clock is stopped.

6.3.4 STASI

Data	Mode	Initial Value	Description
0	Standby	0	Standby for audio serial interface input (ASI)
1	ON		Normal operation

6.3.5 STASO

Data	Mode	Initial Value	Description
0	Standby	0	Standby for audio serial interface output (ASO)
1	ON		Normal operation

Caution LRCLK and BCLK operate in standby mode only when both the STASI and STASO bits have been set for standby. For details, see Table 1-1. Pin Status in ASIO Block.

6.3.6 STSYNTH

Data	Mode	Initial Value	Description
0	Standby	0	Standby for sound source block (Synthesizer)
1	ON		Normal operation

6.3.7 STDAC

Data	Mode	Initial Value	Description
0	Standby	0	Standby for DAC block[Note]
1	ON		Normal operation

Note This standby signal is shared by the DAC analog block and the analog volume function.

6.3.8 STREF

Data	Mode	Initial Value	Description
0	Standby	0	Standby for voltage/current reference block[Note]
1	ON		Normal operation

Note This is the standby signal for the analog block's voltage reference and current reference sources.

6.4 Master Clock Switching (MCLK1A, MCLK1B, MCLK2A, MCLK2B)

These registers set master clock 1 and master clock 2.

Address: 01H, register name: MCLK1A, block: PLL1, access: R/W, initial value: 1CH

D7	D6	D5	D4	D3	D2	D1	D0
0	MCLK1A[6:0]						

Address: 02H, register name: MCLK1B, block: PLL1, access: R/W, initial value: 80H

D7	D6	D5	D4	D3	D2	D1	D0
MCLK1B[7:0]							

Address: 03H, register name: MCLK2A, block: PLL2, access: R/W, initial value: 02H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	MCLK2A[4:0]				

Address: 04H, register name: MCLK2B, block: PLL2, access: R/W, initial value: 29H

D7	D6	D5	D4	D3	D2	D1	D0
MCLK2B[7:0]							

6.4.1 MCLK1A[6:0]

Data	Mode	Initial Value	Description
MCLK1A[6:0]		1CH	Sets PLL1, used to generate the audio master clock.

6.4.2 MCLK1B[7:0]

Data	Mode	Initial Value	Description
MCLK1B[7:0]		80H	Sets PLL1, used to generate the audio master clock.

6.4.3 MCLK2A[4:0]

Data	Mode	Initial Value	Description
MCLK2A[4:0]		02H	Sets PLL2, used to generate the sound source master clock.

6.4.4 MCLK2B[7:0]

Data	Mode	Initial Value	Description
MCLK2B[7:0]		29H	Sets PLL2, used to generate the sound source master clock.

Master clock setting examples are shown below.

(1) Audio master clock setting

This sets the clock frequency supplied to all blocks except the sound source block. Be sure to set the MCLK1A and MCLK1B registers according to the input clock frequency and sampling frequency. The input clock signal is first divided by the value set to the MCLK1A register and is then multiplied by the value set to the MCLK1B register.

(a) Divided clock

100 kHz < (CLKIN / MCLK1A) < 250 kHz

(b) Target audio master clock

22.579200 MHz (Target clock at 44.1 kHz)

24.576000 MHz (Target clock at 8 kHz/16 kHz/32 kHz/48 kHz)

(c) Clock calculation

(Calculated clock) = (CLKIN / MCLK1A) *MCLK1B

(d) Acceptable error

–0.02 %(–2.0E–4) < (Acceptable error) < 0.02 %(2.0E–4)

(e) Example

When CLKIN = 13 MHz, MCLK1A = 76 (Dec), MCLK1B = 132 (Dec), fs = 44.1 kHz

(a) -> (CLKIN / MCLK1A) = 171.053 kHz

(c) -> (CLKIN / MCLK1A) *MCLK1B = 22.578947 MHz

(d) -> (22.578947E6 – 22.5792E6) / 22.5792E6 = –0.0011 %

CLKIN Input Frequency [MHz]	MCLK1A		MCLK1B		Sampling Frequency fs [kHz]
	(Dec)	(HEX)	(Dec)	(HEX)	
2.688	20	14	168	A8	44.1
5.376	40	28	168	A8	44.1
12.000	76	4C	143	8F	44.1
12.600	77	4D	138	8A	44.1
13.000	76	4C	132	84	44.1
14.400	125	7D	196	C4	44.1
16.128	120	78	168	A8	44.1
2.688	14	0E	128	80	48
5.376	28	1C	128	80	48
12.000	62	3E	127	7F	48
12.600	81	51	158	9E	48
13.000	64	40	121	79	48
14.400	75	4B	128	80	48
16.128	84	54	128	80	48
2.688	14	0E	128	80	32
5.376	28	1C	128	80	32
12.000	62	3E	127	7F	32
12.600	81	51	158	9E	32
13.000	64	40	121	79	32
14.400	75	4B	128	80	32
16.128	84	54	128	80	32
2.688	14	0E	128	80	8
5.376	28	1C	128	80	8
12.000	62	3E	127	7F	8
12.600	81	51	158	9E	8
13.000	64	40	121	79	8
14.400	75	4B	128	80	8
16.128	84	54	128	80	8
2.688	14	0E	128	80	16
5.376	28	1C	128	80	16
12.000	62	3E	127	7F	16
12.600	81	51	158	9E	16
13.000	64	40	121	79	16
14.400	75	4B	128	80	16
16.128	84	54	128	80	16

(2) Sound source master clock setting

This sets the frequency of the clock to be supplied to the sound source block. Be sure to set values in the MCLK2A and MCLK2B registers according to the input clock frequency. The input clock signal is first divided by the ★ value set to the MCLK2A register and is then multiplied by the value set to the MCLK2B register. Also, sets sampling frequency as 32 kHz when using the sound source.

(a) Divided clock

2 MHz < (CLKIN / MCLK2A) < 3 MHz

(b) Target sound source master clock

54.5 MHz < (Target clock at 32 kHz) < 55.5 MHz

(c) Clock calculation

(Calculated clock) = (CLKIN / MCLK2A) *MCLK2B / 2

(d) Acceptable error

–0.03 %(–3.0E–4) < (Acceptable error of 32 kHz sampling clock) < 0.03 %(3.0E–4)

(e) Example

When CLKIN = 13 MHz, MCLK2A = 5 (Dec), MCLK2B = 42 (Dec), fs = 32 kHz

(a) -> (CLKIN / MCLK2A) = 2.6 MHz

(b),(c)->(CLKIN / MCLK2A)*MCLK2B / 2 = 54.6 MHz

(d) -> 54.6 MHz / 32 kHz = 1706.25 (Division ratio is 1706)

54.6 MHz / 1706 = 32004.7 Hz

(32004.7 − 32000)/32000 = 0.0147%

★

CLKIN Input Frequency [MHz]	MCLK2A		MCLK2B		Master clock frequency for sound source [MHz]
	(Dec)	(HEX)	(Dec)	(HEX)	
2.688	1	01	41	29	55.10400
5.376	2	02	41	29	55.10400
12.000	5	05	46	2E	55.20000
12.600	5	05	44	2C	55.44000
13.000	5	05	42	2A	54.60000
14.400	6	06	46	2E	55.20000
16.128	6	06	41	29	55.10400

6.5 Switching/Mixing of Surround Block Input Source (SLSORCE)

This register is used to set switching and mixing of the surround block's input source.

Address: 05H, register name: SLSORCE, block: Selector, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	MIX	SLSORCE

6.5.1 SLSORCE

Data	Mode	Initial Value	Description
0	SYNTH	0	Select input from sound source (synthesizer)
1	ASI		Select input from audio serial interface input (ASI)

6.5.2 MIX

Data	Mode	Initial Value	Description
0	Path selection	0	Path is used for output from either the sound source or ASI (set via SLSORCE).
1	Mixing		Mixes sound source and ASI signals (SLSORCE setting is invalid).

Cautions 1. Mixing mode is supported only when the sampling frequency is 32 kHz. Consequently, when setting MIX = 1, be sure to set the FS[2:0] bits of the SLFS register (07H) to 000B (see 6.7 Fs Setting and BCLK Setting for ASIO (SLFS)).

2. If the sum of the sound source and the ASI signal exceeds the full scale, the output signal will be clipped.

3. When setting the MIX bit to 1 while ASIO is in slave mode (MS bit of SLASI register = 1 (08H)), be sure to set the STASI bit and STASO bit of the STNBY register (00H) to 1 and input BCLK and LRCLK.

6.6 Surround On/Off Switching (ENSRD)

This switches the surround function on and off.

Address: 06H, register name: ENSRD, block: DVX, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	ENSRD[1:0]	

6.6.1 ENSRD[1:0]

Data	Mode	Initial Value	Description
00B	OFF	00B	Surround processing is not performed (surround coefficient read/write enabled).
01B	SPK		The coefficient set to the SP's coefficient setting registers (addresses 40H and 41H) is used to perform surround processing.
10B	HP		The coefficient set to the HP's coefficient setting registers (addresses 42H and 43H) is used to perform surround processing.
11B	–		Setting prohibited

Caution Reading or writing of the surround coefficient is enabled only when ENSRD[1:0] = 00B.

6.7 Fs Setting and BCLK Setting for ASIO (SLFS)

This sets the ASI's sampling rate and the frequency of BCLK.

Address: 07H, register name: SLFS, block: ASIO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
BFS[4:0]					FS[2:0]		

6.7.1 FS[2:0]

Data	Mode	Initial Value	Description
000B	32 kHz	000B	Sets ASIO's sampling rate as 32 kHz.
001B	44.1 kHz		Sets ASIO's sampling rate as 44.1 kHz.
010B	48 kHz		Sets ASIO's sampling rate as 48 kHz.
100B	8 kHz		Sets ASIO's sampling rate as 8 kHz.
101B	16 kHz		Sets ASIO's sampling rate as 16 kHz.

Caution Be sure to set this in tandem with the master clock setting (set for each sampling frequency). Do not set any data that is not shown above.

6.7.2 BFS[4:0]

Data	Mode	Initial Value	Description
00H	64 fs	00H	Sets 64 fs as BCLK frequency (can be set during master mode).
01H	62 fs		Sets 62 fs as BCLK frequency.
02H	60 fs		Sets 60 fs as BCLK frequency.
03H	58 fs		Sets 58 fs as BCLK frequency.
04H	56 fs		Sets 56 fs as BCLK frequency.
05H	54 fs		Sets 54 fs as BCLK frequency.
06H	52 fs		Sets 52 fs as BCLK frequency.
07H	50 fs		Sets 50 fs as BCLK frequency.
08H	48 fs		Sets 48 fs as BCLK frequency.
09H	46 fs		Sets 46 fs as BCLK frequency.
0AH	44 fs		Sets 44 fs as BCLK frequency.
0BH	42 fs		Sets 42 fs as BCLK frequency.
0CH	40 fs		Sets 40 fs as BCLK frequency.
0DH	38 fs		Sets 38 fs as BCLK frequency.
0EH	36 fs		Sets 36 fs as BCLK frequency.
0FH	34 fs		Sets 34 fs as BCLK frequency.
10H	32 fs		Sets 32 fs as BCLK frequency (can be set during master mode).

Caution During master mode (MS = 1), only 64 fs (00H) or 32 fs (10H) can be set. If any other value is set, 64 fs (the initial value) will be selected.

During slave mode (MS = 0), any sampling frequency from 32 fs to 64 fs can be set in 2 fs increments.

In both master mode and slave mode in the IIS format, only 64 bits (64fs) can be selected.

6.8 ASIO Mode Setting (SLASI)

This specifies the ASI setting as shown below.

Address: 08H, register name: SLASI, block: ASIO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SLR	MS	ASIM	LRCLK

6.8.1 SLR

Data	Mode	Initial Value	Description
0	SR	0	Right-justified format
1	SL		Left-justified format

6.8.2 MS

Data	Mode	Initial Value	Description
0	SLAVE	0	Slave mode
1	MASTER		Master mode

Caution During slave mode, external clock input is required. For description of the pin status of the ASIO block during various modes, see 1.5 Pin Status.

6.8.3 ASIM

Data	Mode	Initial Value	Description
0	LR	0	LR mode
1	IIS		IIS mode (In this case, the SLR bit is a “don’t care” bit).

6.8.4 LRCLK

Data	Mode	Initial Value	Description
0	LCH	0	When LRCLK is at high level, this specifies L channel data.
1	RCH		When LRCLK is at high level, this specifies R channel data.

Caution Be sure to set LRCLK = 1 when IIS mode is selected.

6.9 Digital Volume (L) Setting (DAULGA)

This sets the L channel's digital gain.

Address: 09H, register name: DAULGA, block: Digital Volume, access: R/W, initial value: 02H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DAULGA[4:0]				

6.9.1 DAULGA[4:0]

Data	Mode	Initial Value	Description
DAULGA[4:0]		02H	Sets digital gain (L ch)

6.10 Digital Volume (R) Setting (DAURGA)

This sets the R channel's digital gain.

Address: 0AH, register name: DAURGA, block: Digital Volume, access: R/W, initial value: 02H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DAURGA[4:0]				

6.10.1 DAURGA[4:0]

Data	Mode	Initial Value	Description
DAURGA[4:0]		02H	Sets digital gain (R ch)

Table 6-1. Digital Volume (5-Bit Non-Linear)

Gain	DAULGA[4:0]/ DAURGA[4:0]	Gain	DAULGA[4:0]/ DAURGA[4:0]
+12 dB	00H	–30 dB	0CH
+6 dB	01H	–33 dB	0DH
±0 dB	02H (Initial value)	–36 dB	0EH
–3 dB	03H	–39 dB	0FH
–6 dB	04H	–42 dB	10H
–9 dB	05H	–45 dB	11H
–12 dB	06H	–48 dB	12H
–15 dB	07H	–51 dB	13H
–18 dB	08H	–54 dB	14H
–21 dB	09H	–57 dB	15H
–24 dB	0AH	–60 dB	16H
–27 dB	0BH	Mute	17H

6.11 Analog Volume (L ch) Setting (AAULGA)

This sets the L channel's analog gain.

Address: 0BH, register name: AAULGA, block: Analog Volume, access: R/W, initial value: 1FH

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	AAULGA[4:0]				

6.11.1 AAULGA[4:0]

Data	Mode	Initial Value	Description
AAULGA[4:0]		1FH	Sets analog gain (L ch)

6.12 Analog Volume (R ch) Setting (AAURGA)

This sets the R channel's analog gain.

Address: 0CH, register name: AAURGA, block: Analog Volume, access: R/W, initial value: 1FH

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	AAURGA[4:0]				

6.12.1 AAURGA[4:0]

Data	Mode	Initial Value	Description
AAURGA[4:0]		1FH	Sets analog gain (R ch)

Table 6-2. Analog Volume (5-Bit Linear)

Gain	AAULGA[4:0] / AAURGA[4:0]
±0 dB	00H
–1.5 dB	01H
–3 dB	02H
–4.5 dB	03H
–6 dB	04H
–7.5 dB	05H
–9 dB	06H
–10.5 dB	07H
–12 dB	08H
–13.5 dB	09H
–15 dB	0AH
–16.5 dB	0BH
–18 dB	0CH
–19.5 dB	0DH
–21 dB	0EH
–22.5 dB	0FH

Gain	AAULGA[4:0] / AAURGA[4:0]
–24 dB	10H
–25.5 dB	11H
–27 dB	12H
–28.5 dB	13H
–30 dB	14H
–31.5 dB	15H
–33 dB	16H
–34.5 dB	17H
–36 dB	18H
–37.5 dB	19H
–39 dB	1AH
–40.5 dB	1BH
–42 dB	1CH
–43.5 dB	1DH
–45 dB	1EH
Mute	1FH (Initial value)

6.13 VIB and LED Settings (VIB)

This register is used to control the output port for the vibrator and LED.

Address: 0DH, register name: VIB, block: Analog Volume, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	VIB	LED

6.13.1 LED

Data	Mode	Initial Value	Description
0	LOW	0	Low-level output from LED pin
1	HIGH		High-level output from LED pin

6.13.2 VIB

Data	Mode	Initial Value	Description
0	LOW	0	Low-level output from VIB pin
1	HIGH		High-level output from VIB pin

Caution For both LED and VIB, the register value is output to the μPD9992's pins.

6.14 Setting of General-Purpose Output Pins (POUT)

This sets the output level for the general-purpose output pins (pins PO0 to PO3).

Address: 0EH, register name: POUT, block: PO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	POUT3	POUT2	POUT1	POUT0

6.14.1 POUT0 to POUT3

Data	Mode	Initial Value	Description
0	LOW	0	Low-level output from corresponding pins PO0 to PO3.
1	HIGH		High-level output from corresponding pins PO0 to PO3.

6.15 LSI Version (VER)

This displays the LSI's version information.

Address: 3FH, register name: VER, block: other, access: R, initial value: differs depending on LSI version

D7	D6	D5	D4	D3	D2	D1	D0
VER[7:0]							

6.15.1 VER[7:0]

Data	Mode	Initial Value	Description
VER[7:0]		–	LSI version

6.16 Surround Coefficient Write Register (for Speaker) (SPSRDW1, SPSRDW2)

This register is used to write the surround coefficient for the speaker.

Address: 40H, register name: SPSRDW1, block: DVX, access: W, initial value: undefined

D7	D6	D5	D4	D3	D2	D1	D0
SPSRDW1[7:0]							

Address: 41H, register name: SPSRDW2, block: DVX, access: W, initial value: undefined

D7	D6	D5	D4	D3	D2	D1	D0
SPSRDW2[7:0]							

6.16.1 SPSRDW1[7:0]

Data	Mode	Initial Value	Description
SPSRDW1[7:0]		Undefined	Surround coefficient setting register 1 (for speaker)

6.16.2 SPSRDW2[7:0]

Data	Mode	Initial Value	Description
SPSRDW2[7:0]		Undefined	Surround coefficient setting register 2 (for speaker)

6.17 Surround Coefficient Write Register (for Headphones) (HPSRDW1, HPSRDW2)

This register is used to write the surround coefficient for the headphones.

Address: 42H, register name: HPSRDW1, block: DVX, access: W, initial value: undefined

D7	D6	D5	D4	D3	D2	D1	D0
HPSRDW1[7:0]							

Address: 43H, register name: HPSRDW2, block: DVX, access: W, initial value: undefined

D7	D6	D5	D4	D3	D2	D1	D0
HPSRDW2[7:0]							

6.17.1 HPSRDW1[7:0]

Data	Mode	Initial Value	Description
HPSRDW1[7:0]		Undefined	Surround coefficient setting register 1 (for headphones)

6.17.2 HPSRDW2[7:0]

Data	Mode	Initial Value	Description
HPSRDW2[7:0]		Undefined	Surround coefficient setting register 2 (for headphones)

Cautions 1. To access the surround coefficient write registers (40H, 41H, 42H, and 43H), first write to the surround address setting register, then continuously write data 192 times. Writing the data 192 times sets values to the RAM that stores internal surround coefficients.

2. The surround coefficient must be written using continuous write access. Even if the CS_B pin goes to high level during the continuous write operation and the CPU control switches to another device, the surround coefficient is written without any problem if it is accessed following the previous write operation when the CS_B pin goes to low level.

3. If an interrupt (INT_B) occurs while data is being written continuously, start over by writing the surround mode setting register again.

4. Reading and writing of surround coefficients are enabled only when ENSRD[1:0] = 00B.

6.18 Surround Coefficient Read Register (for Speaker) (SPSRDR1, SPSRDR2)

This register is used to read the surround coefficient for the speaker.

Address: 44H, register name: SPSRDR1, block: DVX, access: R, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
SPSRDR1[7:0]							

Address: 45H, register name: SPSRDR2, block: DVX, access: R, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
SPSRDR2[7:0]							

6.18.1 SPSRDR1[7:0]

Data	Mode	Initial Value	Description
SPSRDR1[7:0]		Undefined	Surround coefficient setting register 1 (for speaker)

6.18.2 SPSRDR2[7:0]

Data	Mode	Initial Value	Description
SPSRDR2[7:0]		Undefined	Surround coefficient setting register 2 (for speaker)

6.19 Surround Coefficient Read Register (for Headphones) (HPSRDR1, HPSRDR2)

This register is used to read the surround coefficient for the headphones.

Address: 46H, register name: HPSRDR1, block: DVX, access: R, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
HPSRDR1[7:0]							

Address: 47H, register name: HPSRDR2, block: DVX, access: R, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
HPSRDR2[7:0]							

6.19.1 HPSRDR1[7:0]

Data	Mode	Initial Value	Description
HPSRDR1[7:0]		Undefined	Surround coefficient setting register 1 (for headphones)

6.19.2 HPSRDR2[7:0]

Data	Mode	Initial Value	Description
HPSRDR2[7:0]		Undefined	Surround coefficient setting register 2 (for headphones)

Cautions 1. To access the surround coefficient read registers (44H, 45H, 46H, and 47H), first write to the surround address setting register, then continuously read data 192 times. Reading the data 192 times sets values to the RAM that stores internal surround coefficients.

2. The surround coefficient must be read using continuous read access. Even if the CS_B pin goes to high level during the continuous read operation and the CPU control switches to another device, the surround coefficient is read without any problem if it is accessed following the previous read operation when the CS_B pin goes to low level.

3. If an interrupt (INT_B) occurs while data is being read continuously, start over by writing the surround mode setting register again.

4. Reading and writing of surround coefficients are enabled only when ENSRD[1:0] = 00B.

6.20 Surround Mode Setting Register (SRDRA)

This register sets the mode for reading/writing of surround coefficients.

Address: 48H, register name: SRDRA, block: DVX, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
SRDRA[7:0]							

6.20.1 SRDRA[7:0]

Data	Mode	Initial Value	Description
SRDRA[7:0]		00H	Sets access to surround register

Caution Set SRDRA[7:0] to 00H.

6.21 BANK Register

This register is used to switch the Sound Register Bank and Control Register Bank in serial I/F mode.
This register is available in serial I/F mode only (it is only valid when PS = 1).

Address: 4FH, register name: BANK, CPU interface, access: R/W, initial value: 01H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	BANK

6.21.1 BANK

Data	Mode	Initial Value	Description
BANK		01H	BANK register for switching between Sound Register Bank and Control Register Bank.

When BANK = 0, Sound Register Bank is selected.
When BANK = 1, Control Register Bank is selected.
The BANK register can be accessed from both register banks.

Remark Fill the unused bits (D [7:1]) with zero values.

7. POWER STARTUP PROCEDURE

The μPD9992 includes four power supply units: the internal digital logic block power supply (DV_{DD}), PLL1/PLL2 power supply (AV_{DD}_P), internal analog circuit's power supply (AV_{DD}), and the I/O circuit's power supply (EV_{DD}).

7.1 Power Up Sequence

<1> With the RESET_B pin set to low level, turn on the power supply units (DV_{DD}, AV_{DD}, AV_{DD}_P, and EV_{DD}). We recommend turning on all four of these units at the same time.
<2> Wait until the power supply voltage reaches the specified voltage value.
<3> Cancel the hardware reset.
To cancel, set the RESET_B pin to high level.

7.2 Power Down Sequence

<1> With the RESET_B pin set to low level, turn off the power supply units (DV_{DD}, AV_{DD}, AV_{DD}_P, and EV_{DD}). We recommend turning off all four of these units at the same time.
<2> After power-down, the status of the RESET_B pin is undefined.

8. POWER SAVING FUNCTION

8.1 Software Power Saving Function (command-driven)

The μPD9992 includes a power saving function (standby mode) that is controlled by command input. For details, see **6.3 Standby Setting (STNBY)**.

8.2 Hardware Power Saving Function (by powering down the power supply

In addition to the software power saving function, a hardware power saving function is available. In such cases, note with caution that all data written to registers and memory will be deleted (be sure to rewrite this data after canceling the power saving operation).

Follow the steps described below when setting hardware power saving.

<1> With the RESET_B pin set to low level, turn off DV_{DD}, AV_{DD}, and AV_{DD}_P.
<2> Continue supplying EV_{DD} since it is used to protect the CPU bus line.
<3> Be sure to fix the RESET_B pin to low level during a hardware power saving operation.

Follow the steps described below to cancel hardware power saving.

<1> With the RESET_B pin set to low level, turn on DV_{DD}, AV_{DD}, and AV_{DD}_P.
<2> Set the RESET_B pin to high level.

9. SETTING SEQUENCE

In this chapter, two steps ‘switching to Sound Register Bank’ and ‘switching to Control Register Bank’ are required when PS = 1 (serial I/F mode).

‘Switching to Sound Register Bank’ means to switch to the Sound Register Bank when the current BANK register is the Control Register Bank. ‘Switching to Control Register Bank’ means to switch to the Control Register Bank when the current BANK register is the Sound Register Bank”.

On the other hand, ‘switching to Sound Register Bank’ and ‘switching to Control Register Bank’ are not required when PS = 0 (parallel I/F mode).

9.1 Power Up

Steps	Items	Target Register, etc.
1	Cancel hardware reset	RESET_B pin (low to high)
2	Set PLL	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS
4	Cancel PLL standby	STPLL1, STPLL2, STREF
5	Cancel standby	STSYNTH, STDIG, STASI, STASO, STDAC
6	Internal clock is valid	After canceling standby for STDIG and STSYNTH, normal operation begins after at least 2 ms have elapsed.

9.2 Basic Sequence for Switching Among Operation Modes

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STREF, STSYNTH, STDIG, STASI, STASO, STDAC
5	Switch sound source/audio path	SLSORCE
6	Switching surround on/off setting	ENSRD
7	Set sampling frequency	FS
8	Set ASIO mode	MS, ASIM, LRCLK, SLR
9	Cancel PLL standby	STPLL1, STPLL2, STREF
10	Cancel standby	STSYNTH, STDIG, STASI, STASO, STDAC
11	Internal clock is valid	After canceling standby for STDIG and STSYNTH, normal operation begins after at least 2 ms have elapsed.
12	Cancel analog volume mute	AAULGA, AAURGA
13	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Remarks 1. During slave mode, input of LRCLK and BCLK are required.

2. Setting of mute after using the analog volume control to lower the volume step by step and to raise of the volume after canceling the mute setting are performed in order to eliminate any audible change in sound that can occur due to single-frame operation errors in the digital data that is generated while switching.

An example of raising and lowering volume step by step is shown below.

Example STEP = 1.5 dB (minimum unit)
Cycle (time per step) for raising or lowering = 200 μs per step

These values are merely an example from our company's evaluations. Adjustments for each set should be made as determined by the manufacturer.

3. The STDIG signal is also used to reset operations such as digital filter operations, so it is required when switching modes.

9.2.1 Mute

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume mute	AAULGA, AAURGA

9.2.2 Standby

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STREF, STSYNTH, STDIG, STASI, STASO, STDAC
5	Cancel PLL standby	STPLL1, STPLL2, STREF
6	Cancel standby	STSYNTH, STDIG, STASI, STASO, STDAC
7	Internal clock is valid	After canceling standby for STDIG and STSYNTH, normal operation begins after at least 2 ms have elapsed.
8	Cancel analog volume mute	AAULGA, AAURGA
9	Raise analog volume step by step (recommended)	AAULGA, AAURGA

9.2.3 FS Setting

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STREF, STSYNTH, STDIG, STASI, STASO, STDAC
5	Set sampling frequency	FS
6	Cancel PLL standby	STPLL1, STPLL2, STREF
7	Cancel standby	STSYNTH, STDIG, STASI, STASO, STDAC
8	Internal clock is valid	After canceling standby for STDIG and STSYNTH, normal operation begins after at least 2 ms have elapsed.
9	Cancel analog volume mute	AAULGA, AAURGA
10	Raise analog volume step by step (recommended)	AAULGA, AAURGA

9.2.4 Path Setting

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume mute	AAULGA, AAURGA
4	Switch sound source/audio path	SLSORCE
5	Cancel analog volume mute	AAULGA, AAURGA
6	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Caution Data may be incorrect in one frame.

9.2.5 Surround Setting

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume mute	AAULGA, AAURGA
4	Switching surround on/off setting	ENSRD
5	Cancel analog volume mute	AAULGA, AAURGA
6	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Caution Data may be incorrect in one frame.

9.2.6 ASIO Setting

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STREF, STSYNTH, STDIG, STASI, STASO, STDAC
5	Set ASIO mode	MS, ASIM, LRCLK, SLR
6	Cancel PLL standby	STPLL1, STPLL2, STREF
7	Cancel standby	STSYNTH, STDIG, STASI, STASO, STDAC
8	Internal clock is valid	After canceling standby for STDIG and STSYNTH, normal operation begins after at least 2 ms have elapsed.
9	Cancel analog volume mute	AAULGA, AAURGA
10	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Caution Data may be incorrect in one frame.

9.2.7 DVX RAM access

Steps	Items	Target Register, etc.
1	Switching to Control Register Bank (When PS = 1)	BANK
2	Read/write of the surround coefficient	ENSRD[1:0]=00B
3	Address specification	Address specification
4	Data transfer	Data transfer

9.3 Setting Sequence Example

9.3.1 Sound source-DAC output

(1) Power Up

Steps	Items	Target Register, etc.
1	Cancel hardware reset	RESET_B pin (low to high)
2	Set PLL	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 32 kHz
4	Sound source/audio path switching	SLSORCE = 0
5	Cancel PLL standby	STPLL1 = STPLL2 = STREF = 1
6	Cancel standby	STDIG = STSYNTH = STDAC = 1
7	Internal clock is valid	After canceling standby for STDIG and STSYNTH, normal operation begins after at least 2 ms have elapsed.

(2) 'Switching to Sound Register Bank' (When PS = 1)

(3) Sound source setting

(4) Sound source data transfer

(5) Raising volume

Steps	Items	Target Register, etc.
8	Switching to Control Register Bank(When PS = 1)	BANK
9	Cancel analog volume mute	AAULGA, AAURGA
10	Raise analog volume step by step (recommended)	AAULGA, AAURGA

9.3.2 Sound source-ASO output

(1) Power Up

Steps	Items	Target Register, etc.
1	Cancel hardware reset	RESET_B pin (low to high)
2	Set PLL	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 32 kHz
4	Sound source/audio path switching	SLSORCE = 0
5	Set ASIO mode	MS, ASIM, LRCLK, SLR
6	Cancel PLL standby	STPLL1 = STPLL2 = STREF = 1
7	Cancel standby	STDIG = STSYNTH = STASO = 1
8	Internal clock is valid	After canceling standby for STDIG and STSYNTH, normal operation begins after at least 2 ms have elapsed.

(2) 'Turning to Sound Register Bank' (When PS = 1)

(3) Sound source setting

(4) Sound source data transfer

9.3.3 ASI-DAC output

(1) Power Up

Steps	Items	Target Register, etc.
1	Cancel hardware reset	RESET_B pin (low to high)
2	Set PLL	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, or 48 kHz
4	Sound source/audio path switching	SLSORCE = 1
5	Set ASIO mode	MS, ASIM, LRCLK, SLR
6	Cancel PLL standby	STPLL1 = STREF = 1
7	Cancel standby	STDIG = STDAC = STASI = 1
8	Internal clock is valid	After canceling standby for STDIG, normal operation begins after at least 2 ms have elapsed.

(2) Music data transmission

(3) Raising volume

Steps	Items	Target Register, etc.
9	Cancel analog volume mute	AAULGA, AAURGA
10	Raise analog volume step by step (recommended)	AAULGA, AAURGA

9.3.4 ASI-ASO output

(1) Power application

Steps	Items	Target Register, etc.
1	Cancel hardware reset	RESET_B pin (low to high)
2	Set PLL	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 8 kHz, 16 kHz, 32 kHz, 44.1 kHz or 48 kHz
4	Sound source/audio path switching	SLSORCE = 1
5	Set ASIO mode	MS, ASIM, LRCLK, SLR
6	Cancel PLL standby	STPLL1 = STREF = 1
7	Cancel standby	STDIG = STASI = STASO = 1
8	Internal clock is valid	After canceling standby for STDIG, normal operation begins after at least 2 ms have elapsed.

(2) Music data transmission

9.4 Relation Between Setting Modes and Internal Operations (Relation with Synchronization Clock)

Table 9-1. Relation Between Setting Modes and Internal Operations (Relation with Synchronization Clock)

Function	Register				Pin (Signal) Status					Actual Use	Remark
	MS	SLSORCE	STASI	STASO	LRCLK, BCLK	Sync. Clock sync_lr	ASI	ASO	LINE_OUT (DAC)		
Slave mode, sound source path, standby during ASI and ASO	0 slave	0 synth	0 off	0 off	Input/ internal low	Internal	Invalid	Hi-Z	OUT	Sound source-DAC	Even though slave mode has been set, the internal clock operates.
Slave mode, sound source path, ASI standby, ASO output	0 slave	0 synth	0 off	1 on	Signal input	External	Invalid	OUT	OUT	Sound source-ASO	Uses external synchronization clock. If the external LRCLK signal has not yet been input, outputs are stopped.
Slave mode, audio path, ASI input, ASO standby	0 slave	1 audio	1 on	0 off	Signal input	External	IN	Hi-Z	OUT	ASI-DAC	Uses external synchronization clock. If the external LRCLK signal has not yet been input, outputs are stopped.
Slave mode, audio path, ASI input, ASO output	0 slave	1 audio	1 on	1 on	Signal input	External	IN	OUT	OUT	ASI-ASO	Uses external synchronization clock. If the external LRCLK signal has not yet been input, outputs are stopped.
Master mode, sound source path, standby during ASI and ASO	1 master	0 synth	0 off	0 off	Low output	Internal	Invalid	Hi-Z	OUT	Sound source-DAC	The internal clock operates.
Master mode, sound source path, ASI standby, ASO output	1 master	0 synth	0 off	1 on	Signal output	Internal	Invalid	OUT	OUT	Sound source-ASO	The internal clock operates.
Master mode, audio path, ASI input, ASO standby	1 master	1 audio	1 on	0 off	Signal output	Internal	IN	Hi-Z	OUT	ASI-DAC	The internal clock operates.
Master mode, audio path, ASI input, ASO output	1 master	1 audio	1 on	1 on	Signal output	Internal	IN	OUT	OUT	ASI-ASO	The internal clock operates.

Remark The operations in Table 9-1 apply to the operations in mixing mode (address 05H, MIX = 1). Therefore, when setting mixing (MIX = 1) while the ASIO is in slave mode (address 08H, MS = 1), be sure to set STASI = 1 and input BCLK and LRCLK.

When stopping the ASI input and using the sound source only, retain the settings of MS = 1, MIX = 1, and STASI = 1 or set MIX = 0 and SLSORCE = 0.

10. STANDBY MODE

Set standby mode using the STNBY register (address: 00H) (see **6.3 Standby Setting (STNBY)**). Observe the following regarding the standby status of each block.

10.1 Clock Supply

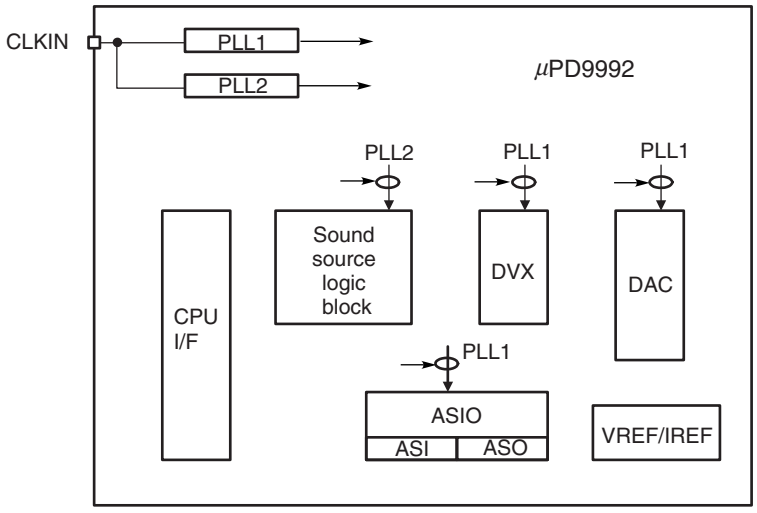
To use the sound source logic block, the PLL2 standby mode must be canceled.

To use the DVX, DAC and ASIO blocks, see the table below and **9.3 Setting Sequence Example**.

Address	Remark
01H to 04H, 07H to 08H	The data must be set in the PLL1 standby mode.
00H, 0DH to 0EH, 3FH, 4FH (in serial mode only)	Writing/reading data is enabled in either the PLL1 standby mode or PLL1 On mode (standby mode canceled).
05H to 06H, 09H to 0CH	Basically set data in the PLL1 standby mode. In the PLL1 On mode using, see **9.3 Setting Sequence Example**.
40H to 48H	The data must be set in the PLL1 On mode (standby mode canceled).

The supply of clock signals from the PLL to various blocks is illustrated in Figure 10-1.

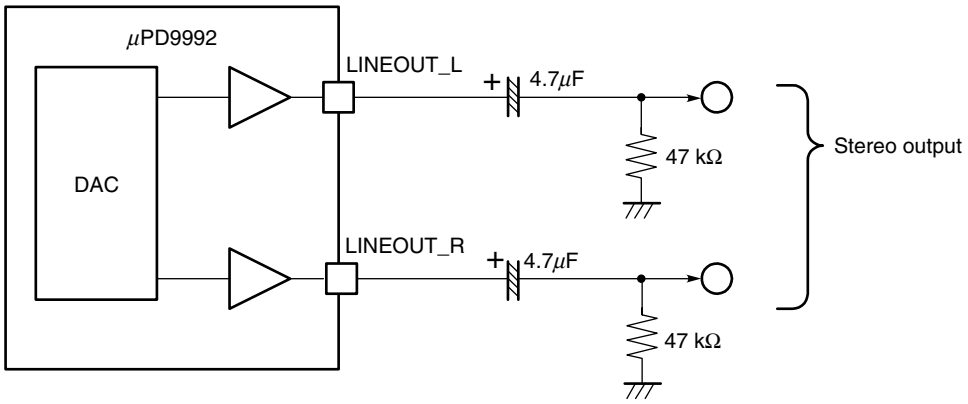
Figure 10-1. Destination of Clocks Supplied from PLL1 and PLL2



11. REFERENCE SCHEMATICS

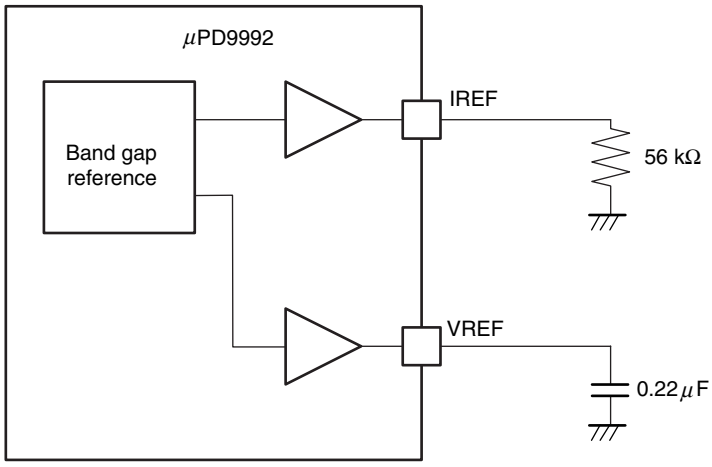
11.1 Line Out Pins (LINEOUT_L and LINEOUT_R)

Figure 11-1. Example of Connection to Line Out Pin



11.2 Reference Power Supply Voltage and Current Supply Pins (VREF and IREF)

Figure 11-2. Handling of VREF and IREF Pins



The VREF and IREF blocks include the following functions.

- Reference voltage is generated using band gap
- The reference current is generated using this reference voltage and an external resistance, and is supplied to all analog circuits.

The VREF and IREF blocks operates when STREF = 1 in the STNBY register. Normal mode is set within 1.0 ms after this STREF bit is set (= 1).

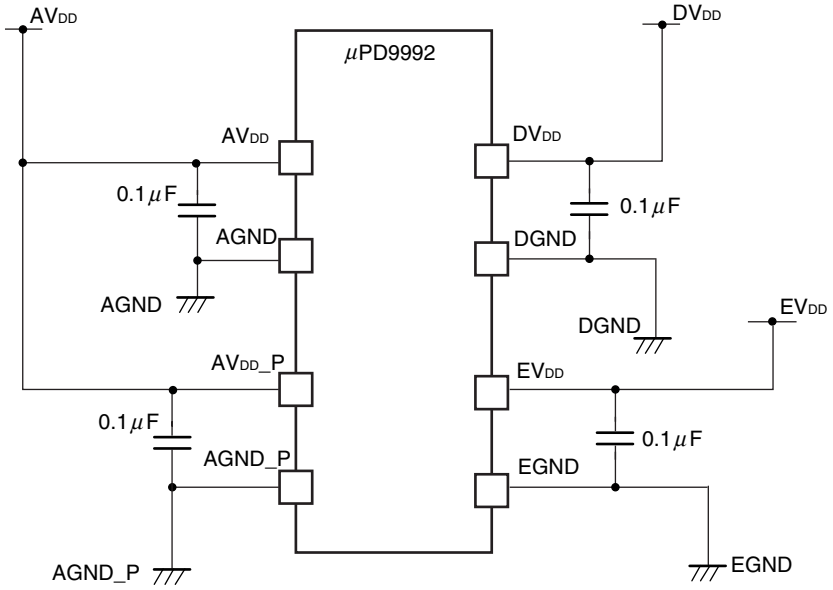
Cautions 1. Be sure to connect a 56 kΩ resistor between the IREF pin and AGND. Do not connect any other resistors to the IREF pin.

2. Be sure to connect a 0.22 μF (±20%) capacitor between the VREF pin and AGND. Do not connect any other capacitors to the VREF pin.

11.3 Power Supply

Whenever possible, avoid placing a decoupling capacitor close to any of the μPD9992's pins.

Figure 11-3. Placement of Decoupling Capacitor

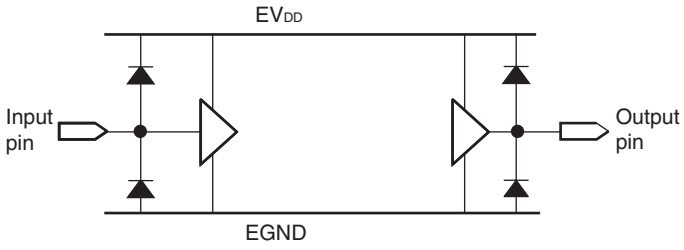
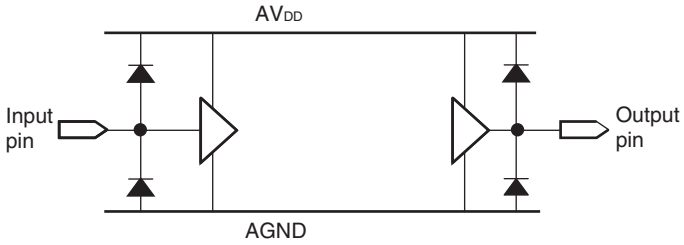
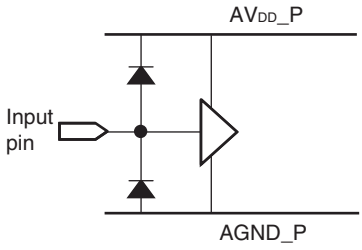
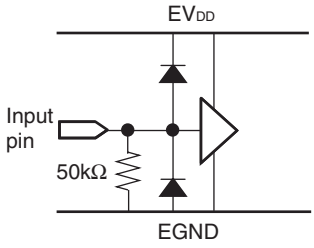


The pairing of pins between the power supply (with decoupling capacitor) and GND is as follows (pin numbers are indicated in parentheses).

AVDD (1E) – AGND (1D)
AVDD_P (2G) – AGND_P (1H)
DVDD (9K) – DGND (5K)
DVDD (10D) – DGND (10J)
EVDD (9C) – EGND (6A)
DVDD (9A) – EGND (6A)

Caution EVDD is used for digital operations. Therefore, it is recommended to use a different power supply to the analog power supplies (AVDD and AVDD_P) to avoid affecting the analog characteristics.

11.4 Pin Outline Schematics

Input Pin	Output Pin	Pin Outline Schematic
TM3, TM4, PO0 to PO3, A1/RXD, A0/Data,TXD, CS_B/SCS, WR_B/SCLK, RD_B/SPIMODE, D0/ SERINIT, D1to D7, RESET_B, LRCLK, BCLK,	TM3, TM4, PO0 to PO3, A0/Data,TXD, D0/SERINIT, D1to D7, INT_B, VIB, LED, LRCLK, BCLK, ASO	
IREF, VREF	IREF, VREF, LINEOUT_L, LINEOUT_R	
CLKIN	–	
TM0 to TM2, ASI, PS, TRSCK, CLK8K, RDATA	–	

12. ELECTRICAL SPECIFICATIONS

12.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	DV_{DD}	For digital ports	–0.3 to +2.0	V
	EV_{DD}	For I/O pins	–0.3 to +4.0	V
	AV_{DD}	For analog ports	–0.3 to +4.0	V
	AV_{DD}_P	For PLL	–0.3 to +4.0	V
Input voltage	V_I	$V_I/V_O < EV_{DD} + 0.5$ V	–0.3 to +4.0	V
Output voltage	V_O		–0.3 to +4.0	V
Power dissipation	P_D		300	mW
Storage temperature	T_{stg}		–50 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

12.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating voltage	DV_{DD}	–20 to +85°C	1.425	1.5	1.575	V
	EV_{DD}		1.71	3.0	3.3	V
	AV_{DD}		2.85	3.0	3.15	V
	AV_{DD}_P		2.85	3.0	3.15	V
Input voltage	V_I		0		EV_{DD}	V
Operating ambient temperature	T_A		–20		+85	°C

12.3 Capacitance

(T_A = +25°C, DV_{DD} = 0 V, EV_{DD} = 0 V)

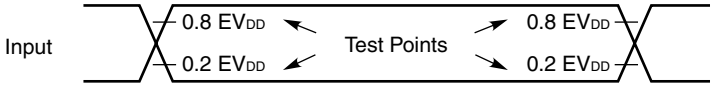
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz, pins other than those tested: 0 V		10		pF
Output capacitance	C_O			10		pF
I/O capacitance	C_{IO}			10		pF

12.4 DC Characteristics

(T_A = –20 to +85°C, with DV_{DD} and EV_{DD} within recommended operating condition range)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IHN}		0.8 EV_{DD}		EV_{DD}	V
Input voltage, low	V_{ILN}		0		0.2 EV_{DD}	V
Output voltage, high	V_{OH3}	EVDD = 3.0 V, I_{OH} = –1 mA (LED, VIB = –4 mA)	0.8 EV_{DD}			V
	V_{OH18}	EVDD = 1.8 V, I_{OH} = –1 mA (LED, VIB = –1.5 mA)	0.8 EV_{DD}			V
Output voltage, low	V_{OL3}	EVDD = 3.0 V, I_{OL} = +1 mA (LED, VIB = +4 mA)			0.2 EV_{DD}	V
	V_{OL18}	EVDD = 1.8 V, I_{OL} = +1 mA (LED, VIB = +1.5 mA)			0.2 EV_{DD}	V
Input leakage current, high	I_{LHN}	V_I = EV_{DD}	0		10	μA
Input leakage current, low	I_{LLN}	V_I = 0 V	–10		0	μA
High-impedance leakage current	I_{ZI}	0 V ≤ V_I ≤ EV_{DD}	0		–10	μA

Common ratings for switching characteristics



12.5 AC Characteristics

(Unless otherwise specified, T_A = –20 to +85°C, with DV_{DD}, EV_{DD}, AV_{DD}, and AV_{DD}_P within recommended operating condition range)

12.5.1 Clock

Timing requirements

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLKIN input frequency	f_{CLKIN}	V_{CLKIN} = 0.5V_{p-p}	2.688		16.128	MHz
CLKIN input level	V_{CLKIN}	f_{CLKIN} = 2.688 MHz to 16.128 MHz[Note 1]	0.5		**Note 2**	V_{p-p}
PLL lockup time	t_{LPLL}				1.0	ms

Notes 1. CLKIN input to be used as PLL input should have capacitive coupling (1000 pF).

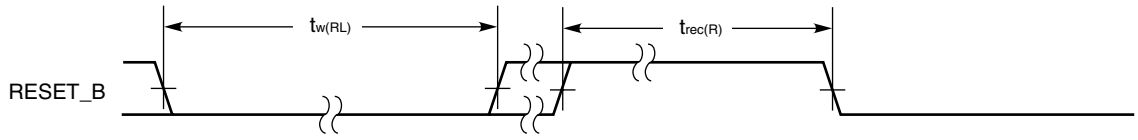
2. The maximum input level for CLKIN should not exceed the power supply (AV_{DD}-P) potential.

12.5.2 Reset

Timing requirements

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RESET_B low-level width	$t_{w(RL)}$		200			ns
RESET_B recovery time	$t_{rec(R)}$		200			ns

Reset timing



12.5.3 Host interface

(1) Parallel I/F mode

Timing requirements (EV_{DD} = 3.0 V and 1.8 V, during access other than DVX register)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RD_B width 1	t_{wRD1}		100			ns
WR_B width 1	t_{wWR1}		40			ns
RD_B recovery time 1	t_{rcRD1}		30			ns
WR_B recovery time 1	t_{rcWR1}		80			ns
Data setup time	t_{suD1}	WR_B↑	50			ns
Data hold time	t_{hD1}	WR_B↑	0			ns
A, CS_B setup time	t_{suAW}	WR_B↑	15			ns
A, CS_B hold time	t_{hAW}	WR_B↑	0			ns
A, CS_B setup time	t_{suAR}	RD_B↓	0			ns
A, CS_B hold time	t_{hAR}	RD_B↑	0			ns

Switching characteristics (EV_{DD} = 3.0 V and 1.8 V, during access other than DVX register)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data access time 1	t_{accDO1}	RD_B↓, I_{sink} = 1 mA			100	ns
Data hold time 1	t_{dDO1}	RD_B↑, I_{sink} = 1 mA	0		30	ns

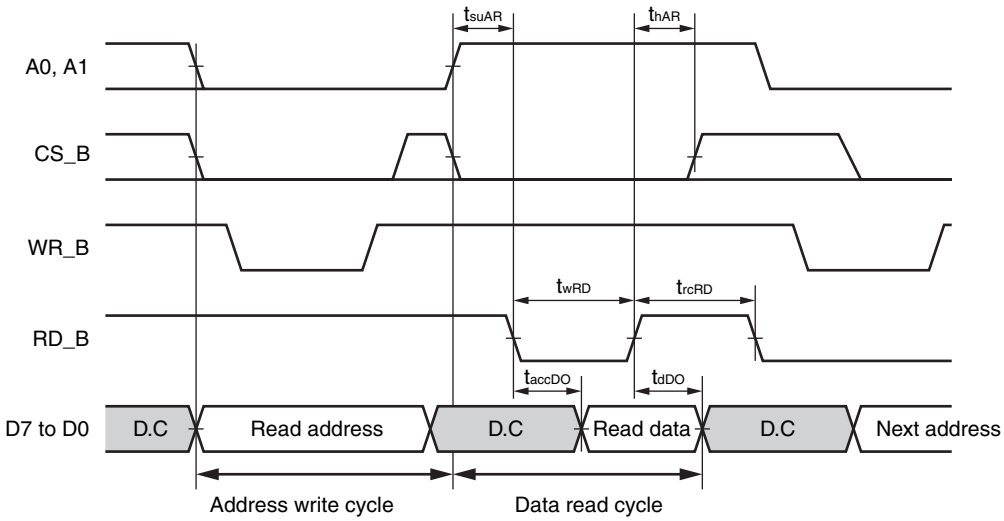
Timing requirements (EV_{DD} = 3.0 V and 1.8 V, during access DVX register)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RD_B width 2	t_{wRD2}		125			ns
WR_B width 2	t_{wWR2}		70			ns
RD_B recovery time 2	t_{rcRD2}		30			ns
WR_B recovery time 2	t_{rcWR2}		120			ns
Data setup time	t_{suD1}	WR_B↑	50			ns
Data hold time	t_{hD1}	WR_B↑	0			ns
A, CS_B setup time	t_{suAW}	WR_B↑	15			ns
A, CS_B hold time	t_{hAW}	WR_B↑	0			ns
A, CS_B setup time	t_{suAR}	RD_B↓	10			ns
A, CS_B hold time	t_{hAR}	RD_B↑	0			ns

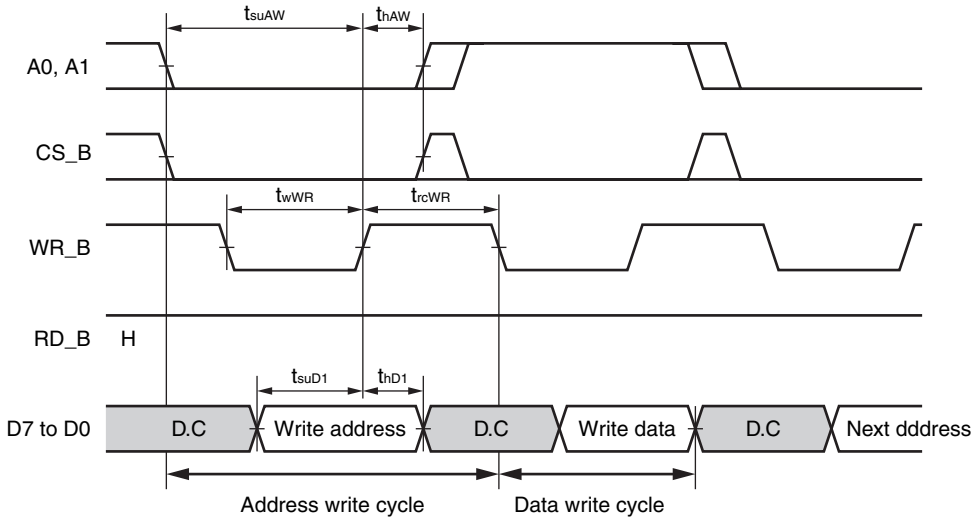
Switching characteristics (EV_{DD} = 3.0 V and 1.8 V, during access DVX register)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data access time 2	t_{accDO2}	RD_B↓, I_{sink} = 1 mA			125	ns
Data hold time 2	t_{dDO2}	RD_B↑, I_{sink} = 1 mA	0		30	ns

Host interface read timing



Host interface write timing



(2) Serial I/F mode (both 3-wire SPI mode and 4-wire SPI mode)

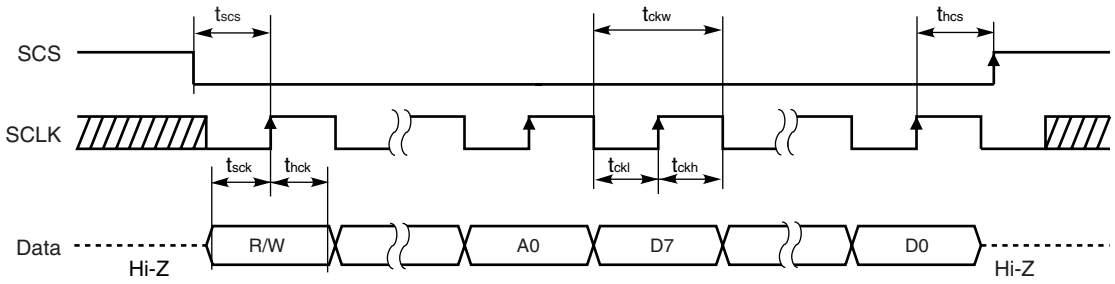
Timing requirements (EV_{DD} = 3.0 V and 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLK period	t_{ckw}		190			ns
SCLK high level width	t_{ckh}		95			ns
SCLK low level width	t_{ckl}		95			ns
Data setup time	t_{sck}	SCLK↑	20			ns
Data hold time	t_{hck}	SCLK↑	10			ns
SCS setup time	t_{scs}	SCLK↑	20			ns
SCS hold time	t_{hcs}	SCLK↑	20			ns
Read data access time 1	t_{racc1}	Hi-Z time from SCLK↓ to data output (D7)	2		75	ns
Read data access time 2	t_{racc2}	From SCLK ↓to data output (D6 to D0)			75	ns
Read data access time 3	t_{dz}	From SCLK↓ to when data changes to Hi-Z	0		75	ns
Next SCS access time	t_{csacc}	From SCS ↑to SCS↓	1			SCLK
SCS setup time	t_{dhh}	SERINT↑	0			ns
SERINIT width	$t_{whSERINIT}$		20			ns
SCS hold time	t_{dll}	SERINT↓	0			ns

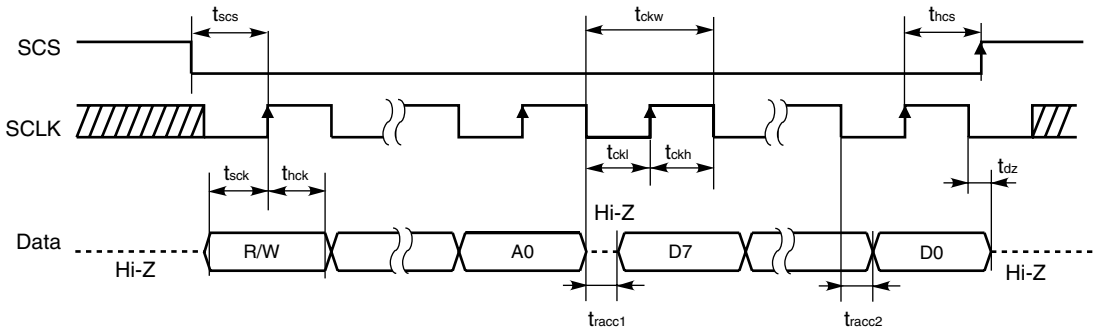
Switching characteristics (EV_{DD} = 3.0 V and 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCS hold time rom SCLK rising edge when accessing FIFOs inside DVX	t_{hcsdvx}	SCLK↑, while accessing DVX RAM	170			ns

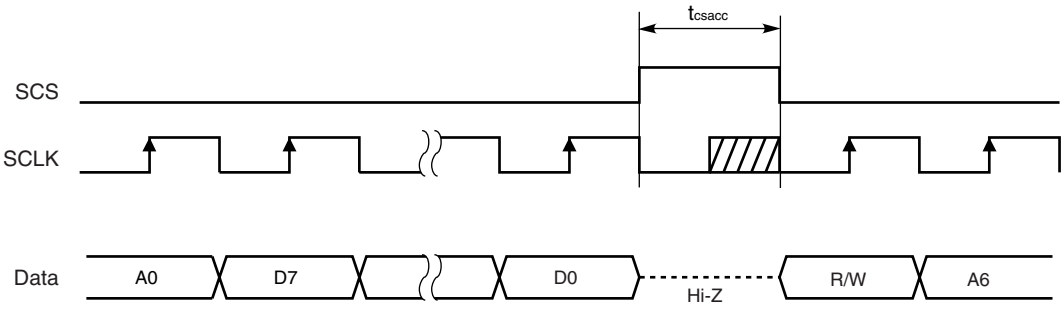
Serial interface write timing



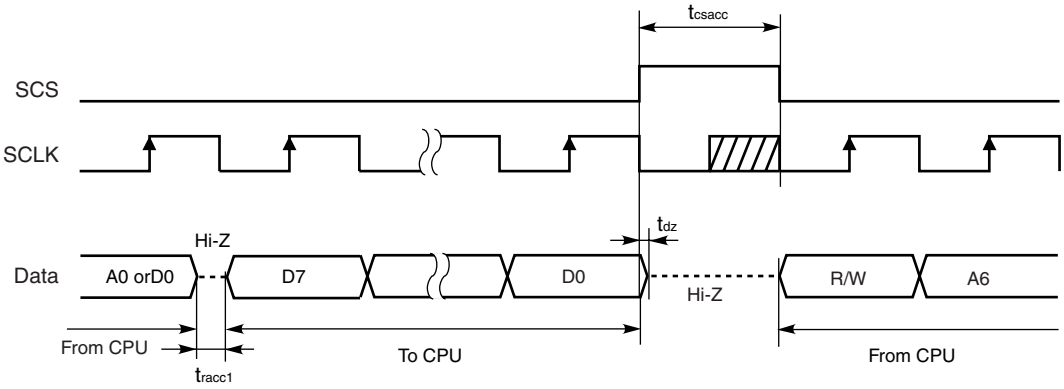
Serial interface read timing



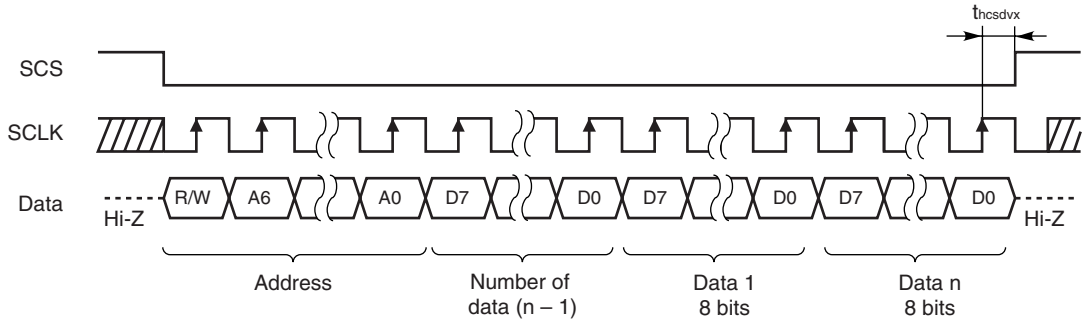
Serial interface write timing (continuous access)



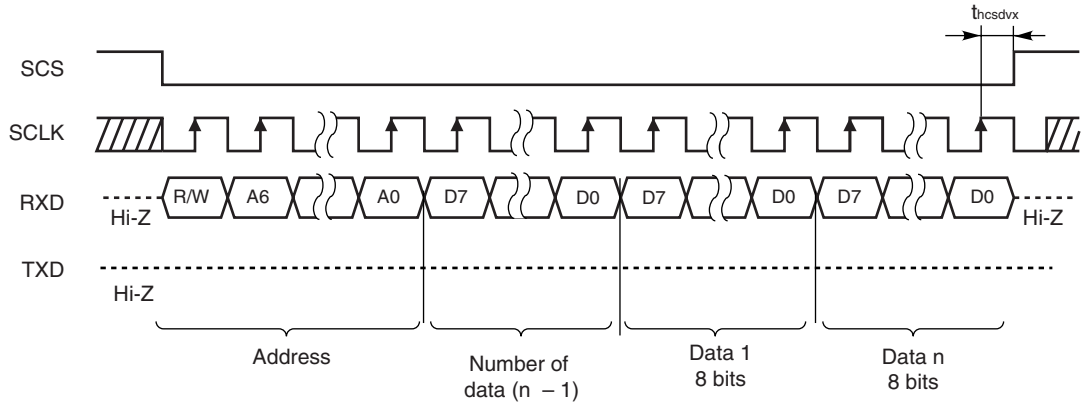
Serial interface read timing (continuous access)



3-wire SPI mode (format of host CPU continuous access 3)



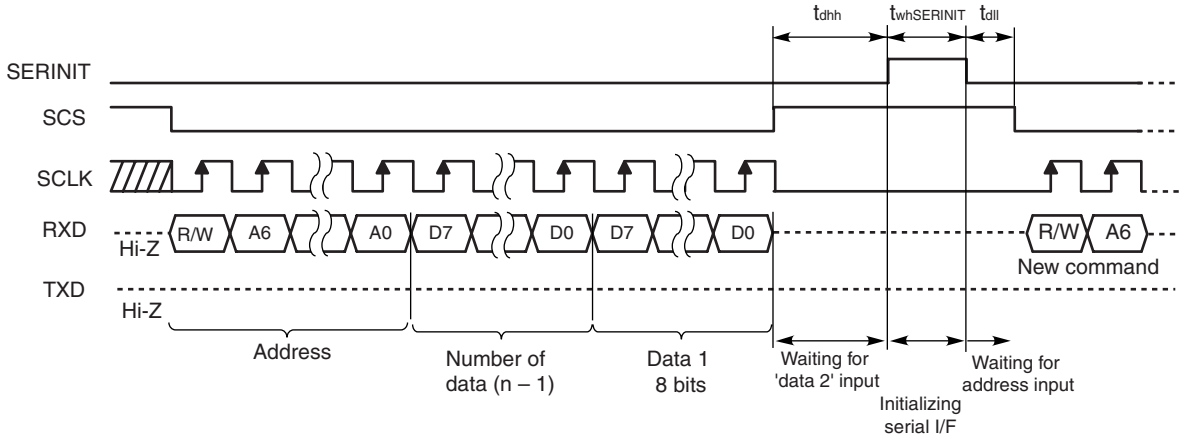
4-wire SPI mode (format of host CPU continuous access 3)



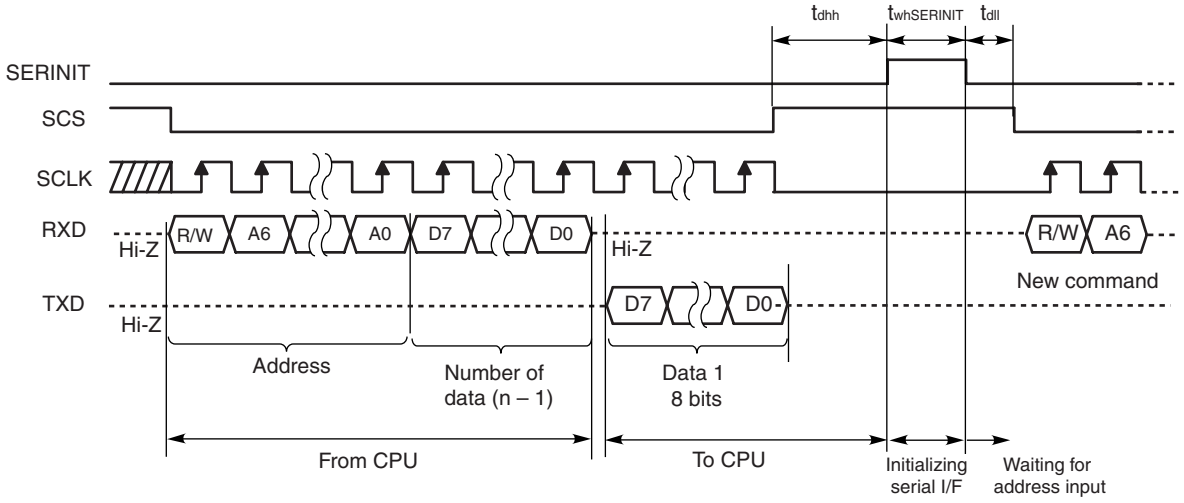
Initialization signal (SERINIT)

Canceling continuous access using SERINIT pin

Write access



Read access



12.5.4 Audio serial interface

Timing requirements (EV_{DD} = 3.0 V and 1.8 V)

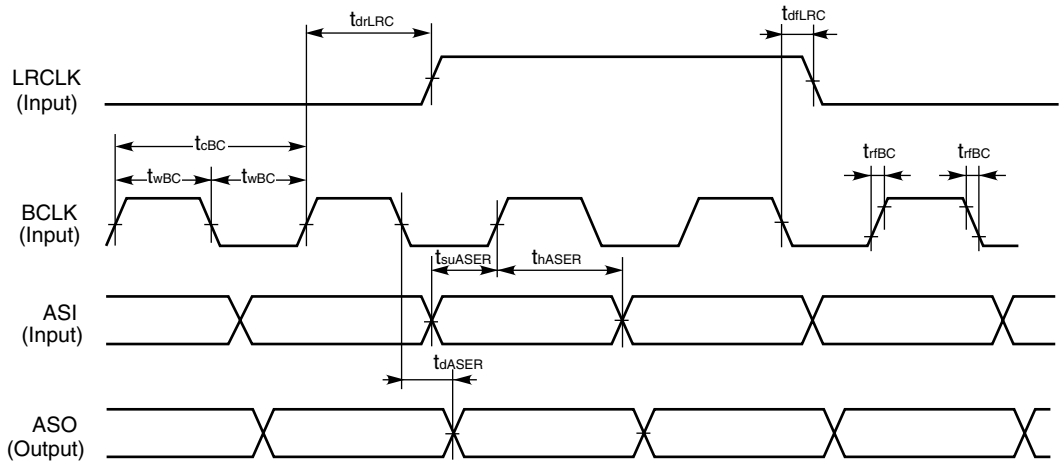
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LRCLK cycle time	t_{cLR}			1/fs		ns
BCLK cycle time	t_{cBC}	When set to 64 bits per frame[Note]		1/(fs × 64)		ns
BCLK high-/low-level width	t_{wBC}			t_{cBC}/2		ns
BCLK rise/fall time	t_{rfBC}				20	ns
LRCLK rising edge delay time	t_{drLRC}	BCLK↑	50			ns
LRCLK falling edge delay time	t_{dfLRC}	BCLK↓	50			ns
ASI input setup time	t_{suASER}	BCLK↑	25			ns
ASI input hold time	t_{hASER}	BCLK↑	25			ns

Note The configuration of each frame varies according to the settings in the BFS[4:0] bits of the SLFS register (07H).

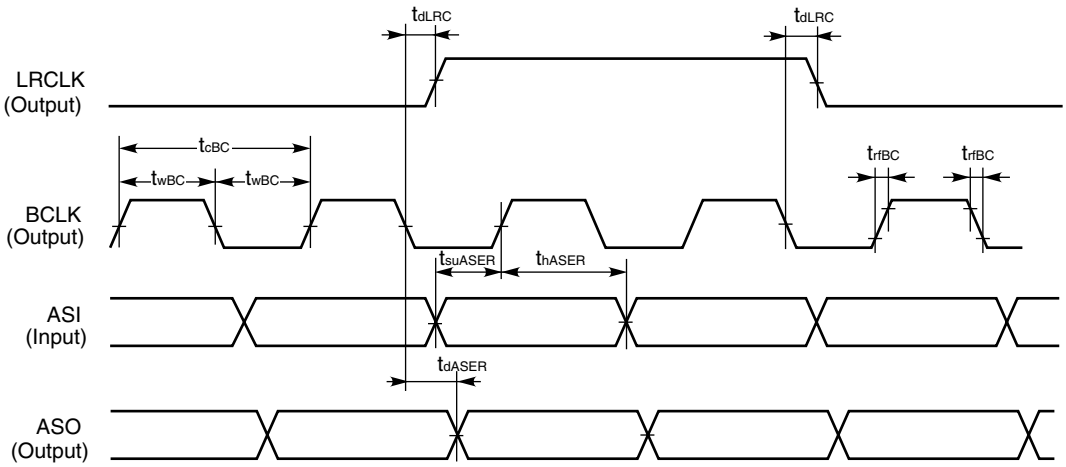
Switching characteristics (EV_{DD} = 3.0 V and 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LRCLK output delay time	t_{dLRC}	BCLK↓			50	ns
ASO output delay time	t_{dASER}	BCLK↓	–37.5		+50	ns

Audio serial I/O timing (slave mode)



Audio serial I/O timing (master mode)



12.6 Analog Characteristics

The propagation characteristics from the D/A converter to the line output are described below.
Unless otherwise specified, the following conditions must be met.

D/A converter input level INPUT = 0 dBFS (D/A converter's full scale input is defined as 0 dBFS)
D/A converter input frequency f_{IN} = 997 Hz
Sampling frequency fs = 48 kHz
Ambient temperature T_A = 25°C
Power supply voltage AV_{DD} = 3.0 V
Output load R_L = 10 kΩ

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum output level	V_O	VOLUME = 0 dB	1.8	2.0	–	V_{p-p}
Gain error 1	GE_{max}	VOLUME = 0 dB, 0 dBr = 2.0 V_{p-p}	–1	0	+1	dBr
Gain error 2	GE_{min}	VOLUME = –45 dB, value relative to G_{Emax} reference	–47	–45	–43	dB
Gain adjustment resolution	G_{step}	VOLUME = When 0 to –45 dB, differential error	1	1.5	2	dB
THD	THD	VOLUME = 0 dB, f = 20 Hz to 19.2 kHz	–	–80	–74	dB
Frequency characteristics 100 Hz to 19.2 kHz	GF	VOLUME = 0 dB, INPUT = –10 dBm@997 Hz, output when at 997 Hz is used as 0 dB reference	–1	0	+1	dB
Dynamic range	SND	VOLUME = 0 dB, INPUT = –60 dBFS, f = 20 Hz to 19.2 kHz, A-wgt filter	80	86	–	dB

12.7 Mode-Specific Current Consumption Characteristics

Unless otherwise specified, the following conditions must be met.

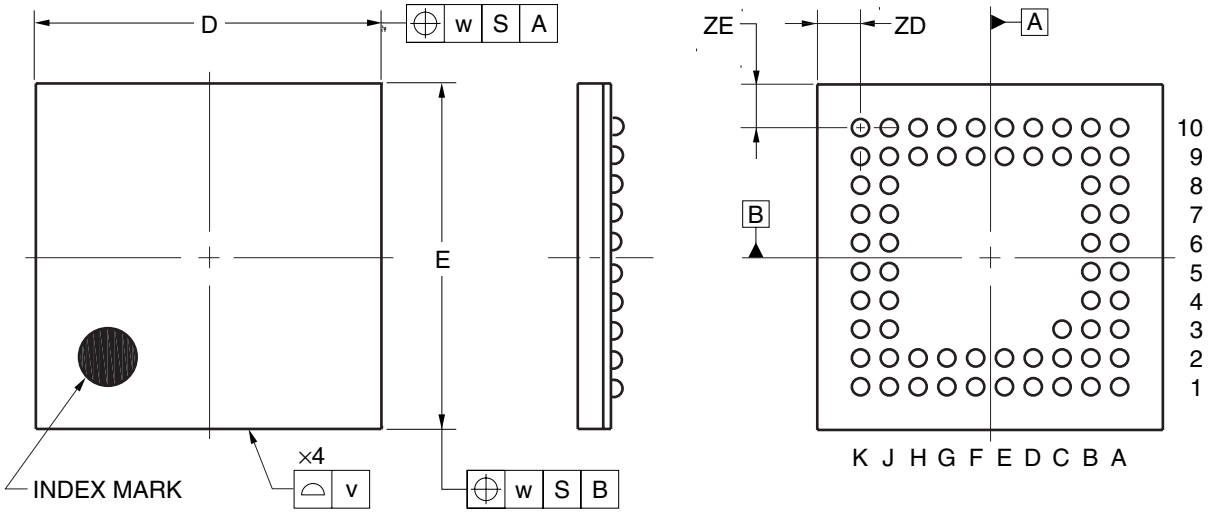
Sound source master clock = 55.104 MHz
Master clock other than sound source master clock = 24.576 MHz
D/A converter input level INPUT = 0 dBFS (D/A converter's full scale input is defined as 0 dBFS)
D/A converter input frequency f_{IN} = 997 Hz
Sampling frequency fs = 48 kHz
Ambient temperature T_A = 25°C
Power supply voltage AV_{DD} = AV_{DD}_P = EV_{DD} = 3.0 V, DV_{DD} = 1.5 V
Output load R_L = 10 kΩ

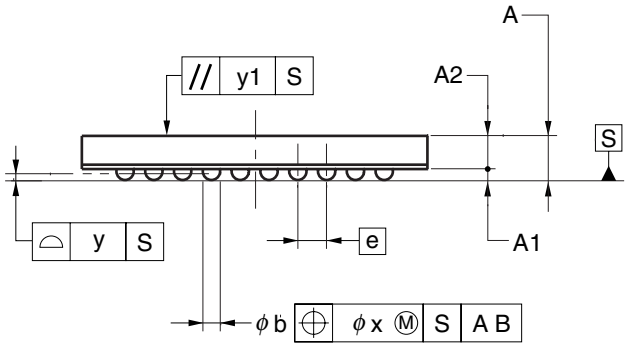
Parameter	Symbol	Conditions	Power Supply Pin	MIN.	TYP.	MAX.	Unit
Current during output from sound source to DAC	I_{DD1}	STDIG = STPLL2 = STPLL1 = STSYNTH = STDAC = STREF = 1, SLSORCE = 0 and sound generator is operating normally	DV_{DD}	–	30	45	mA
			AV_{DD}	–	8	14	mA
			AV_{DD}_P	–	3	6	mA
			EV_{DD} Note	–	–	1	mA
Current during output from sound source to ASO	I_{DD2}	STDIG = STPLL2 = STPLL1 = STSYNTH = STREF = 1, SLSORCE = 0, ASO = 1 and sound generator is operating normally	DV_{DD}	–	30	45	mA
			AV_{DD}	–	4	6	mA
			AV_{DD}_P	–	3	6	mA
			EV_{DD} Note	–	–	5	mA
Current during output from ASI to DAC	I_{DD3}	STDIG = STPLL1 = STDAC = STREF = 1, SLSORCE = 1, ASI = 1	DV_{DD}	–	5	8	mA
			AV_{DD}	–	8	14	mA
			AV_{DD}_P	–	2	4	mA
			EV_{DD} Note	–	–	1	mA
Current during output from ASI to ASO	I_{DD4}	STDIG = STPLL1 = STREF = 1, SLSORCE = 1, ASI = ASO = 1	DV_{DD}	–	5	8	mA
			AV_{DD}	–	4	6	mA
			AV_{DD}_P	–	2	4	mA
			EV_{DD} Note	–	–	5	mA
Standby current (command-driven)	ISTB	STDIG = STPLL2 = STPLL1 = STASI = STASO = STSYNTH = STDAC = STREF = 0, input : connect to GND output : open (no load)	DV_{DD}	–	5	100	μA
			AV_{DD}	–	1	5	μA
			AV_{DD}_P	–	1	5	μA
			EV_{DD} Note	–	–	10	μA

Note The EV_{DD} pin current is measured when there is no load.
In the actual operation of the μPD9992, the EV_{DD} pin current differs depending on the external environment such as the clock rate, load capacitance, and load resistance.

13. PACKAGE DRAWING

65-PIN TAPE FBGA (6x6)





(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.10
E	6.00±0.10
v	0.15
w	0.20
e	0.50
A	0.83±0.10
A1	0.18±0.05
A2	0.65
b	0.32±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P65F9-50-BA1-1

14. RECOMMENDED SOLDERING CONDITIONS

The μPD9992 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

★ • μPD9992FP-BA1-A: 65-pin tape FBGA (6 × 6)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 250°C, Time: 80 sec. max. (at 220°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that prebaking is necessary at 125°C for 10 to 72 hours) Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. **<Caution>** **Products packed in a medium other than a heat-resistance tray (such as a magazine, taping, and non-heat-resistance tray) cannot be baked.**	IR50-107-2

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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