

# 1.5A Dual WLED Flash Driver with I<sup>2</sup>C Compatible Interface

## DESCRIPTION

The EUP2471 is a 2MHz fixed frequency, current mode synchronous boost converter. The device is designed to operate as a dual 750mA (1.5A total) constant current driver for flash white LED application.

An industry-standard I<sup>2</sup>C serial digital input is used to enable, disable and set the movie-mode current for each flash LED with up to 16 movie-mode settings. The EUP2471 also includes a separate Flash Enable input to initiate both the flash operation and the default timer, which can be used either to terminate a flash event at the end of a user-programmed delay or as a safety feature. The maximum flash and movie-mode current is set by one external resistor; the ratio of Flash to Movie-mode current is set at approximately 6.1:1.

An over-voltage protection feature keeps the output voltage below the OVP threshold in case of an open LED and an output short circuit protection limits the output current during an output short to GND. The chip's quiescent current is less than 1.0μA in shutdown mode.

## FEATUES

- 2.7V to 5.5V Input Supply Range
- Dual Channel Output with Separate Flash Enable
- Up to 1.5A Regulated Output Current (750mA per channel)
- Up to 85% Efficiency
- 2 MHz Fixed Switching Frequency
- I<sup>2</sup>C Compliant Serial Interface
  - 400kHz Serial Transfer Rate
  - 16 Level Movie-mode Current
  - Flash/Movie-mode
  - Programmable LED Current
  - Programmable Flash Safety Timer
- True Load Disconnect
- Input Current Limit
- Output Over-Voltage, Short Circuit, and Over-Temperature Protection
- 3mm×3mm TDFN-14 Package
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

## APPLICATIONS

- Camera-enabled Cellular Phones and Smart Phones
- Digital Still Cameras (DSCs)
- LED Photo Flash/Torch

## Typical Application Circuit

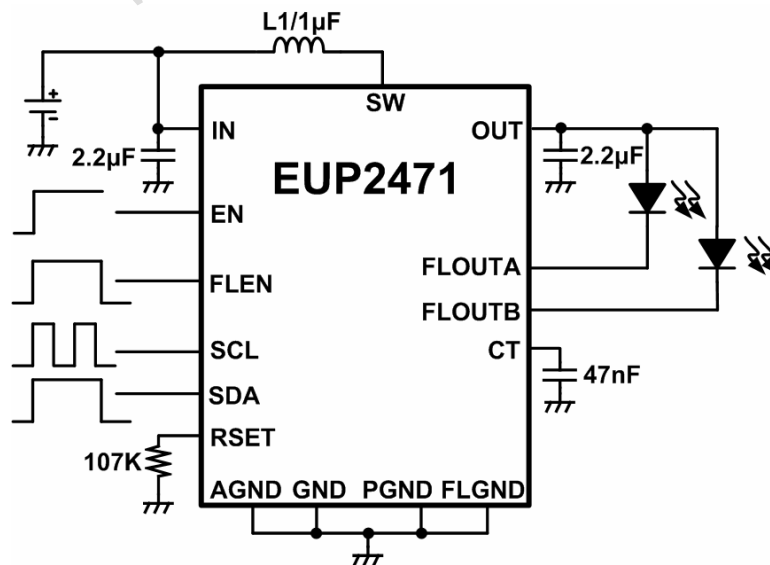


Figure 1. EUP2471 Typical Application

**Pin Configurations**

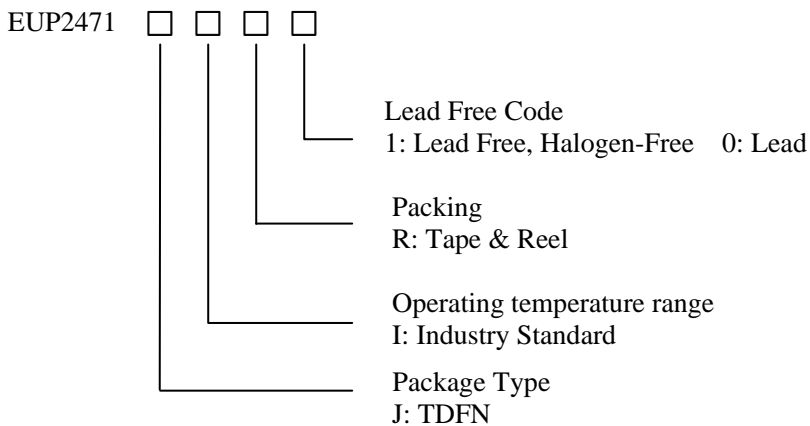
Package Type	Pin Configurations
TDFN-14	<p>(TOP VIEW)</p> <p>The diagram shows a top view of the TDFN-14 package. It is a square package with pins numbered 1 through 14. Pins 1-7 are on the left side, and pins 8-14 are on the right side. A large dashed rectangle in the center is labeled 'Thermal Pad'. The pin functions are listed as follows:</p> <ul style="list-style-type: none"> <li>Pin 1: CT</li> <li>Pin 2: EN</li> <li>Pin 3: FLEN</li> <li>Pin 4: AGND</li> <li>Pin 5: IN</li> <li>Pin 6: SW</li> <li>Pin 7: PGND</li> <li>Pin 8: OUT</li> <li>Pin 9: SCL</li> <li>Pin 10: SDA</li> <li>Pin 11: FLOUTB</li> <li>Pin 12: FLGND</li> <li>Pin 13: FLOUTA</li> <li>Pin 14: RSET</li> </ul>

**Pin Description**

PIN	TDFN-14	DESCRIPTION
1	CT	Flash timer control input. Connect a capacitor between CT and AGND to set maximum duration of the flash pulse. To disable the flash timer, connect CT to AGND.
2	EN	Enable input. EN is an active HIGH asserted input. EN must be strobed low-to-high to enable the EUP2471 to accept I <sup>2</sup> C programming instructions.
3	FLEN	Flash enable pin. A low-to-high transition on the FLEN pin initiates a flash pulse and starts the flash timer.
4	AGND	Analog ground pin. Connect AGND to PGND, GND, and FLGND at a single point as close to the EUP2471 as possible.
5	IN	Power input. Connect IN to the input power supply voltage. Connect a 2.2μF or larger ceramic capacitor from IN to PGND as close as possible to the EUP2471.
6	SW	Boost converter switching node. Connect a 1μH inductor between SW and IN.
7	PGND	Power ground pin. Connect PGND to AGND, GND, and FLGND at a single point as close to the EUP2471 as possible.
8	OUT	Power output of the boost converter. Connect a 2.2μF or larger ceramic capacitor from OUT to PGND as close as possible to the EUP2471. Connect OUT to the anode(s) of the Flash LED(s).
9	SCL	I <sup>2</sup> C interface serial control line.
10	SDA	I <sup>2</sup> C interface serial data/address.
11	FLOUTB	Flash Output B. Connect cathode of Flash LEDB to FLOUTB. For a single flash LED, connect FLOUTB and FLOUTA together. For two flash LEDs, each output will conduct 50% of the total flash output current.
12	FLGND	Flash ground pin. Connect FLGND to PGND, GND, and AGND at a single point as close to the EUP2471 as possible.
13	FLOUTA	Flash Output A. Connect cathode of Flash LEDA to FLOUTA. For a single flash LED, connect FLOUTA and FLOUTB together. For two flash LEDs, each output will conduct 50% of the total flash output current.
14	RSET	Flash current setting input. A 107kΩ resistor from RSET to AGND sets the maximum flash current available at FLOUTA and FLOUTB to 1.5A. Each FLOUTA and FLOUTB channel will conduct 50% of the maximum programmed current. The EUP2471's flash-to-movie-mode ratio is fixed at 6.1:1.
Thermal Pad	-	Thermal paddle (bottom); Connect EP to PGND as close as possible to the EUP2471.

**Ordering Information**

Order Number	Package Type	Marking	Operating Temperature Range
EUP2471JIR1	TDFN-14	XXXXX P2471	-40 °C to +85°C



**Block Diagram**

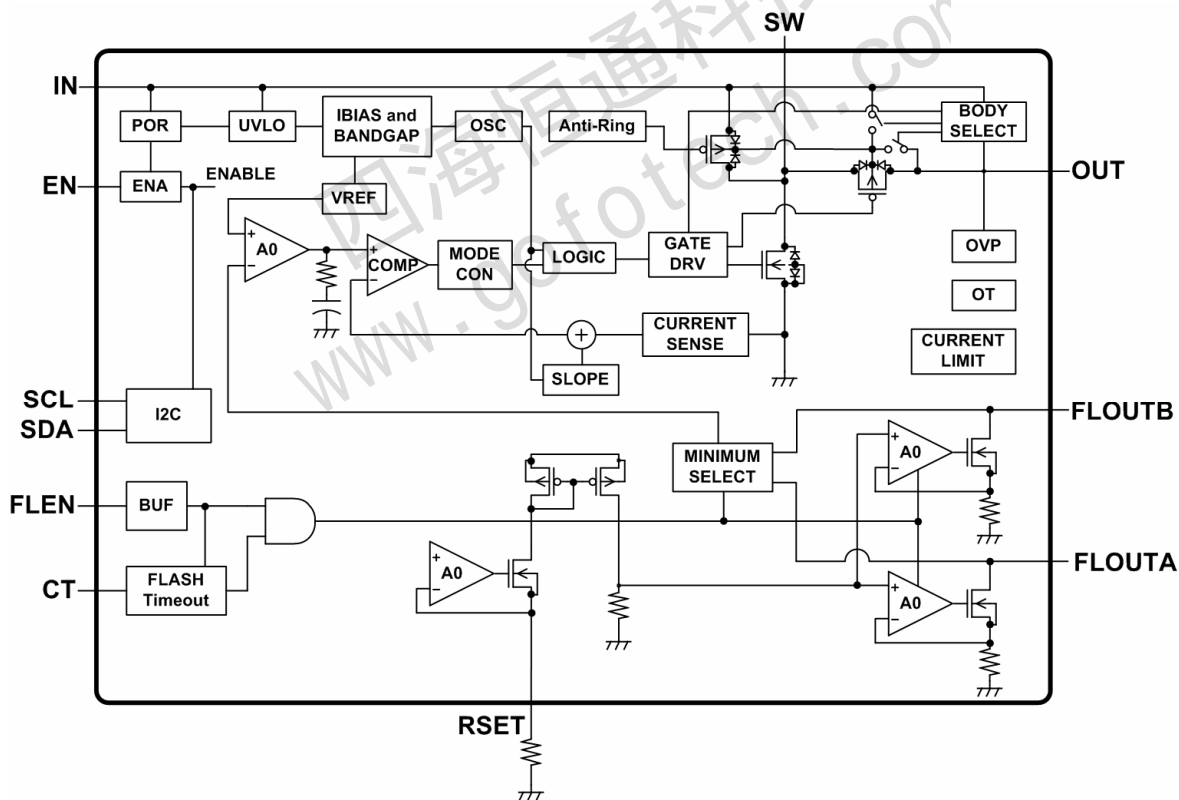


Figure 2. EUP2471 Block Diagram

**Absolute Maximum Ratings**

- IN, SW, OUT ----- -0.3V to 6V
- RSET, EN, FLEN, SDA, SCL, CT, FLOUTA, FLOUTB -----  $V_{IN} + 0.3V$
- Power Dissipation, PD@  $T_A=25^{\circ}C$   
 TDFN-14 ----- 1.923W
- Package Thermal Resistance  
 $\theta_{JA}$  (TDFN-14) -----  $65^{\circ}C/W$
- Junction Temperature Range -----  $-40^{\circ}C$  to  $150^{\circ}C$
- Lead Temperature (Soldering, 10sec.) -----  $260^{\circ}C$
- Storage Temperature Range -----  $-65^{\circ}C$  to  $150^{\circ}C$

**Recommended Operating Conditions**

	Min	Max	Unit
Supply voltage, $V_{IN}$	2.6	5	V
Operating free-air temperature, $T_A$	-40	85	$^{\circ}C$

**Electrical Characteristics**

$V_{IN} = 3.6V$ ,  $C_{IN} = 2.2\mu F$ ,  $C_{OUT} = 2.2\mu F$ ,  $L = 1\mu H$ ,  $R_{SET} = 107k\Omega$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ .

Symbol	Parameter	Conditions	EUP2471			Unit
			Min.	Typ.	Max.	
<b>Power Supply</b>						
$V_{IN}$	Input Voltage Range		2.7		5.5	V
$V_{OUT(MAX)}$	Maximum Voltage				5.5	V
$I_{IN(Q)}$	Supply Current	Flash Mode, $I_{LOAD}=1.5A$		0.48		mA
		Movie Mode		0.45		mA
$I_{SHUTDOWN}$	$V_{IN}$ Shutdown Current	EN=FLEN=GND			1	$\mu A$
$I_{FL(TOTAL)}$	Total Output Current, Flash Mode	$R_{SET} = 107k\Omega$ , FLOUTA + FLOUTB		1.5		A
$I_{FL(MATCH)}$	FLOUTA and FLOUTB Current Matching			10		%
$I_{MM(LOAD)}$	Total Output, Movie Mode	$R_{SET}=107k\Omega$ , Movie Mode Current Set = 100%; FLOUTA + FLOUTB		220		mA
$F_{OSC}$	Switching Frequency	$T_A=25^{\circ}C$		2.0		MHz
$t_{DEFAULT}$	Default On Time	$C_T=74nF$		600		ms
$T_{SD}$	Thermal Shutdown Threshold			140		$^{\circ}C$
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis			15		$^{\circ}C$
<b>I<sup>2</sup>C Control – SDA, SCL</b>						
$V_{IL}$	Input Threshold Low				0.4	V
$V_{IH}$	Input Threshold High		1.4			V
$I_I$	Input Current		-1.0		1.0	$\mu A$
$V_{OL}$	Output Logic Low (SDA)	$I_{PULLUP}=3mA$			0.4	V
$f_{SCL}$	SCL Clock Frequency		0		400	kHz
$t_{LOW}$	SCL Clock Low Period		1.3			$\mu s$
$t_{HIGH}$	SCL Clock High Period		0.6			$\mu s$
$t_{HD\_STA}$	Hold Time START Condition		0.6			$\mu s$
$t_{SU\_STA}$	Setup Time for Repeat START		0.6			$\mu s$

**Electrical Characteristics (Continued)**

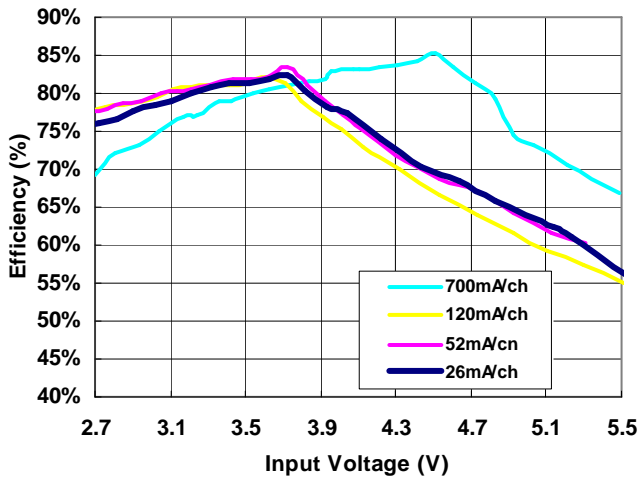
$V_{IN} = 3.6V$ ,  $C_{IN} = 2.2\mu F$ ,  $C_{OUT} = 2.2\mu F$ ,  $L = 1\mu H$ ,  $R_{SET} = 107k\Omega$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ , unless otherwise noted.

Typical values are at  $T_A = 25^{\circ}C$ .

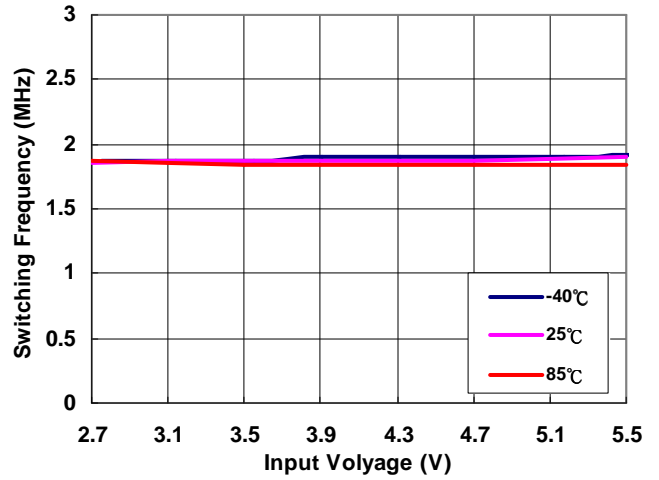
Symbol	Parameter	Conditions	EUP2471			Unit
			Min.	Typ.	Max.	
<b>I<sup>2</sup>C Control – SDA, SCL</b>						
$t_{SU\_DAT}$	SDA Data Setup Time		100			ns
$t_{HD\_DAT}$	SDA Data Hold Time				0.9	$\mu s$
$t_{SU\_STO}$	Setup Time for STOP Condition		0.6			$\mu s$
$t_{BUF}$	Bus Free Time between STOP and START Condition		1.3			$\mu s$
<b>EN, FLEN Logic Control</b>						
$V_{EN(L)}$ , $V_{FLEN(L)}$	EN, FLEN Input Low Threshold				0.4	V
$V_{EN(H)}$ , $V_{FLEN(H)}$	EN, FLEN Input High Threshold		1.4			V
$t_{FLEN\_OND}$	FLEN ON Delay Time	EN= AGND		80		$\mu s$
$t_{FLEN\_OFFD}$	FLEN OFF Delay Time	EN= AGND		2		$\mu s$

**Typical Operating Characteristics**

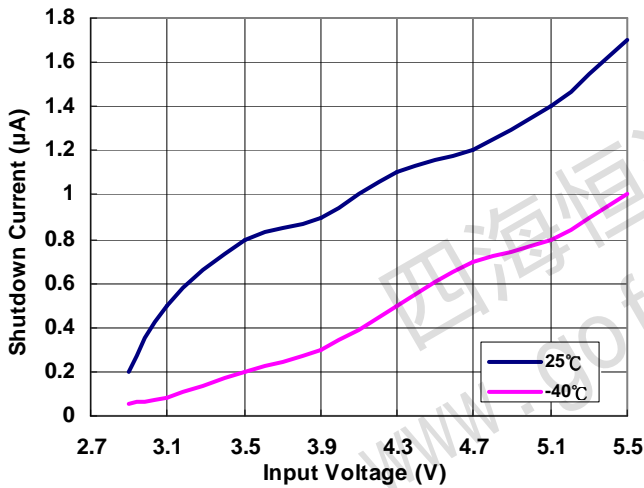
**Efficiency vs. Input Voltage**  
(Movie and Flash Mode)



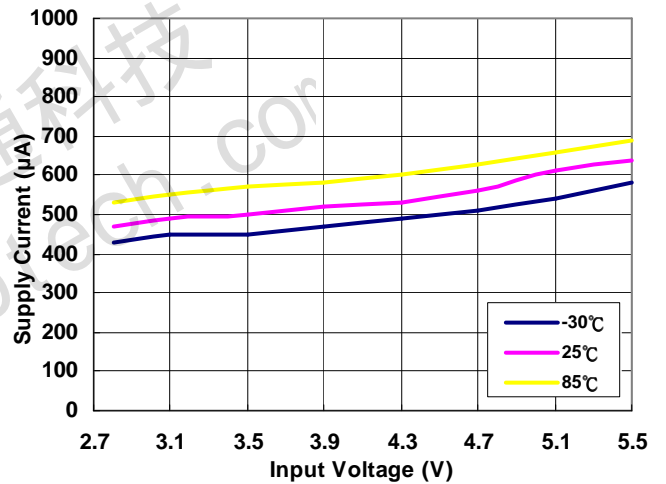
**Boost Switching Frequency vs. Input Voltage**  
(Movie Mode; L=1μH)



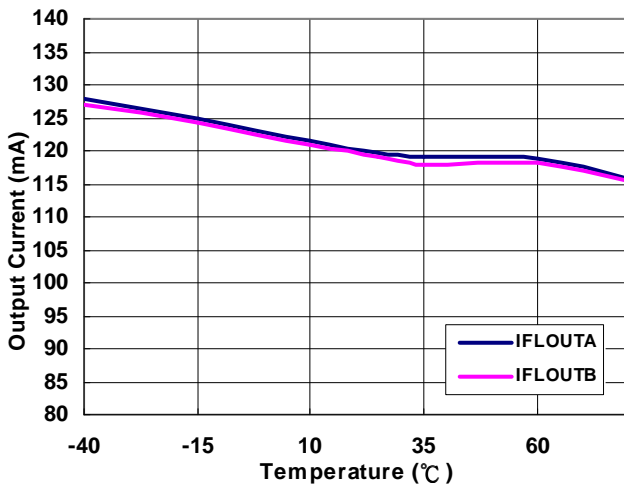
**Shutdown Current vs. Input Voltage**  
(V<sub>EN/SET</sub>=V<sub>FLEN</sub>=0V)



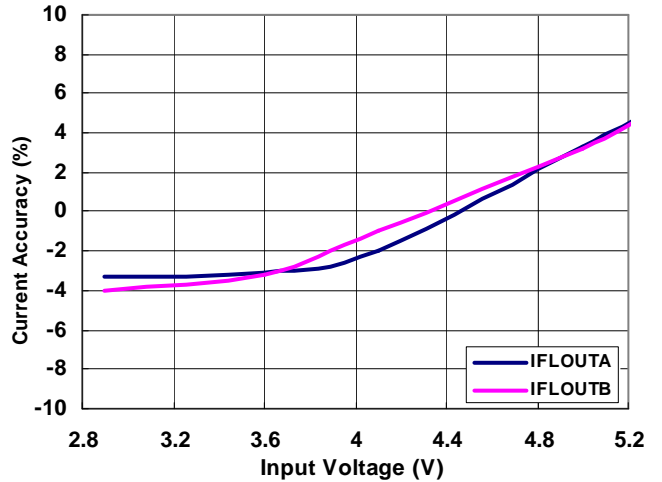
**Supply Current vs. Input Voltage**  
(V<sub>EN</sub>=V<sub>FLEN</sub>=3.6V)



**Movie Mode Current vs. Temperature**  
(I<sub>FLOUTX</sub>=120mA/ch; V<sub>IN</sub>=3.6V; L=1μH)

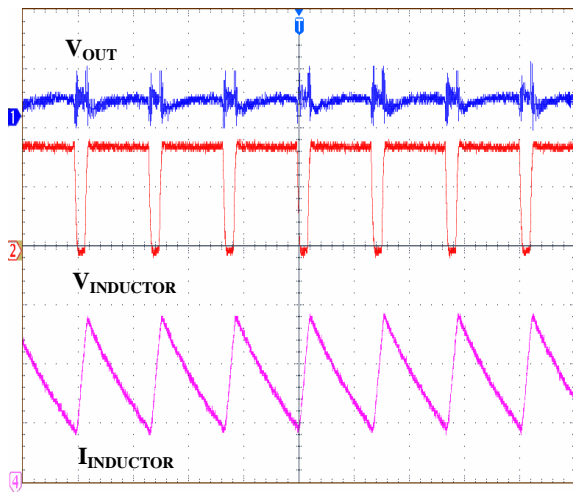


**Movie Mode LED Current Accuracy vs. Input Voltage**  
(I<sub>FLOUTX</sub>=120mA/ch; L=1μH)

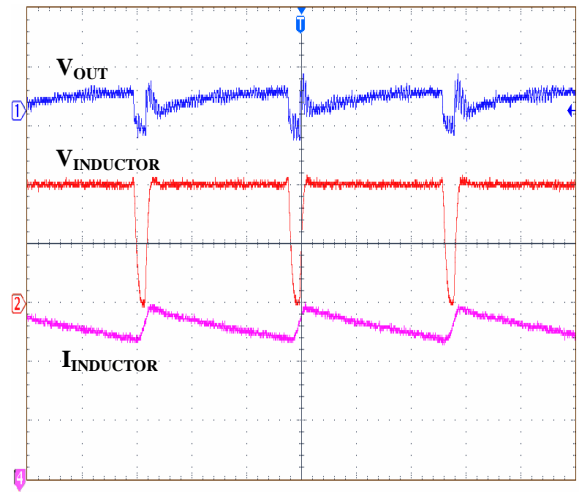


**Typical Operating Characteristics (Continued)**

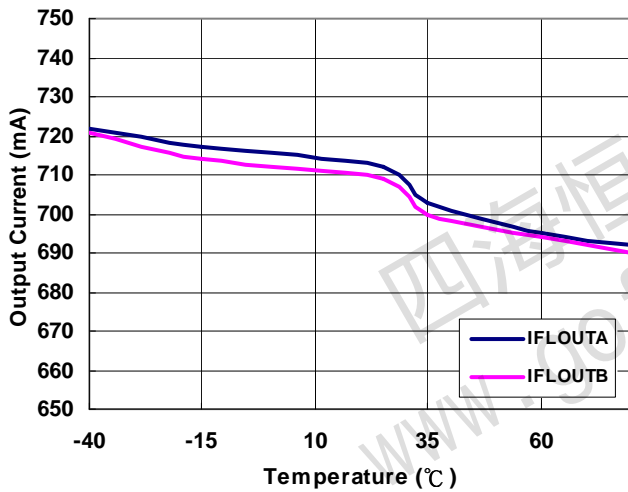
**Movie Mode Output Ripple**  
( $I_{FLOUTX}=120\text{mA/ch}$ ;  $V_{IN}=3.6\text{V}$ ;  $L=1\mu\text{H}$ )



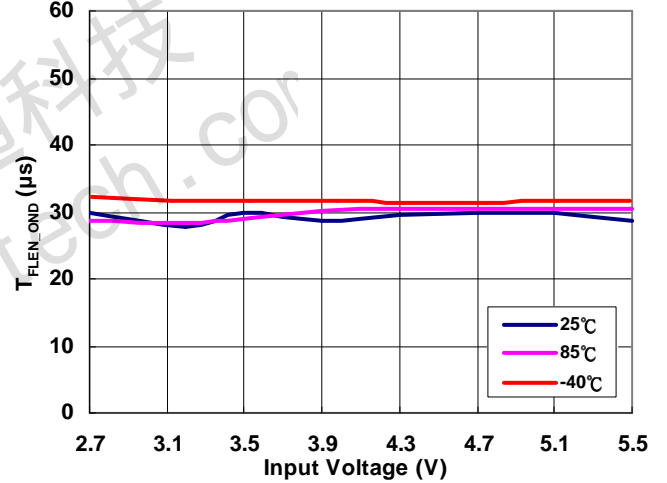
**Flash Mode Output Ripple**  
( $I_{FLOUTX}=750\text{mA/ch}$ ;  $V_{IN}=4\text{V}$ ;  $L=1\mu\text{H}$ )



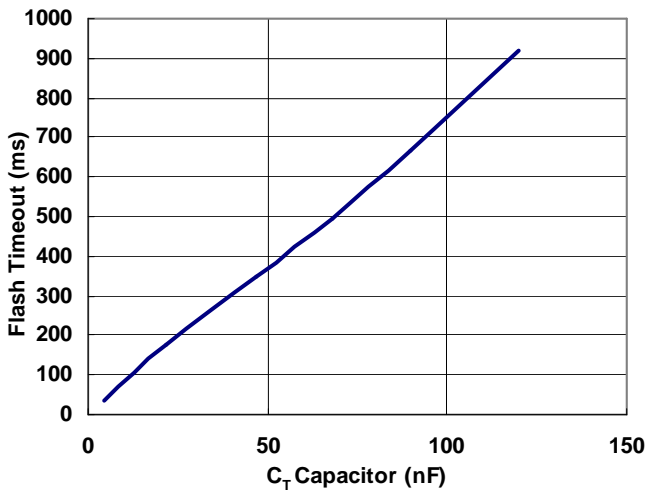
**Flash LED Current Matching vs. Temperature**  
( $I_{FLOUTX}=750\text{mA/ch}$ ;  $V_{IN}=4.2\text{V}$ ;  $L=1\mu\text{H}$ )



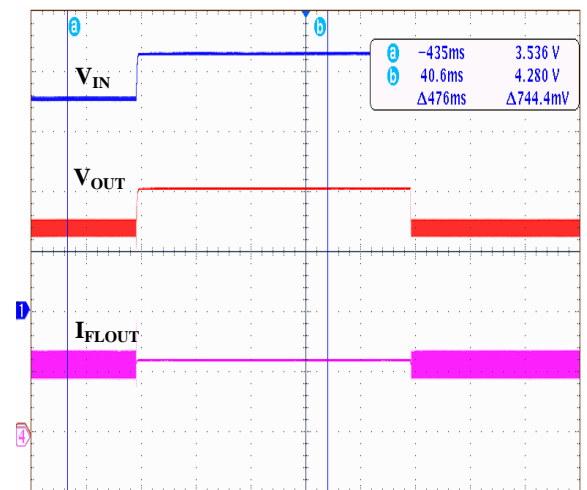
**Flash On Time Delay vs. Input Voltage**  
( $I_{FLOUTX}=750\text{mA/ch}$ ;  $C_{OUT}=2.2\mu\text{F}$ ;  $L=1\mu\text{H}$ )



**Flash Timeout Delay vs.  $C_T$  Capacitor**  
( $I_{FLOUTX}=750\text{mA/ch}$ ;  $V_{IN}=3.6\text{V}$ )

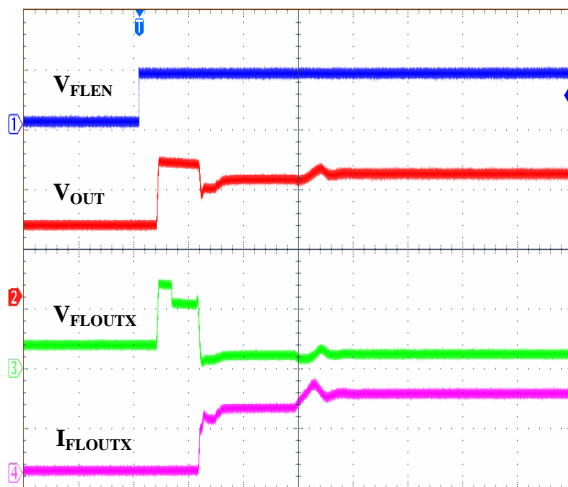


**Movie Mode Line Transient**  
( $I_{FLOUTX}=120\text{mA/Ch}$ ;  $V_{IN}=4.2\text{V to }3.6\text{V}$ )

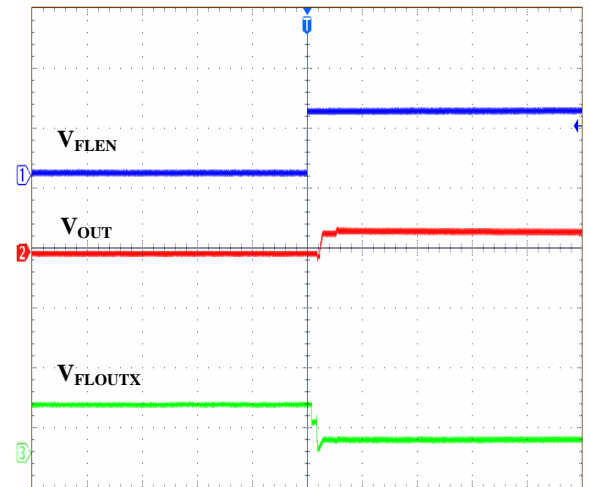


**Typical Operating Characteristics (Continued)**

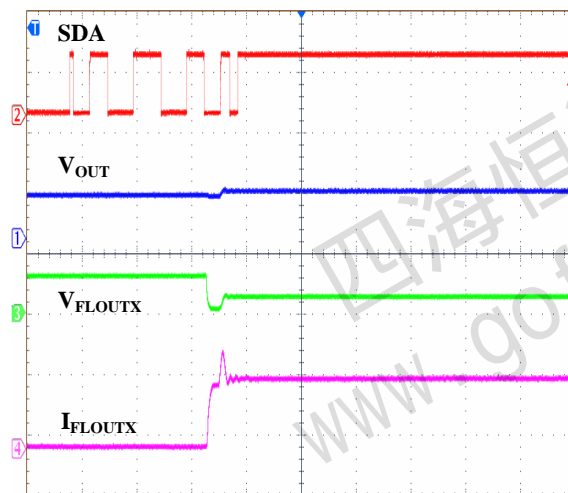
**Flash Turn On Characteristic**  
( $I_{FLOUTX}=750\text{mA/ch}$ ;  $V_{IN}=3.6\text{V}$ ;  $L=1\mu\text{H}$ )



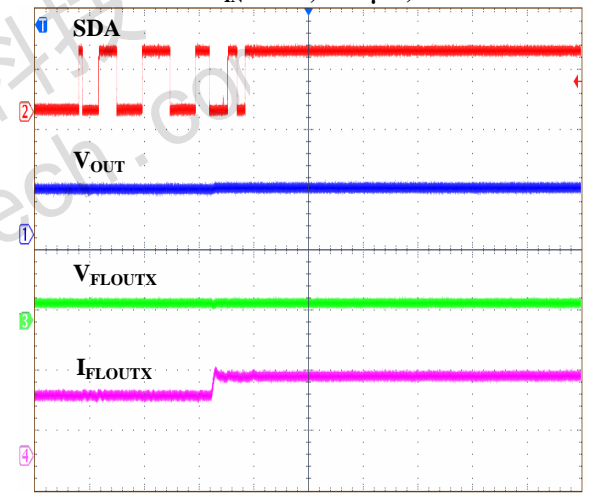
**Movie Mode to Flash Turn On Characteristic**  
( $I_{FLOUTX}=120\text{mA to }750\text{mA/ch}$ ;  $V_{IN}=3.6\text{V}$ ;  $L=1\mu\text{H}$ )



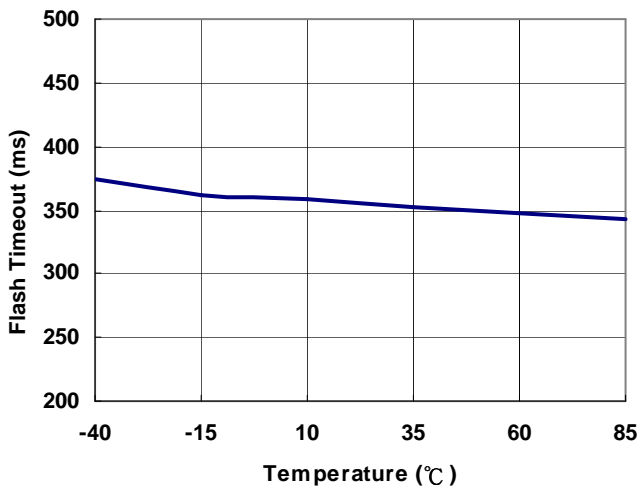
**Movie Mode Turn On Characteristic**  
( $I_{FLOUTX}=120\text{mA/ch}$ ;  $V_{IN}=3.6\text{V}$ ;  $L=1\mu\text{H}$ )



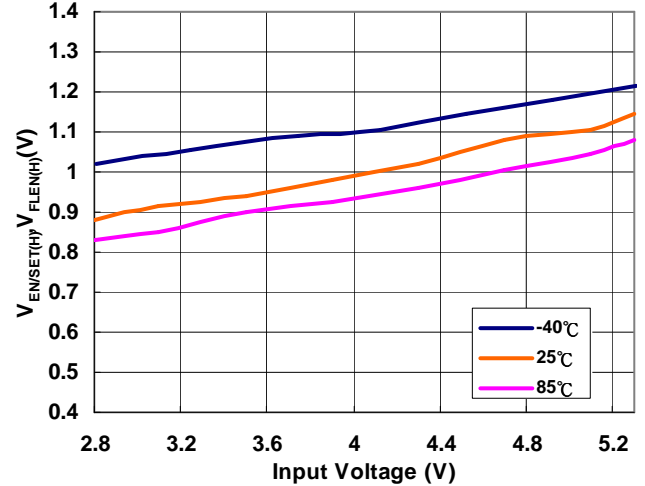
**Movie Mode Transient Characteristic**  
( $I_{FLOUTX}=102\text{mA to }188\text{mA/ch}$ ;  $C_{OUT}=0.22\mu\text{F}$ ;  $V_{IN}=3.6\text{V}$ ;  $L=1\mu\text{H}$ )



**Flash Timeout vs. Temperature**  
( $I_{FLOUTX}=750\text{mA/ch}$ ;  $V_{IN}=3.6\text{V}$ ;  $C_T=47\text{nF}$ )



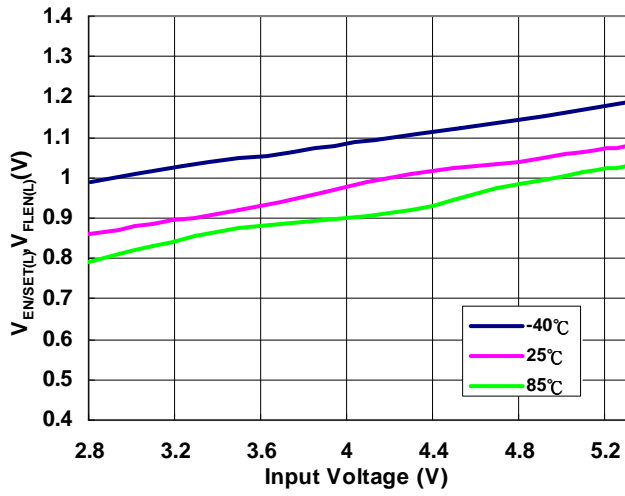
**EN, FLEN High Threshold Voltage vs. Input Voltage**





**Typical Operating Characteristics (Continued)**

**EN, FLEN Low Threshold Voltage  
vs. Input Voltage**



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## Application Information

The EUP2471 is a boost converter with a regulated output current which designed to drive high current white LEDs used in camera flash applications. The maximum flash current is set by an external resistor,  $R_{SET}$ , which sets the flash current and the maximum movie-mode current. The maximum movie-mode current is equal to the maximum programmed flash current divide the programmed flash-to-movie-mode ratio whose default value is 6.1.

A flash pulse is initiated by strobe the FLEN input pin low-to-high, which initiates a flash pulse and also starts the internal timer. The maximum flash current in the EUP2471 is set by an external resistor,  $R_{SET}$ , which sets the flash current and the maximum movie-mode current reduced by a factor of 2. The flash timer will terminate the flash current regardless of the status of the FLEN pin. This can be either used as a simple flash timing pulse or can be used as a safety timer in the event of a control logic malfunction to prevent the LED from over-heating.

The maximum flash time is determined by an external timing capacitor connected to the  $C_T$  pin. The flash duration can be set from 50ms up to a maximum of 1s which determined by customer. The I<sup>2</sup>C-compliant interface allows further adjustment of the flash timer duration. This allows the flash timer duration to be reduced in 16 linear steps from the maximum time set by the timing capacitor. If the safety timer is not needed in the application, it can be disabled by connecting the  $C_T$  pin directly to AGND.

The EUP2471 has two LED current sources which share the output current equally. For a single white LED application, the two current sources can be connected together to apply full output current into the LED. In two LED applications, each diode can be connected to its corresponding current source (FLOUTA or FLOUTB) and the output current will be shared. In applications where only one LED is connected to either FLOUTA or FLOUTB, the unused current sink must be directly connected to OUT, thereby disable that channel.

### Movie Mode

The movie mode current level, the flash safety timer, the output channel enable, and the flash-to-movie mode current ratio can be set through the EUP2471's I<sup>2</sup>C-compliant interface. The movie-mode current level can be adjusted in 16 steps using a logarithmic scale where each code is 1dB below the previous code. The flash safety delay can be reduced from the maximum value programmed externally by  $C_T$  in 16 linear steps. The flash current outputs FLOUTA and FLOUTB can be enabled or disabled individually or together. The flash-to-movie-mode current ratio can be set from 1:2 to 1:17 with respect to the maximum programmed flash current. The FLEN signal takes priority over movie-mode operation. Lastly, the EN pin must be toggled low-to-high to enable the EUP2471 to accept I<sup>2</sup>C programming instructions.

### Over-Temperature Protection

Thermal protection disables the EUP2471 when internal power dissipation becomes excessive, as it disables both MOSFETs. The junction over-temperature threshold is 140°C with 15°C of temperature hysteresis. The output voltage automatically recovers when the over-temperature fault condition is removed.

### Over-Voltage Protection (Open LED, Open Circuit)

The EUP2471's output voltage is limited by internal over voltage protection circuitry, which prevents damage to the EUP2471 from open LED or open circuit conditions. During an open circuit, the output voltage rises and reaches 5.5V (typical), and the OVP circuit disables the switching, preventing the output voltage from rising higher. Once the open circuit condition is removed, switching will resume. The controller will return to normal operation and maintain an average output voltage.

### LED Selection

The EUP2471 is specifically designed to drive white flash LEDs (typical forward voltage of 2.5V to 4.0V). Since the FLOUTA and FLOUTB input current sinks are matched with low voltage dependence; the LED-to-LED brightness will be matched regardless of the individual LED forward voltage ( $V_F$ ) levels.

### Flash Mode LED Current

The LED current is controlled by the RSET resistor. For maximum accuracy, a 1% tolerance resistor is recommended. FLOUTA and FLOUTB can be programmed up to a maximum total flash current of 1.5A or up to 750mA per channel. FLOUTA and FLOUTB output current is matched across the programming range. A flash event is initiated by asserting the FLEN pin. A flash event is automatically terminated when FLEN is disabled or if the safety timer terminates before the FLEN pin is disabled.

The maximum flash current in each FLOUTA and FLOUTB is set by the  $R_{SET}$  resistor and can be calculated using the following equation:

$$I_{FLOUTA} = I_{FLOUTB} = \frac{81K\Omega \cdot A}{R_{SET}} = \frac{81K\Omega \cdot A}{107K\Omega} \cong 750mA$$

per channel

To prevent excessive power dissipation during higher flash current operation,  $R_{SET}$  values smaller than 107k $\Omega$  are not recommended.

### Auto-Disable Feature Movie Mode LED Current

The EUP2471 is equipped with an auto-disable feature for each LED channel. After the IC is enabled and started up, a test current of 2-3mA (typical) is forced through each sink channel. The channel will be disabled if the voltage of that particular SINK pin does not drop to a certain threshold. This feature is very convenient for disabling an unused channel or during an LED fail-short event. This small test current should be added to the set

output current in both Flash and MM conditions. The maximum movie-mode current level is set by the maximum programmed flash current reduced by the programmed flash-to-movie-mode ratio in which the default value is 6.1:

$$I_{\text{MOVIE-MODE}[A/B]} = \frac{I_{\text{FLOUT}[A/B](\text{MAX})}}{6.1} = \frac{750\text{mA}}{6.1} \cong 120\text{mA}$$

To change the configuration or the settings, the EUP2471 can be programmed via the I<sup>2</sup>C interface. Triggering the FLEN low to high will enable a flash event with the maximum flash current set by the R<sub>SET</sub> resistor or with programmed flash current set via the I<sup>2</sup>C interface. Concurrently, the flash timer is also initiated. All data and register contents are cleared (reset to the default value) after each flash event.

### Flash Safety Timeout

The EUP2471 includes a timer circuit that enables the flash current for a programmed period of time. This feature eliminates the need for an external, housekeeping baseband controller to contain a safety delay routine. It also serves as a protection feature to minimize thermal issues with the flash LEDs in the event an external controller's flash software routine experiences hang-up or freeze. The flash safety timeout, T can be calculated by the following equation:

$$T = 7.98\text{s}/\mu\text{F} \cdot C_T$$

Where T is in seconds and C<sub>T</sub> is the capacitance of the timer capacitor in μF.

For example, using a 47nF capacitor for C<sub>T</sub> sets the flash timeout to:

$$\text{Flash Safety Timeout} = 7.98\text{s}/\mu\text{F} \cdot 0.047\mu\text{F} = 375\text{ms}$$

The relationship between the flash safety timeout and the capacitance of the timer capacitor is illustrated in Flash Timeout Delay VS C<sub>T</sub> Capacitance.

### I<sup>2</sup>C Serial Interface

The EUP2471 is fully compliant with the industry-standard I<sup>2</sup>C interface. The I<sup>2</sup>C two-wire communications bus consists of SDA and SCL lines. SDA provides data, while SCL provides clock synchronization with speed up to 400kHz. SDA data transfers device address followed by a register address and data bits sequence. When using the I<sup>2</sup>C interface, EN is pulled high to enable the device or low to disable the device. The I<sup>2</sup>C serial interface requires a master to initiate all the communications with target devices. The EUP2471 is a target device and only supports the write protocol. The EUP2471 is manufactured with a target device address of 0×37 (Hex). See Figure 3 for the I<sup>2</sup>C interface diagram.

### I<sup>2</sup>C START and STOP Conditions

START and STOP conditions are always generated by the master. Prior to initiating a START, both the SDA and SCL pins are in idle mode (idle mode is when there is no activity on the bus and SDA and SCL are pulled high by the external pull-up resistors). A START condition occurs when the master strobes the SDA line low and after a short period strobes the SCL line low. A START condition acts as a signal to all ICs that transmission activity is about to occur on the I<sup>2</sup>C bus. A STOP condition, as shown in Figure 4, is when master releases the bus and SCL changes from low to high followed by SDA low-to-high transition. The master does not issue an ACKNOWLEDGE and releases the SCL and SDA pins.

### I<sup>2</sup>C Address Bit Map

Figure 5 illustrates the address bit transfer. The 7-bit address is transferred with the Most Significant Bit (MSB) first and is valid when SCL is high. This is followed by the R/W bit in the Least Significant Bit (LSB) location. The R/W bit on the eighth bit determines the direction of the transfer (a '1' for read or a '0' for write). The EUP2471 is a write-only device and the R/W bit must be set low. The Acknowledge bit (ACK) is set to low by the EUP2471 to acknowledge receipt of the address.

### I<sup>2</sup>C Register Address/Data Bit Map

Figure 6 illustrates the Register Address or the serial data bit transfer. The 8-bit data is always transferred most significant bit first and is valid when SCL is high. The Acknowledge bit (ACK) is set low by the EUP2471 to acknowledge receipt of the register address or the data.

### I<sup>2</sup>C Acknowledge Bit (ACK)

The Acknowledge bit is the ninth bit of each transfer on the SDA line. It is used to send back a confirmation to the master that the data has been received properly by the target device. For each ACK to take place, the master must first release the SDA line, and then the target device will pull the SDA line low, as shown in Figures 3, 5, and 6.

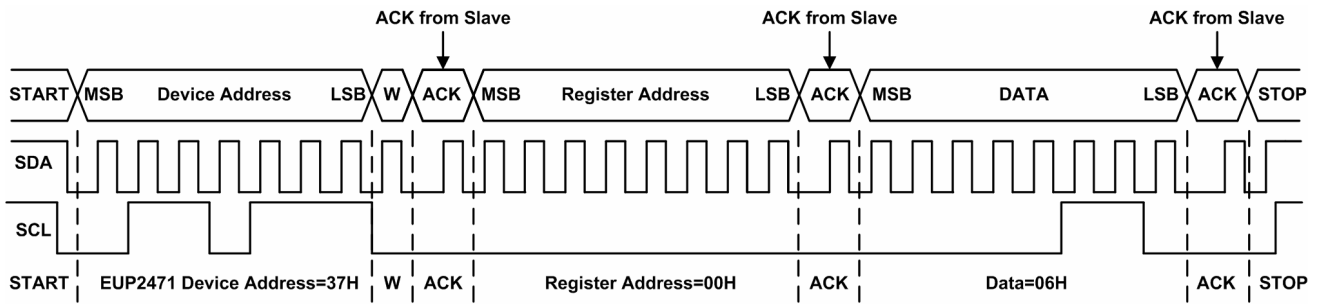


Figure 3. I<sup>2</sup>C Interface Diagram



Figure 4. I<sup>2</sup>C STOP and START Conditions

START: A High “1” to Low “0” Transition on the SDA Line While SCL is High “1”  
 STOP: A Low “0” to High “1” Transition on the SDA Line While SCL is High “1”

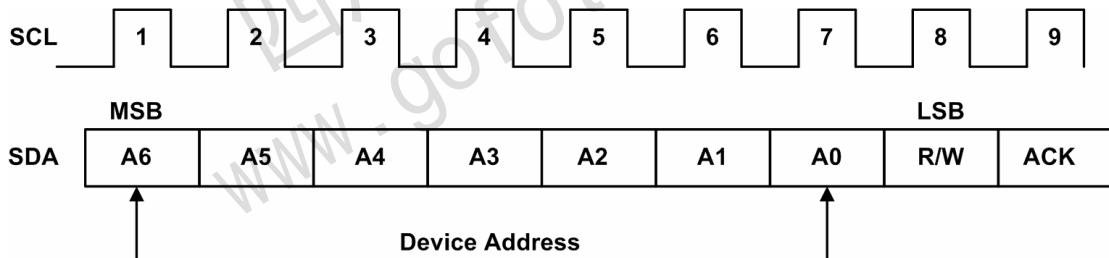


Figure 5. I<sup>2</sup>C Address Bit Map

7-bit Slave Address (A6-A0), 1-bit Read/Write (R/W), 1-bit Acknowledge (ACK)

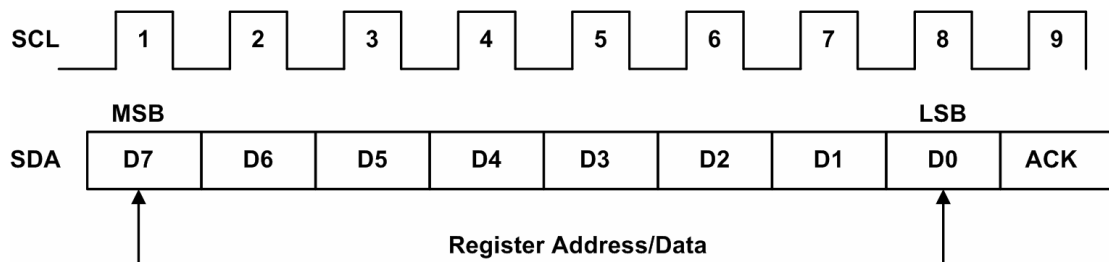


Figure 6. I<sup>2</sup>C Register Address and Data Bit Map

8-bit Data (D7-D0), 1-bit Acknowledge (ACK)

**Device Register Information**

To program the register through the I<sup>2</sup>C interface, the master needs to send the EUP2471’s device address, 0×37 (Hex), first, and then sends an 8-bit register address and 8-bit data. The EUP2471 has two registers, Register 0 and Register 1. If no instruction is written to the register, the default value is applied.

**Register 0 (REG0), Register Address: 00h**

Bits [7:4] Program the movie-mode current with 16 different percentage levels.

Bits [3:0] Program the flash safety timeout with 16 different fractions from the hardware configuration, C<sub>T</sub>.

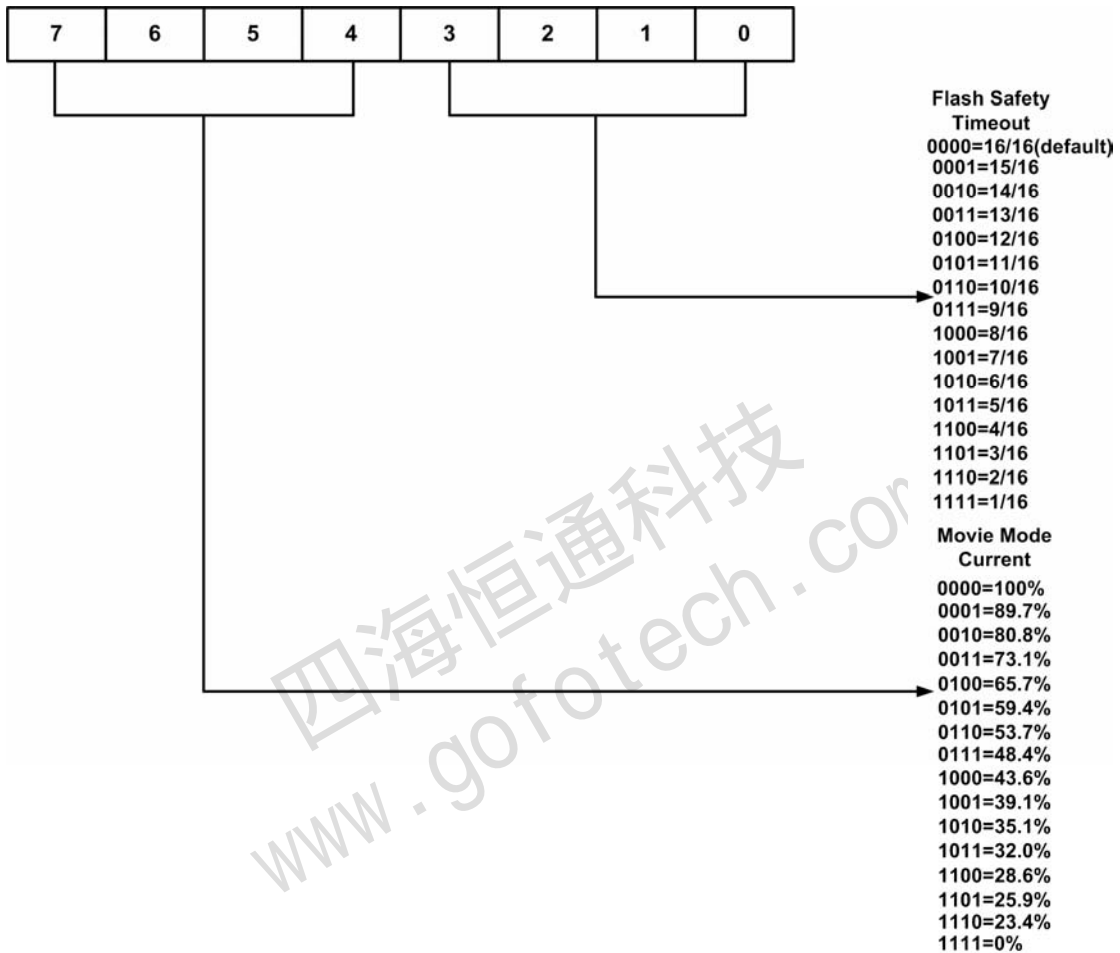


Figure 7: EUP2471 Register 0 Programming.

**Register 1 (REG1); Register Address: 01h**

Bits [5:4] Program the FLOUTA and FLOUTB with four ON/OFF configurations.

Bits [3:0] Program the flash-to-movie mode ratio with 16 different fractions from the hardware configuration,  $R_{SET}$ .

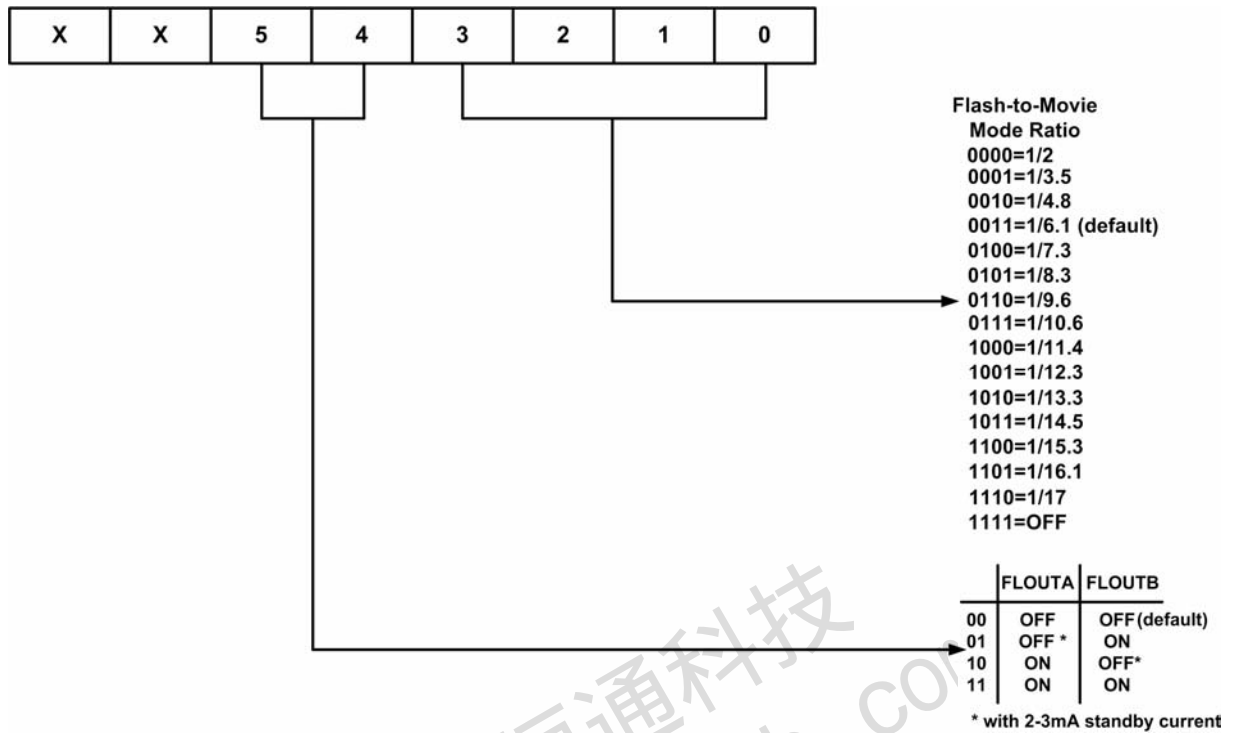


Figure 8: EUP2471 Register 1 Programming.



## Selecting the Boost Inductor

The EUP2471 controller utilizes PWM control and the switching frequency is fixed. To maintain 2MHz maximum switching frequency and stable operation, a 1μH inductor is recommended. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and peak inductor current rating, which is determined by the saturation characteristics. Measurements at full load and high ambient temperature should be performed to ensure that the inductor does not saturate or exhibit excessive temperature rise.

The inductor (L) is selected to avoid saturation at minimum input voltage and maximum output load conditions. Worst case peak current occurs at minimum input voltage (maximum duty cycle) and maximum load. Bench measurements are recommended to confirm actual I<sub>PEAK</sub> and to ensure that the inductor does not saturate at maximum LED current and minimum input supply voltage. The RMS current flowing through the boost inductor is equal to the DC plus AC ripple components. Under worst case RMS conditions, the current waveform is critically continuous. The resulting RMS calculation yields worst case inductor loss. The RMS current value should be compared against the inductor manufacturer's temperature rise, or thermal derating guidelines:

$$I_{\text{RMS}} = \frac{I_{\text{PEAK}}}{\sqrt{3}}$$

For a given inductor type, smaller inductor size leads to an increase in DCR winding resistance and, in most cases, increased thermal impedance. Winding resistance degrades boost converter efficiency and increases the inductor's operating temperature:

$$P_{\text{LOSS(INDUCTOR)}} = I_{\text{RMS}}^2 \cdot \text{DCR}$$

## Selecting the Boost Capacitors

In general, it is good design practice to place a decoupling capacitor (input capacitor) between the IN and GND pins. An input capacitor in the range of 2.2μF to 10μF is recommended. A larger input capacitor in this application may be required for stability, transient response, or ripple performance. The high output ripple inherent in the boost converter necessitates the use of low impedance output filtering. Multi-layer ceramic (MLC) capacitors provide small size and adequate capacitance, low parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL), and are well suited for use with the EUP2471 boost regulator. MLC capacitors of type X7R or X5R are recommended to ensure good capacitance stability over the full operating temperature range. The output capacitor is selected to maintain the output load without significant voltage droop (ΔV<sub>OUT</sub>) during the power switch ON interval. A 2.2μF ceramic output capacitor is recommended. Typically, 6.3V or 10V rated capacitors are required for this flash LED boost output. Ceramic capacitors selected as small as 0603 are available which

meet these requirements. MLC capacitors exhibit significant capacitance reduction with applied voltage. Output ripple measurements should confirm that output voltage droop and operating stability are within acceptable limits. Voltage derating can minimize this factor, but results may vary with package size and among specific manufacturers. To maintain stable operation at full load, the output capacitor should be selected to maintain ΔV<sub>OUT</sub> between 100mV and 200mV. The boost converter input current flows during both ON and OFF switching intervals. The input ripple current is less than the output ripple and, as a result, less input capacitance is required.

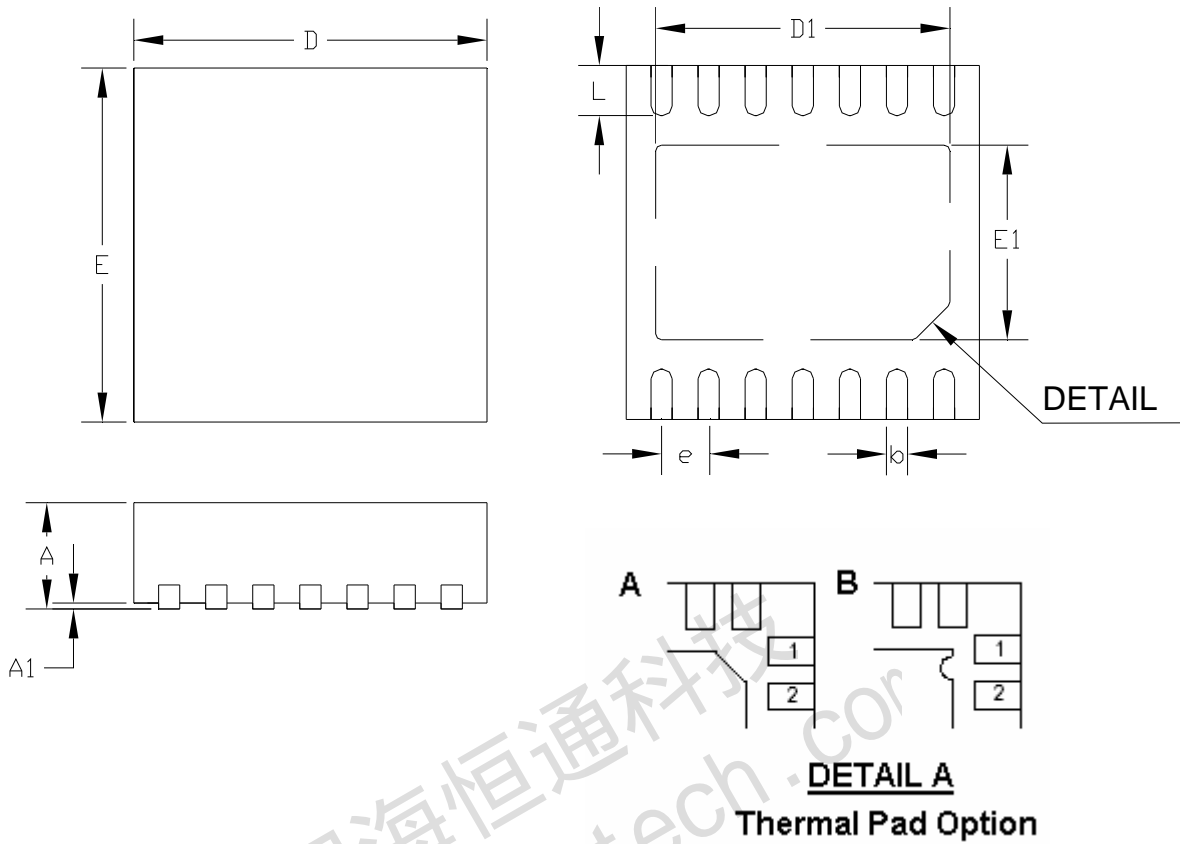
## PCB Layout Guidelines

Boost converter performance can be adversely affected by poor layout. Possible impact includes high input and output voltage ripple, poor EMI performance, and reduced operating efficiency. Every attempt should be made to optimize the layout in order to minimize parasitic PCB effects (stray resistance, capacitance, and inductance) and EMI coupling from the high frequency SW node. The following PCB layout guidelines should be considered:

1. Minimize the distance from capacitor C<sub>IN</sub> and C<sub>OUT</sub>'s negative terminals to the PGND pins. This is especially true with output capacitor C<sub>OUT</sub>, which conducts high ripple current from the output to the PGND pins.
2. Minimize the distance under the inductor between IN and switching pin SW; minimize the size of the PCB area connected to the SW pin.
3. Maintain a ground plane and connect to the IC PGND pin(s) as well as the PGND connections of C<sub>IN</sub> and C<sub>OUT</sub>.
4. Consider additional PCB exposed area for the flash LEDs to maximize heat sinking capability. This may be necessary when using high current application and long flash duration application.
5. Connect the exposed paddle (bottom of the die) to either PGND or GND. Connect AGND, FLGND to GND as close as possible to the package.

**Package Information**

**TDFN-14**



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.13	0.23	0.008	0.014
E	2.90	3.10	0.114	0.122
D	2.90	3.10	0.114	0.122
D1	2.50		0.098	
E1	1.65		0.065	
e	0.40		0.016	
L	0.30	0.50	0.012	0.020