LZ95D52/M

Synchronous Signal Genertor LSI for CCD

DESCRIPTION

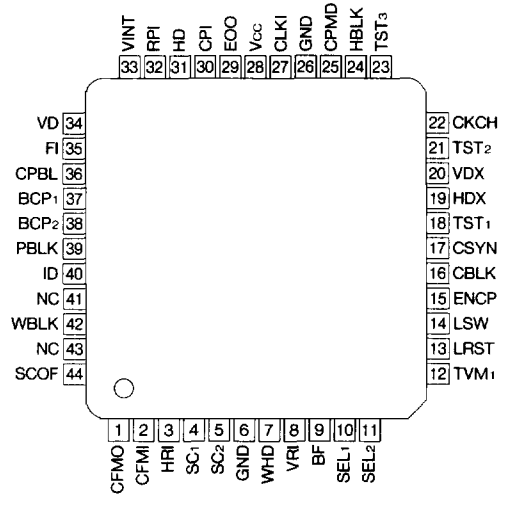
The LZ95D52/M is a CMOS synchronous signal generator LSI which provides TV synchronous pulses and video signal processing pulses in combination with the timing signal generator LSI (LZ95D42/M or LZ95D71M).

FEATURES

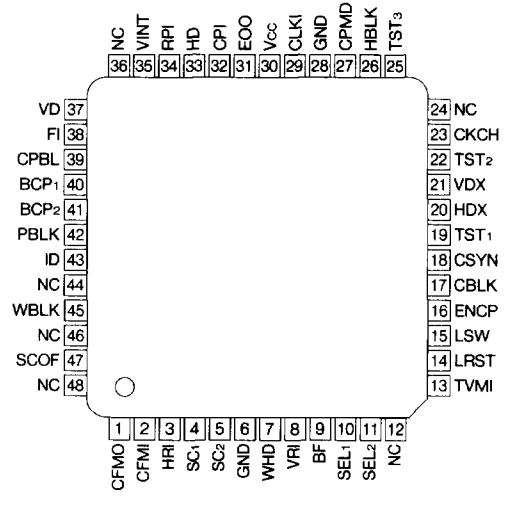
- Switchable between 410 000 pixels CCD and 470 000 pixels CCD
- Switchable between NTSC (EIA) and PAL (CCIR) systems
- Included phase comparator circuit
- In NTSC mode, switchable between subcarrier generate and subcarrier stop
- Non-interlace mode is possible
- Switchable between two timing LSI (LZ95D42/M, LZ95D71M)
- External synchronization is possible
- Single +5 V power supply
- Packages :
  LZ95D52 : 44-pin QFP(QFP044-P-1010)
  LZ95D52M : 48-pin QFP(QFP048-P-0707)

PIN CONNECTIONS

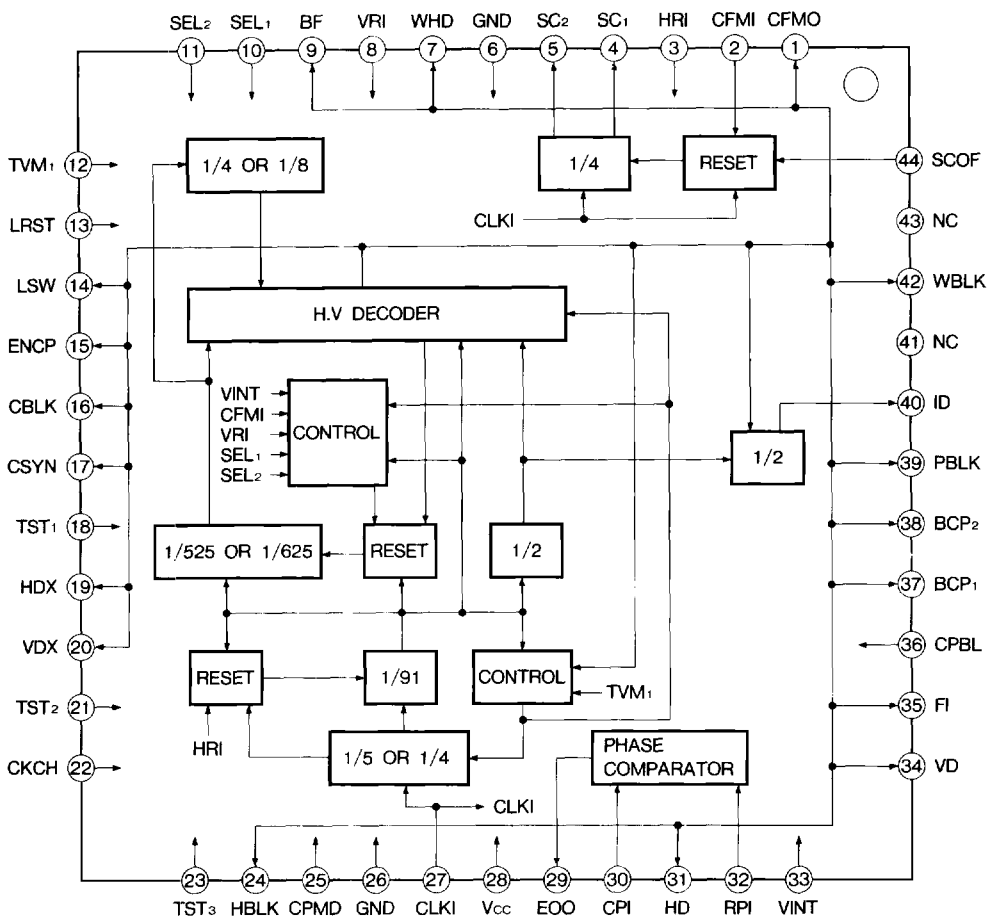
44-PIN QFP TOP VIEW



48-PIN QFP



BLOCK DIAGRAM



NOTE :
Pin numbers apply to the 44-pin QFP.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{CC}+0.3	V
Output voltage	V_O	−0.3 to V_{CC}+0.3	V
Operation temperature	Topr	−20 to +70	°C
Storage temperature	Tstg	−55 to +150	°C

DC CHARACTERISTICS

(V_{CC} = +5 V±5%, Ta = −20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V_{IL}				1.5	V	1
Input High voltage	V_{IH}		3.5			V	
Input High threshold voltage	V_{T+}				3.7	V	2
Input Low threshold voltage	V_{T-}		1.0			V	
Hysteresis voltage	$V_{T+}-V_{T-}$		0.4			V	
Input Low current	$\lvert I_{IL1} \rvert$	V_I = 0 V			1.0	μA	3
	$\lvert I_{IL2} \rvert$	V_I = 0 V	8.0		60	μA	4
Input High current	$\lvert I_{IH1} \rvert$	$V_I = V_{CC}$			1.0	μA	5
	$\lvert I_{IH2} \rvert$	$V_I = V_{CC}$	8.0		60	μA	6
Output High voltage	V_{OH1}	I_{OH} = −2 mA	4.0			V	7
Output High voltage	V_{OH2}	I_{OH} = −6 mA	4.0			V	8
Output Low voltage	V_{OL1}	I_{OL} = 4 mA			0.4	V	7
Output Low voltage	V_{OL2}	I_{OL} = 12 mA			0.4	V	8
Leak output current	$\lvert I_{OZ} \rvert$	High-Z			1.0	μA	

NOTE :

1. Applied to inputs (IC, ICD, ICU).
2. Applied to schmitt-trigger input (ICSU).
3. Applied to inputs (IC, ICD).
4. Applied to inputs (ICU, ICSU).
5. Applied to inputs (IC, ICU, ICSU).
6. Applied to input (ICD).
7. Applied to all outputs (O).
8. Applied to tri-state output (TO).

PIN FUNCTION (Pin numbers apply to 44-pin QFP)

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	CFMO	O	⎍	Color frame output	A pulse to control color frame; Occurs at every 4 fields in NTSC mode, occurs at every 8 fields in PAL mode.
2	CFMI	ICD	–	Color frame reset input	An input pin for color frame signal; Connect to external color frame signal in External Synchronous mode. Connect to CFMO (pin 1) in Internal Synchronous mode or Initialize mode with VINT (pin 33).
3	HRI	ICSU	–	Horizontal reset input	An input pin for resetting internal horizontal counter. Set open or to H level when not resetting.
4	SC_1	O	⎍⎍	Subcarrier output 1	An output pin for color subcarrier in NTSC mode. The frequency of the signal is 1/4 the CLKI (pin 27) frequency. The signal is reset by color frame pulse CFMI (pin 2). When the SCOF (pin 44) is H level or in PAL mode, it is held at L level.
5	SC_2	O	⎍⎍	Subcarrier output 2	An output pin for color subcarrier in NTSC mode. When the phase of SC_1 (pin 4) is 180 degree, the phase of SC_2 is 90 degree in NTSC mode. When the SCOF (pin 44) is H level or in PAL mode, it is held at L level.
6	GND	–	–	Ground	A grounding pin.
7	WHD	O	⎍	Wide Horizontal drive pulse	An output pin for wide Horizontal drive pulse. The pulse width is equal to that of PBLK (pin 39) and the repetition is horizontal frequency.
8	VRI	ICSU	–	Vertical reset input	An input pin for resetting internal vertical counter. The input pulse is necessary 1/2 horizontal max. delay from vertical synchronous start point, because VRI is counted by 2 times horizontal frequency. Set open or to H level when not resetting.
9	BF	O	⎍ or ⎎	Burst flag	A pulse to define burst period. When CKCH (pin 22) is L level, the polarity is positive, and when CKCH is H level, the polarity is negative.
10	SEL_1	ICD	–	Non-interlace mode select 1	These inputs pin to select Interlace mode or Non-interlace mode. at Internal Synchronous mode. And in Non-interlace mode, switchable TV lines.
11	SEL_2	ICD	–	Non-interlace mode select 2	

SEL_1	L	H	L	H
SEL_2	L	L	H	H
TV mode	Interlace	Non-interlace		
NTSC	262.5H	260H	261H	262H
PAL	312.5H	310H	311H	312H

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
12	TVM_1	ICD	–	TV mode select	An input pin to select TV standards. TVM_1: L → TV mode: NTSC; H → PAL
13	LRST	ICU	–	Line switch reset	The input resets the output from LSW (pin 14). Set open or to H level when not used.
14	LSW	O	⊓	Line switch	The signal switches between H and L at every line in PAL mode. It is set at Low level at the 1st line of the 1st field.
15	ENCP	O	⊓	Encoder DC clamp pulse	A clamp pulse that is used for recovering DC level. The repetition is horizontal frequency. When CKCH (pin 22) is H level, the phase is change.
16	CBLK	O	⊓ or ⊔	Composite blanking pulse	Composite blanking pulses. In NTSC mode; H : 10.97 μs, V : 20 H period In PAL mode; H : 12.12 μs, V : 25 H period When CKCH (pin 23) is L level, the polarity is positive, and when CKCH is H level, the polarity is negative.
17	CSYN	O	⊔	Composite syncronus signal	A composite synchronous signal that comforms to RS-170 in NTSC mode and to CCIR in PAL mode.
18	TST_1	ICD	–	Test terminal 1	A pin for tests. Set open or to L level in the Normal mode.
19	HDX	O	⊔	Horizontal drive pulse2	The pulse occurs at the start of lines and invert pulse of HD (pin 31). When LZ95D71M is used for timing LSI, connect to HDI of timing LSI.
20	VDX	O	⊔	V drive pulse 2	The pulse occurs at the start of every field and invert pulse of VD (pin 34). When LZ95D71M is used for timing LSI, connect to VDI of timing LSI.
21	TST_2	ICD	–	Test terminal 2	A pin for tests. Set open or to L level in the Normal mode.
22	CKCH	ICD	–	Clock polarity select	An input pin to select main clock polariy. When LZ95D42/M is used for timing LSI, set to L level, and LZ95D71M is used, set to H level. The polarity of CBLK (pin 16), PBLK (pin 39), BF (pin 9) and WBLK (pin 42) change, and the phase of ENCP (pin 15) and HBLK (pin 24) change with input level.
23	TST_3	ICD	–	Test terminal 3	A pin for tests. Set open or to L level in the Normal mode.
24	HBLK	O	⊔	Horizontal blanking pulse	When CKCH (pin 22) is L level, pulse that correspondes to the cease period of the horizontal transfer pulse. When CKCH is H level, pulse is gate pulse of burst-flag.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
25	CPMD	ICU	–	Clamp Pulse mode select	An input pin to stop or to continue BCP_1 (pin 37) and BCP_2 (pin 38) pulses within the vertical blanking period. L level : continuous output. Open or H level : becomes Low level during the absence of effective pixels within V blanking period.
26	GND	–	–	Ground	A grounding pin.
27	CLKI	IC	⎍⎍	Main clock	An input pin for reference clock. Connect to timing LSI : Following frequencies appear on this pin; At NTSC mode : 14.318 18 MHz when TVM_1=L level At PAL mode : 14.187 5 MHz when TVM_1=H level
28	Vcc	–	–	Power supply	Supply +5 V power.
29	EOO	TO	–	Phase comparator output	Phase comparator output for input signals RPI (pin 32) and CPI (pin 30). When CPI is advanced, output is Low level. When CPI is delayed, output is High level. When phases are equal, the terminal impedance is High.
30	CPI	ICD	–	Horizontal comparison input	An input pin for comparison signal to the phase comparator. Set open or to L level when comparator is not used.
31	HD	O	⎍	Horizontal drive pulse	The pulse occurs at the start of lines. When LZ95D42/M is used for timing LSI, connect to HDI of timing LSI.
32	RPI	ICD	–	Horizontal reference input	An input pin for the reference signal to the phase comparator. Set open or to L level when comparator is not used.
33	VINT	ICSU	–	Initialize input	An input pin for initializing circuit. It can be used field-reset input, and the circuit is initialized with the 1/2 dividing pulse of VINT. The frequency of VINT is 60 Hz (NTSC) or 50 Hz (PAL). Set open or to H level when Internal Synchronization mode or no initializing.
34	VD	O	⎍	V drive pulse	The pulse occurs at the start of every field. When LZ95D42/M is used for timing LSI, connect to VDI of timing LSI.
35	FI	O	⎍⎍	Field index	The pulse is used for detecting field. At NTSC mode : ODD field; LOW EVEN field; HIGH At PAL mode : 1st and 3rd field; LOW 2nd and 4th field; HIGH

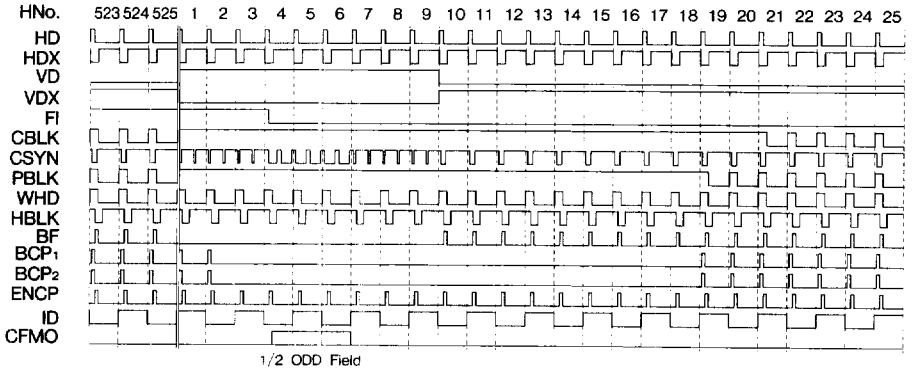
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
36	CPBL	ICD	–	Blanking clamp pulses	When the input is High, BCP_1 (pin 37) and BCP_2 (pin 38) are Low.
37	BCP_1	O	⎍	Optical black clamp pulse 1	A pulse to clamp the optical black signal. This pulse is continuous at Horizontal cycle when CPMD (pin 25) and CPBL (pin 36) are Low.hen CPMD is High and PBL is Low, output stays Low during the absence of effective pixels within the Vertical blanking, otherwise is continuous at Horizontal cycle.
38	BCP_2	O	⎍	Optical black clamp pulse 2	BCP_2 is the same as BCP_1 (pin 37) except that BCP_2 is delayed by 700 ns from BCP_1.
39	PBLK	O	⎍ or ⎎	Pre-blanking pulse	Equivalent to CBLK (pin 16) pulse except for shorter pulse width with cut-off falling edge. When CKCH (pin 22) is L level, the polarity is positive. When CKCH is H level, the polarity is negative.
40	ID	O	⎍	Line index pulse	The pulse is used in color separator. The signal switches between H and L at every line. It resets at the 273th line when in NTSC mode, and at the 326th line when in PAL mode.
41	NC	–	–	No connection	A pin for no use.
42	WBLK	O	⎍ or ⎎	Wide blanking pulse	Equivalent to CBLK (pin 16) except that its pulse width is wider than that of CBLK. When CKCH (pin 22) is L level, the polarity is positive. When CKCH is H level, the polarity is negative.
43	NC	–	–	No connection	A pin for no use.
44	SCOF	ICD	–	Subcarrier control	An input pin for controlling SC_1 (pin 4), SC_2 (pin 5) at NTSC mode. When SCOF is L level, SC_1 and SC_2 are occurred. When SCOF is H level, SC_1 and SC_2 are held at L level.

IC : Input pin (CMOS level).
ICU : Input pin (CMOS level with pull-up resistor).
ICD : Input pin (CMOS level with pull-down resistor).
ICSU : Schmitt-trigger input pin (CMOS level with pull-up resistor).
O : Output pin.
TO : Tri-state output pin.

TIMING DAIGRAM

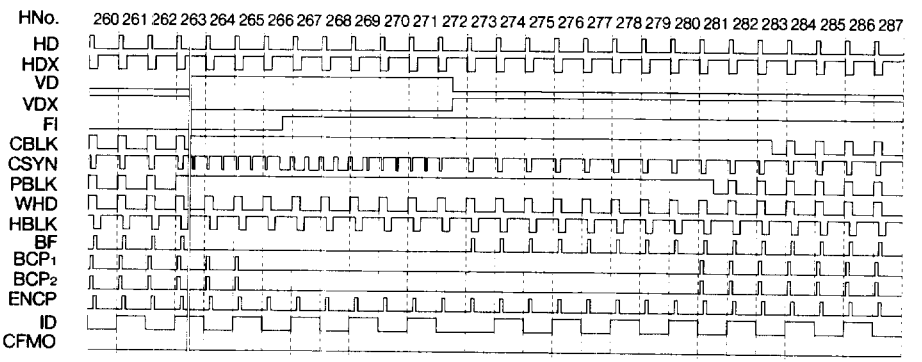
VERTICAL PULSE < NTSC, CKCH = L >

(ODD FIELD)



* CPMD = H, CPBL = L

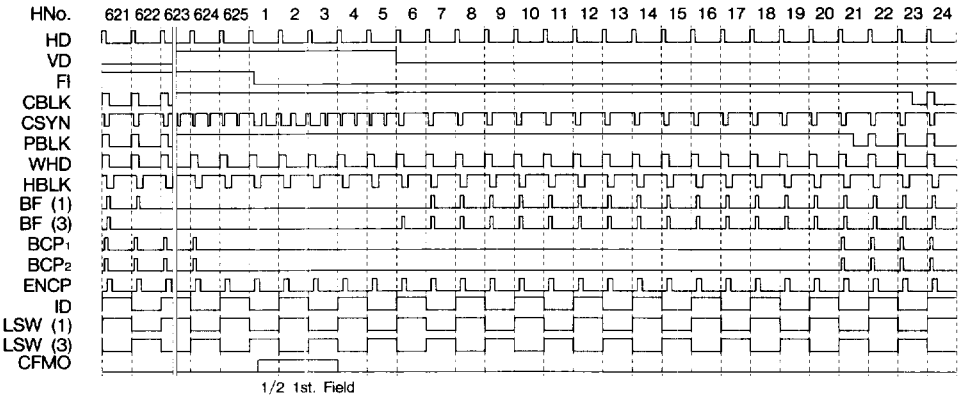
(EVEN FIELD)



* CPMD = H, CPBL = L

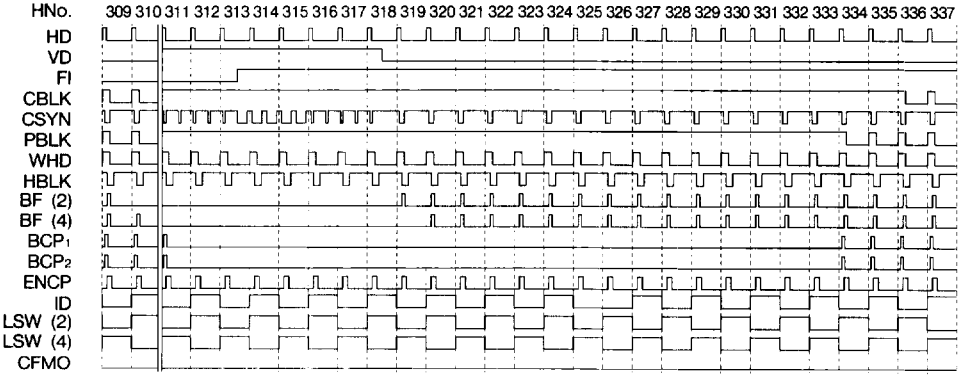
VERTICAL PULSE < PAL, CKCH=L >

(1st, 3rd FIELD)



* CPMD = H, CPBL = L

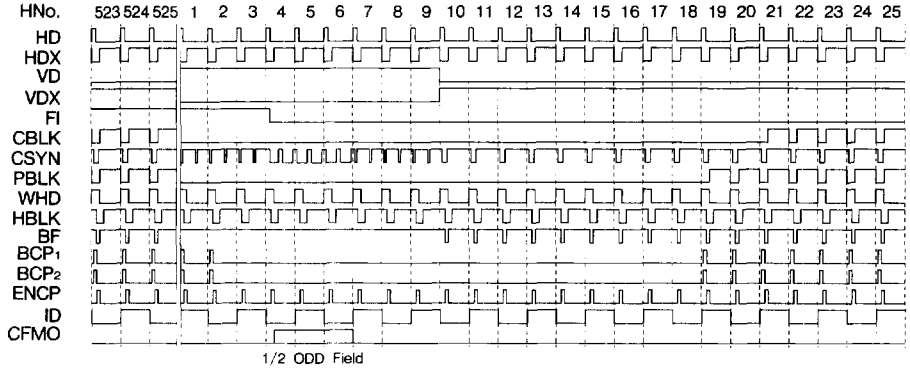
(2nd, 4th FIELD)



* CPMD = H, CPBL = L

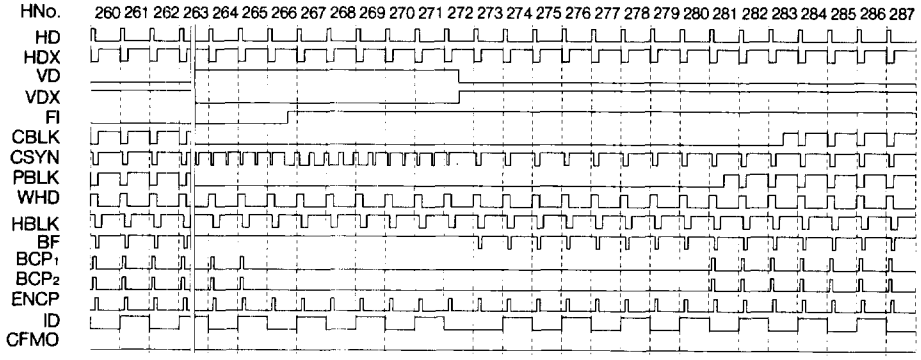
VERTICAL PULSE < NTSC, CKCH=H >

(ODD FIELD)



* CPMD = H, CPBL = L

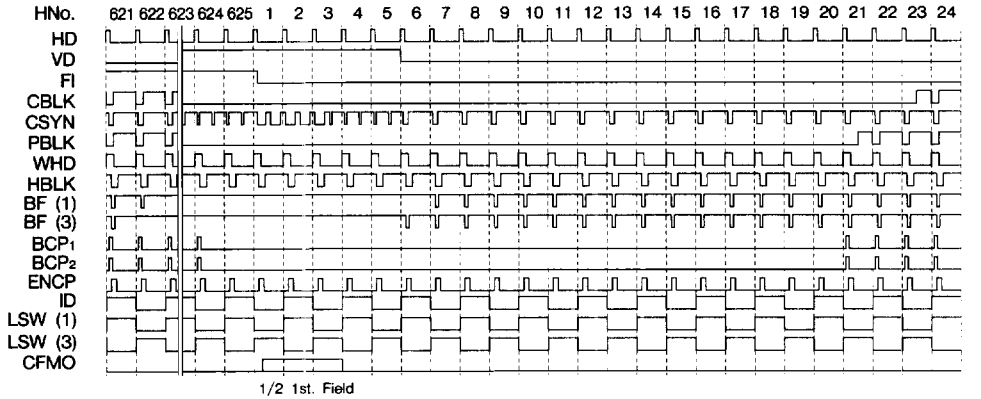
(EVEN FIELD)



* CPMD = H, CPBL = L

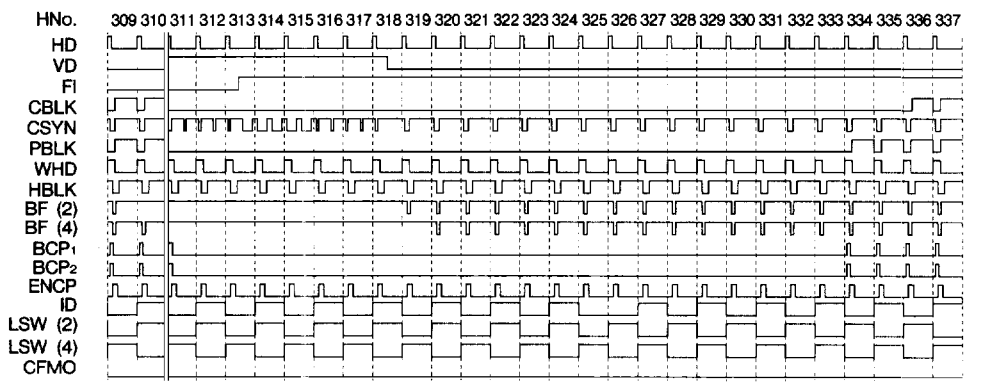
VERTICAL PULSE < PAL, CKCH = H >

(1st, 3rd FIELD)



* CPMD = H, CPBL = L

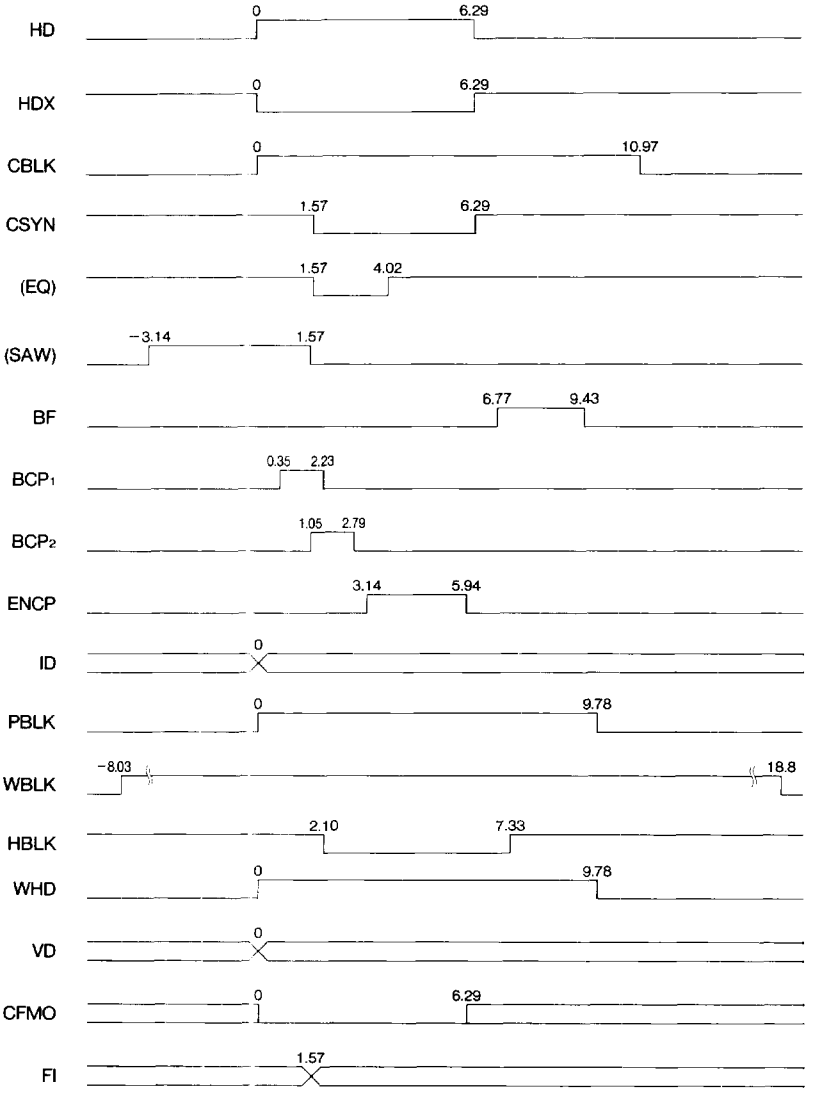
(2nd, 4th FIELD)



* CPMD = H, CPBL = L

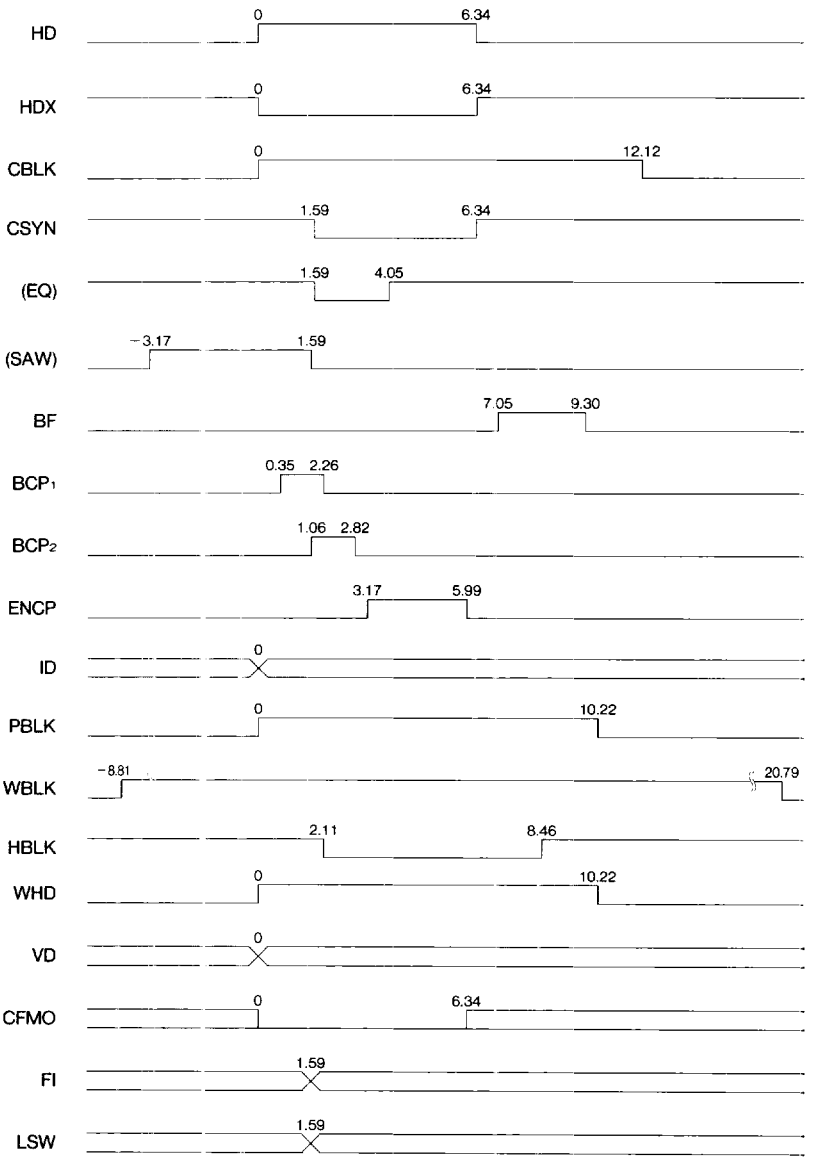
HORIZONTAL PULSE < NTSC, CKCH=L >

Unit : μs



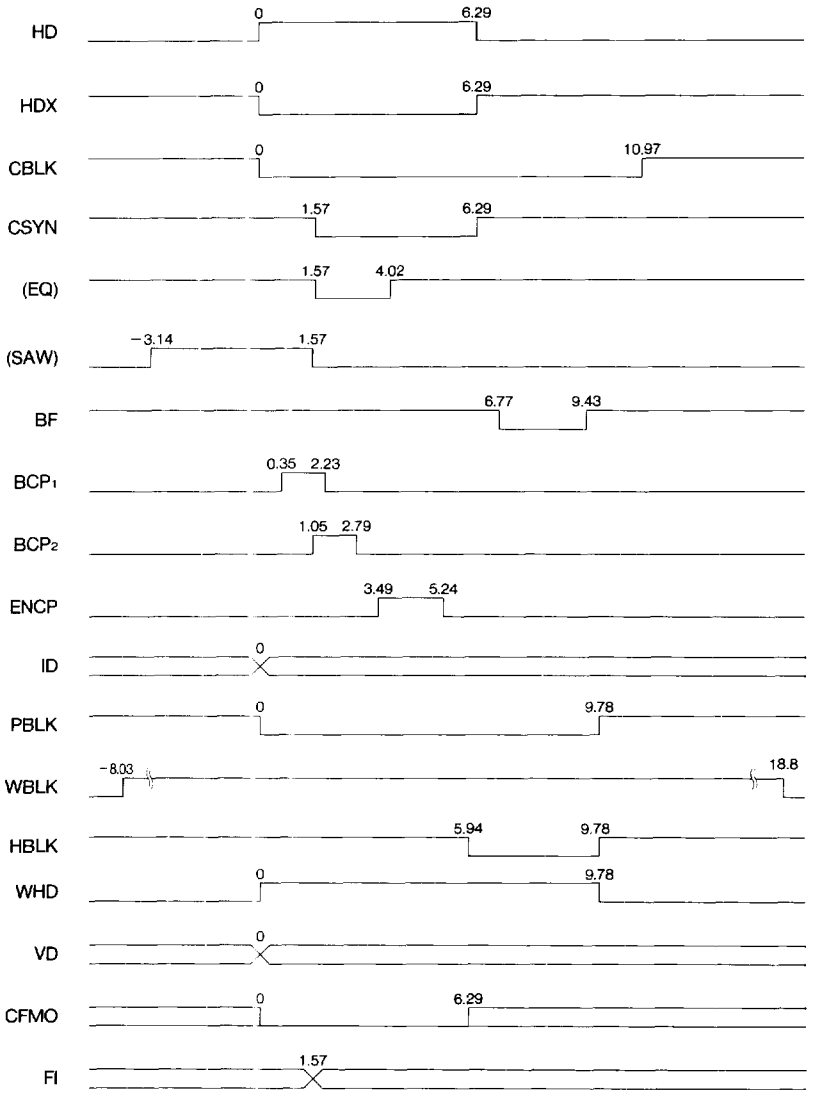
HORIZONTAL PULSE < PAL, CKCH = L >

Unit : μs



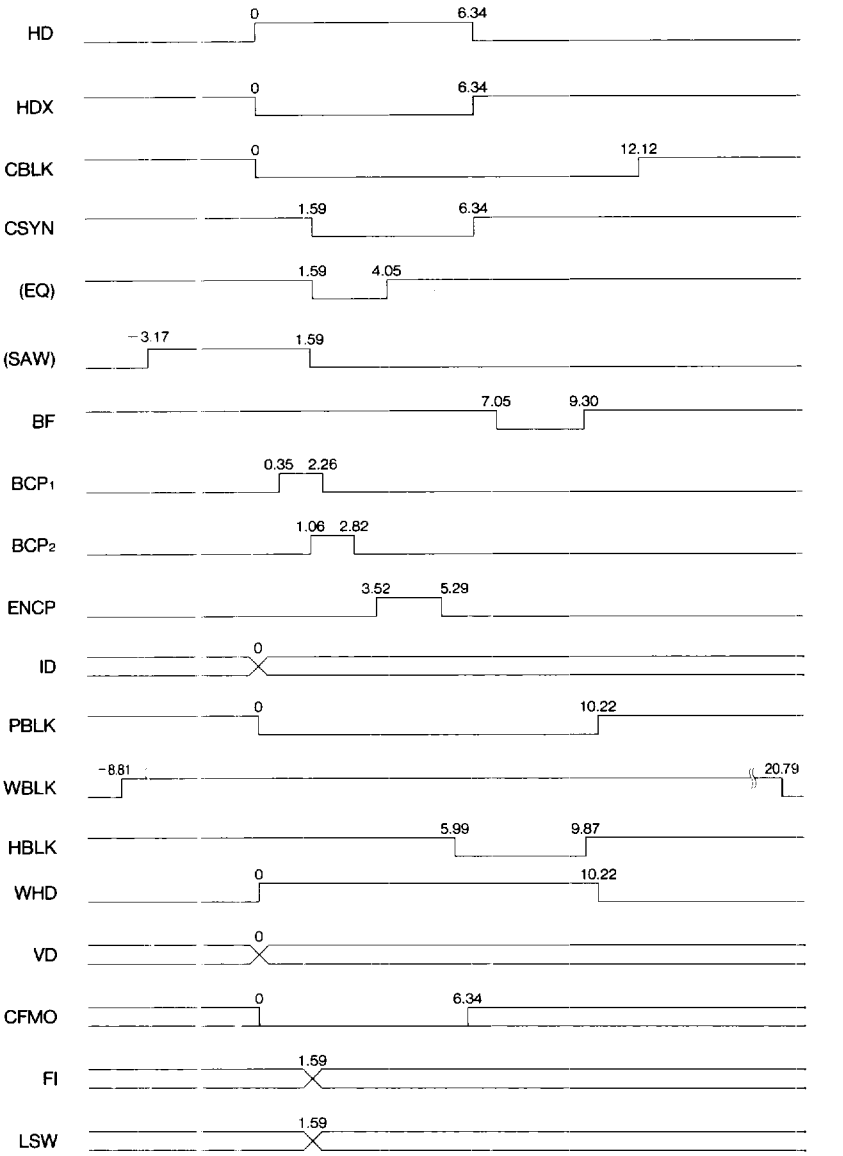
HORIZONTAL PULSE < NTSC, CKCH = H >

Unit : μs



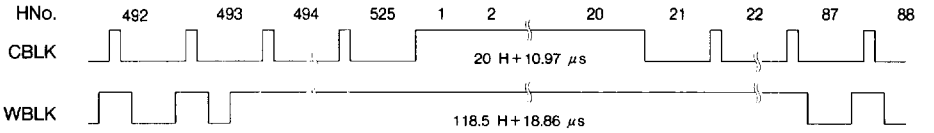
HORIZONTAL PULSE < PAL, CKCH=H >

Unit : μs

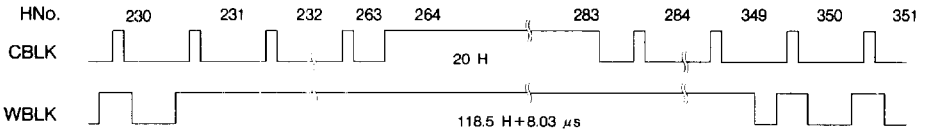


"WBLK" PULSE < CKCH=L >

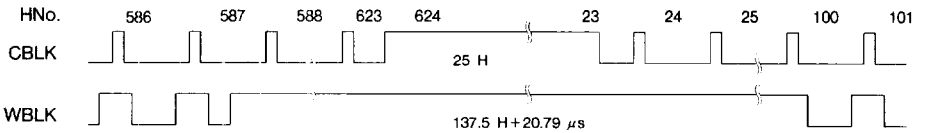
NTSC : (ODD FIELD)



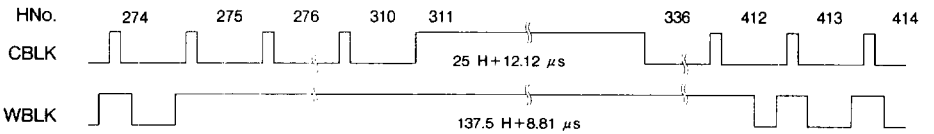
(EVEN FIELD)



PAL : (1st, 3rd FIELD)

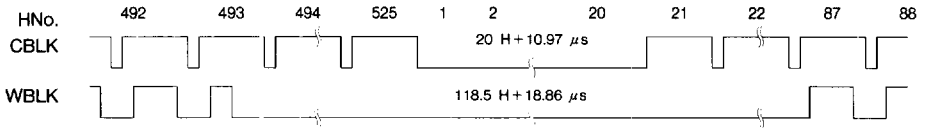


(2nd, 4th FIELD)

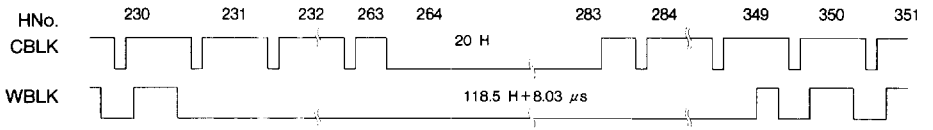


"WBLK" PULSE < CKCH=H >

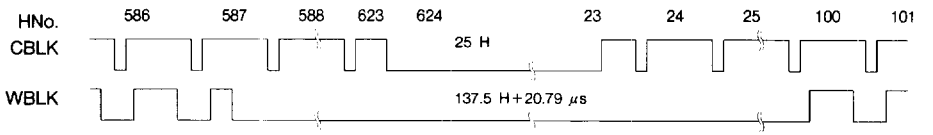
NTSC : (ODD FIELD)



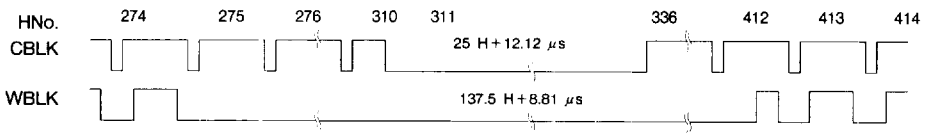
(EVEN FIELD)



PAL : (1st, 3rd FIELD)

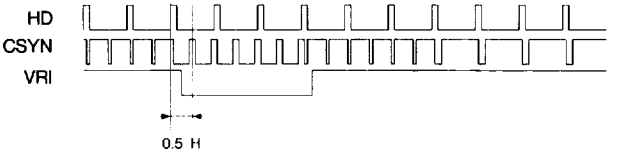


(2nd, 4th FIELD)

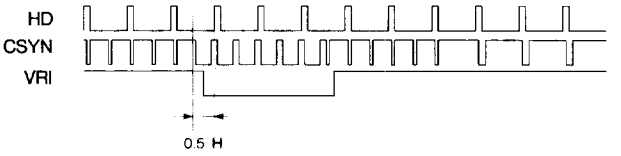


"VRI" INPUT TIMING

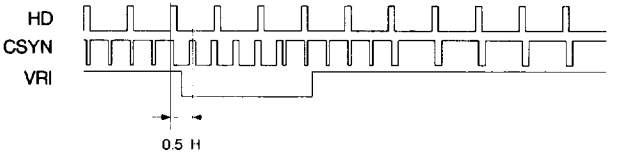
NTSC : (ODD FIELD)



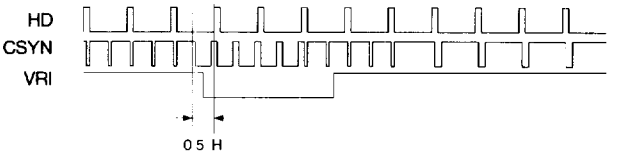
(EVEN FIELD)



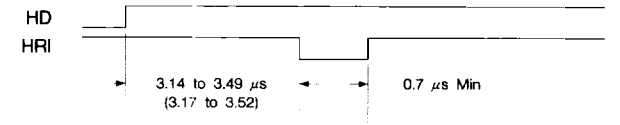
PAL : (1st, 3rd FIELD)



(2nd, 4th FIELD)



"HRI" INPUT TIMING ( ) : PAL



"VINT" INPUT TIMING ( ) : PAL