

MITSUBISHI'S M5M5179AP, J, FP-20, -25, -20L, -25L

73728-BIT (8192-WORD BY 9-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 8192-word by 9-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. 9-bit organization is useful for parity check system. These devices operate on a single 5V supply, and are directly TTL compatible.

FEATURES

- Fast access time M5M5179AP, J, FP-20, -20L ... 20ns(max)
M5M5179AP, J, FP-25, -25L ... 25ns(max)
- Low power dissipation Active 300mW(typ)
Stand-by(-20, -25) 5mW(typ)
Stand-by(-20L, -25L) ... 50μW(typ)
- 9-bit organization
- Single +5V power supply
- Fully static operation: No clocks, no refresh
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by $\overline{S_1}$, S_2
- \overline{OE} prevents data contention in the I/O bus
- Common data I/O

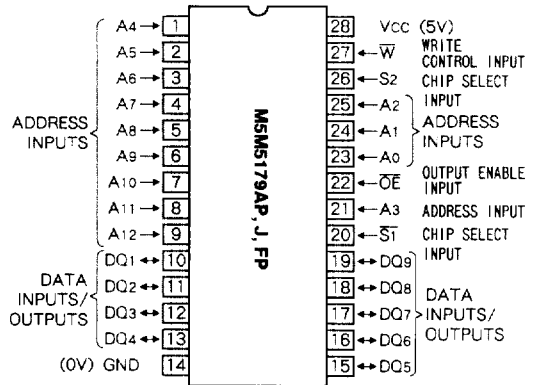
APPLICATION

High-speed memory systems

FUNCTION

The operation mode of the M5M5179A is determined by a combination of the device control inputs $\overline{S_1}$, S_2 , \overline{W} and \overline{OE} . Each mode is summarized in the function table. (see next page)

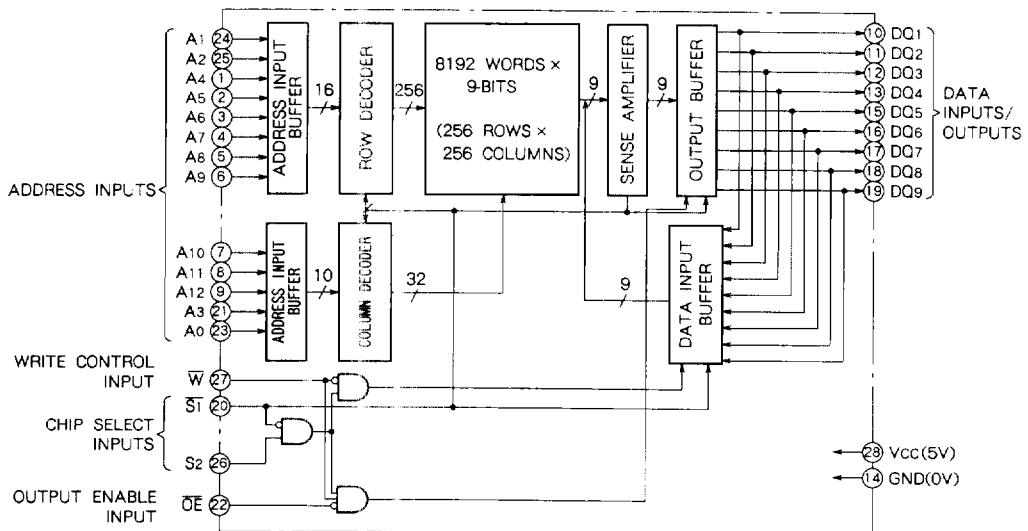
PIN CONFIGURATION (TOP VIEW)



Outline 28P4Y(P)
28P0J(J)
28P2W-C(FP)

A write cycle is executed whenever the low level \overline{W} overlaps with the low level $\overline{S_1}$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

BLOCK DIAGRAM



M5M5179AP, J, FP-20, -25, -20L, -25L

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A read cycle is executed by setting \bar{W} at a high level and \bar{OE} at a low level while \bar{S}_1 and S_2 are in an active state ($\bar{S}_1 = L, S_2 = H$)

When setting \bar{S}_1 at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \bar{S}_1 . The power supply current is reduced as low as the stand-by current which is specified as I_{CC2} or I_{CC3} .

FUNCTION TABLE

\bar{S}_1	S_2	\bar{W}	\bar{OE}	Mode	DQ	I_{CC}
L	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.5 * ~7	V
V	Input voltage		-0.5 * ~ $V_{CC} + 0.3$	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	1000	mW
T_{opr}	Operating temperature		-10~85	$^\circ\text{C}$
T_{stg}	Storage temperature		-65~150	$^\circ\text{C}$

* -3.5V in case of AC (pulse width $\leq 20\text{ns}$), -0.5V in case of DC

DC ELECTRICAL CHARACTERISTICS ($T_a = 0\sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.4		$V_{CC}+0.3$	V
V_{IL}	Low input voltage		-0.5*		0.6	V
V_{OH}	High output voltage	$I_{OH} = -4\text{mA}$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 8\text{mA}$			0.4	V
I	Input current	$V_i = 0\sim V_{CC}$			± 10	μA
I_{OH}	High level output current in off-state	$\bar{S}_1 = V_{IH}$ or $S_2 = V_{IL}$ or $\bar{OE} = V_{IH}$			10	μA
I_{OL}	Low level output current in off-state	$V_{iO} = 0\sim V_{CC}$			-10	μA
I_{CC1}	Active supply current	$\bar{S}_1 = V_{IL}$ Output open Other inputs = V_{IH}	AC(25MHz) DC		120 70	mA
I_{CC2}	Stand by supply current	$S_2 = V_{IL}, \bar{S}_1 = V_{IH}$ Other inputs = $0\sim V_{CC}$	AC(25MHz) DC		30 20	mA
I_{CC3}	Stand by supply current	$\bar{S}_1 \geq V_{CC} - 0.2\text{V}$ Other inputs $\leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V}$	-20, -25 -20L, -25L		2 100	mA μA
C_i	Input capacitance	$\bar{S}_1, S_2, \bar{OE}, \bar{W}$ $A_0\sim A_7$	$V_i = \text{GND}, V_i = 25\text{mVrms}, f = 1\text{MHz}$		7	pF
C_o					Output capacitance	

Note 1. Direction for current flowing into IC is indicated as positive (no mark).

2. C_i, C_o are periodically sampled and are not 100% tested.

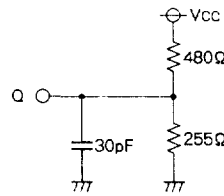
* = -3.0V in case of AC (pulse width $\leq 20\text{ns}$), -0.5V in case of DC

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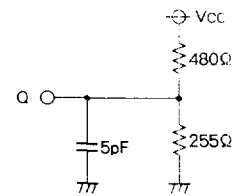
AC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)**(1) MEASUREMENT CONDITIONS**

Input pulse levels $V_{IH} = 3V$, $V_{IL} = 0V$
 Input rise and fall time 3ns
 Input timing standard levels $V_{IH} = V_{IL} = 1.5V$
 Output timing reference levels $V_{OH} = V_{OL} = 1.5V$
 Output loads Fig. 1, Fig. 2



(Including scope and JIG)

Fig. 1 Output load



(Including scope and JIG)

Fig. 2 Output load for t_{en} , t_{dis} **(2) Read cycle**

Symbol	Parameter	Limits				Unit
		M5M5179A-20, -20L		M5M5179A-25, -25L		
		Min	Max	Min	Max	
t_{CR}	Read cycle time					ns
$t_{a(A)}$	Address access time		20		25	ns
$t_{a(S1)}$	Chip select 1 access time		20		25	ns
$t_{a(S2)}$	Chip select 2 access time		15		18	ns
$t_{a(OE)}$	Output enable access time		10		12	ns
$t_{v(A)}$	Data valid time after address change	3		3		ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	3		3		ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		10		15	ns
$t_{en(S2)}$	Output enable time after S_2 high	2		2		ns
$t_{dis(S2)}$	Output disable time after S_2 low		10		15	ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	2		2		ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high		10		15	ns
t_{PU}	Power-up time after chip selection	0		0		ns
t_{PD}	Power-down time after chip selection		20		25	ns

(3) Write cycle

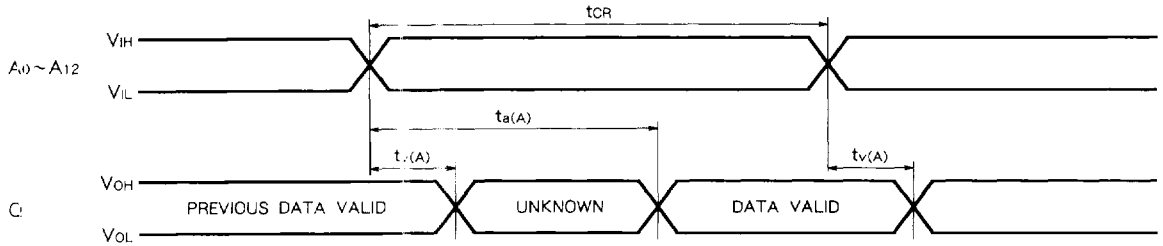
Symbol	Parameter	Limits				Unit
		M5M5179A-20, -20L		M5M5179A-25, -25L		
		Min	Max	Min	Max	
t_{CW}	Write cycle time		20		25	ns
$t_{su(S1)}$	Chip select 1 set up time	16		20		ns
$t_{su(S2)}$	Chip select 2 set up time	12		15		ns
$t_{su(A)1}$	Address set up time 1 (\overline{W} control)	0		0		ns
$t_{su(A)2}$	Address set up time 2 ($\overline{S_1}$ control)	0		0		ns
$t_{su(A)3}$	Address set up time 3 (S_2 control)	0		0		ns
$t_{w(W)}$	Write pulse width	15		18		ns
$t_{rec(W)}$	Write recovery time	3		3		ns
$t_{su(D)}$	Data set up time	10		12		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{dis(W)}$	Output disable time after \overline{W} low		10		12	ns
$t_{en(W)}$	Output enable time after \overline{W} high	0		0		ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high		10		15	ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	2		2		ns
$t_{su(A-\overline{WH})}$	Address to \overline{W} high	15		18		ns

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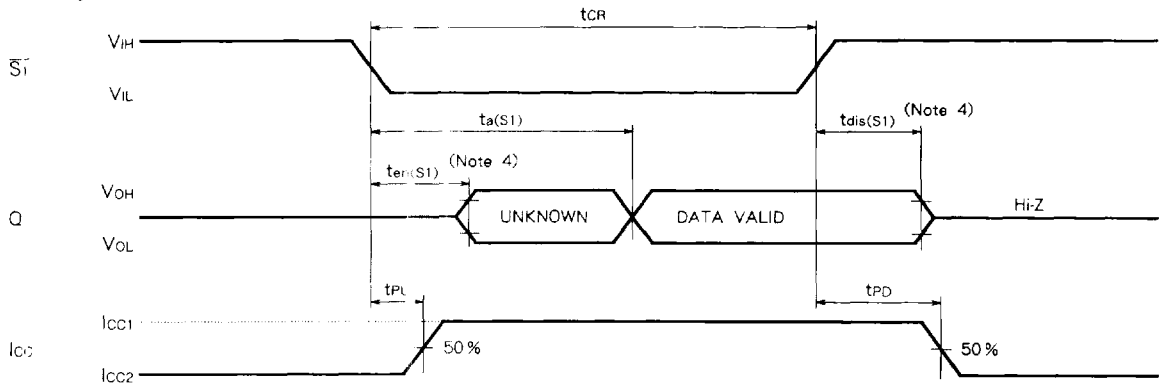
(4) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



S₂ = \bar{W} = H
S₁ = \bar{OE} = L

Read cycle 2 (Note 3)

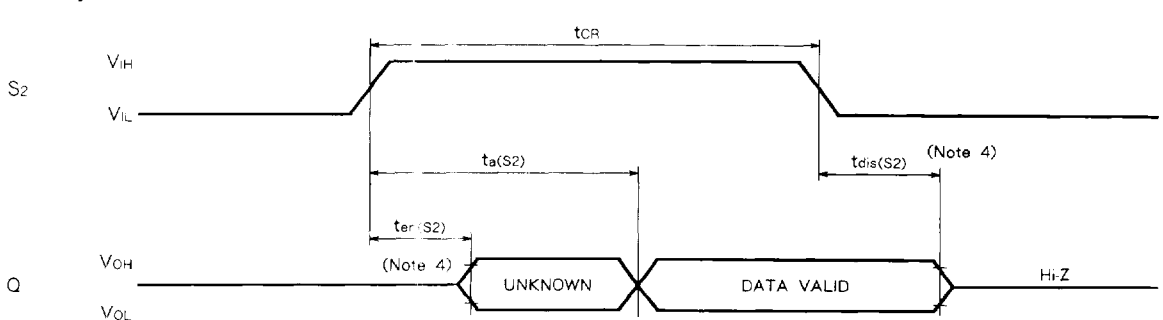


S₂ = \bar{W} = H
 \bar{OE} = L

Note 3. Addresses valid prior to or coincident with $\bar{S1}$ transition low.

4. Transition is measured ± 500 mV from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 5)



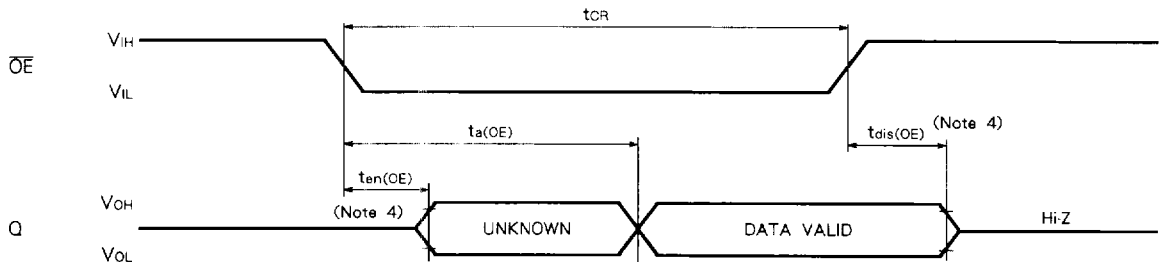
\bar{W} = H
S₁ = \bar{OE} = L

Note 5. Addresses and $\bar{S1}$ valid prior to S₂ transition high by [t_{a(A)} - t_{a(S2)}, t_{a(S1)} - t_{a(S2)}].

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Read cycle 4 (Note 6)

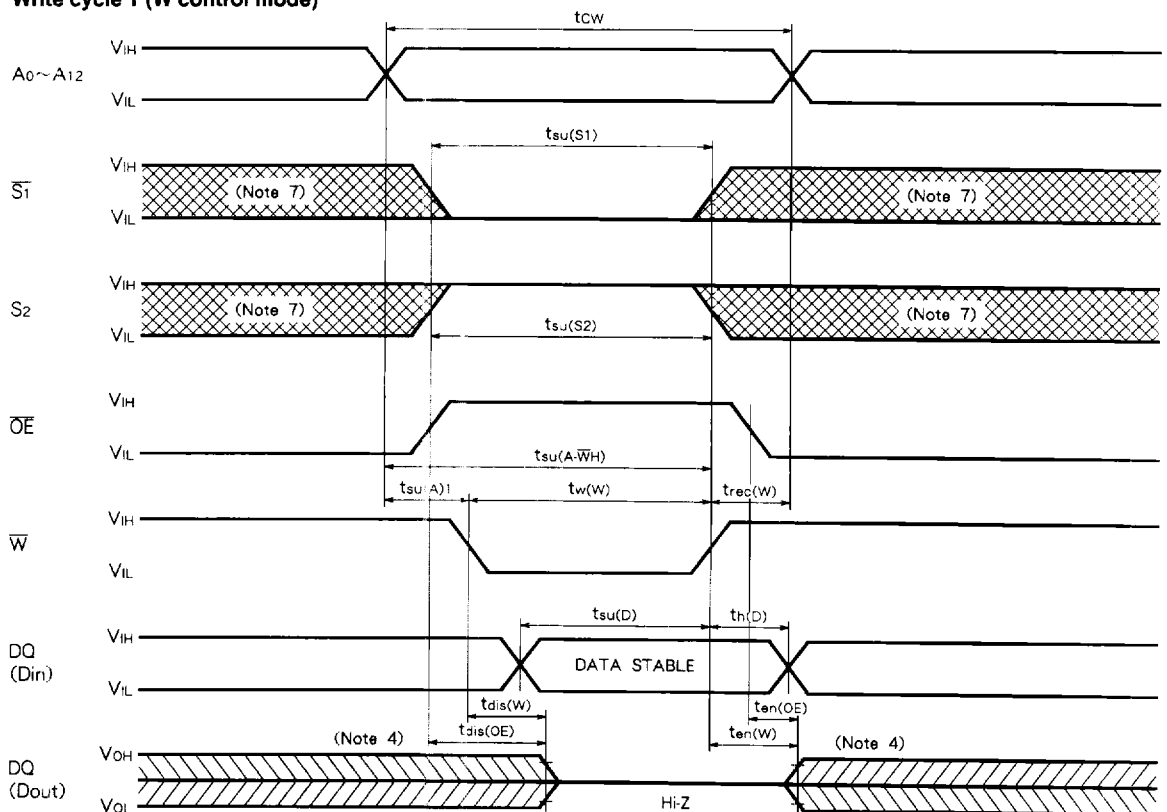


$$\begin{aligned} S_2 &= \bar{W} = H \\ \bar{S}_1 &= _ \end{aligned}$$

Note 6. Addresses and \bar{S}_1 valid prior to \bar{OE} transition low by $[t_{a(A)} - t_{a(OE)}, t_{a(S1)} - t_{a(OE)}]$.

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 (\bar{W} control mode)

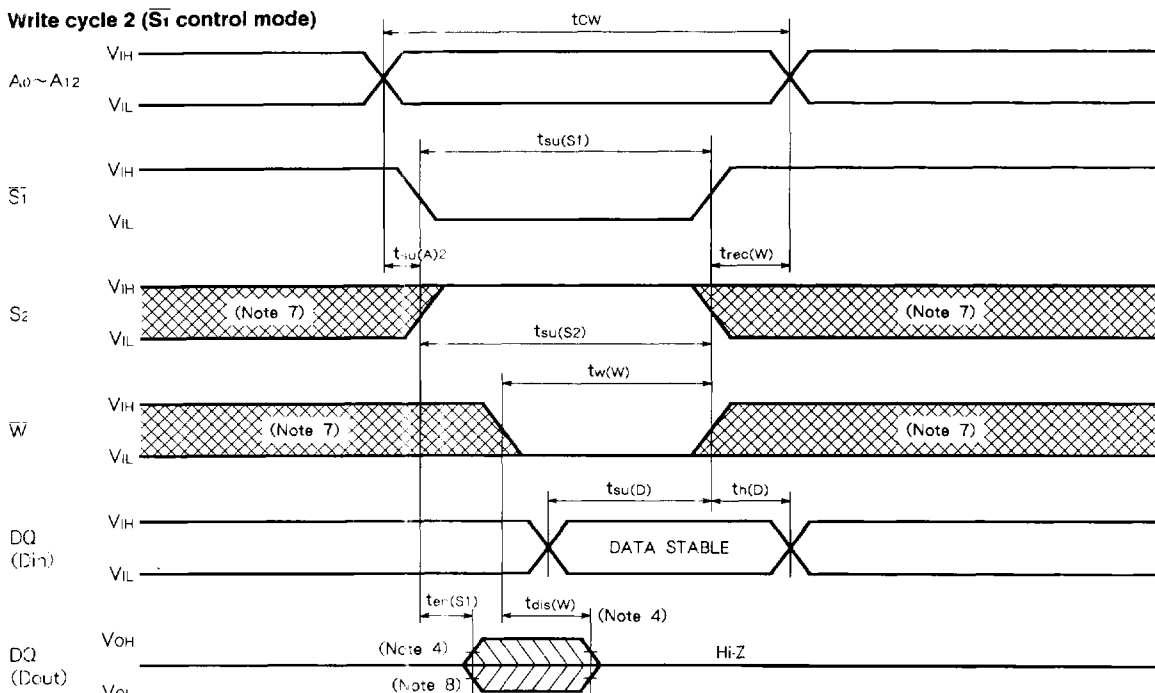


Note 7. Hatching indicates the state is don't care.

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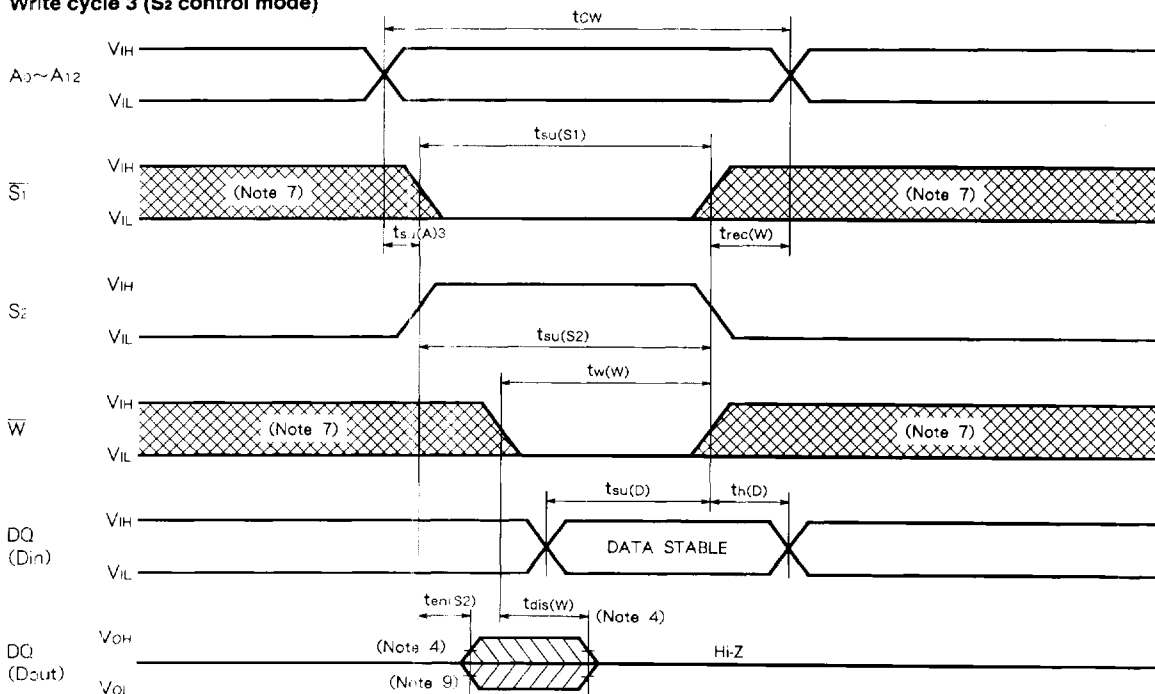
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Write cycle 2 ($\overline{S1}$ control mode)



Note 8. When the falling edge of \overline{W} is simultaneous or prior to the falling edge of $\overline{S1}$, the output is maintained in the high impedance.

Write cycle 3 (S_2 control mode)



Note 9. When the falling edge of \overline{W} is simultaneous or prior to the rising edge of S_2 , the output is maintained in the high impedance.

10. t_{en} , t_{dis} are periodically sampled and are not 100% tested.

M5M5179AP, J, FP-20, -25, -20L, -25L**73728-BIT (8192-WORD BY 9-BIT) CMOS STATIC RAM****POWER DOWN CHARACTERISTICS** ($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{cc(PD)}$	Power down supply voltage		2			V
$V_i(ST)$	Chip select input voltage	$V_i(ST) \geq V_{cc} - 0.2V$	$V_{cc} - 0.2$			V
$t_{su(PD)}$	Power down setup time	$V_i \geq V_{cc} - 0.2V$ or $0V \leq V_i \leq 0.2V$	0			ns
$t_{rec(PD)}$	Power down recovery time		-20L	20		ns
			-25L	25		
$I_{cc(PD)}$	Power down supply current	$V_{cc} = 3.0V$			50	μA
		$V_{cc} = 5.5V$			100	

Note 11. This is only M5M5179AP, J, FP-20L, -25L

TIMING WAVEFORM FOR POWER DOWN