



MACRONIX
INTERNATIONAL Co., LTD.

MX25L6436E
MX25L12836E

MX25L6436E/MX25L12836E
HIGH PERFORMANCE
SERIAL FLASH SPECIFICATION

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64/128M-BIT [x 1/x 2/x 4] CMOS MXSMIO™ (SERIAL MULTI I/O) FLASH MEMORY**FEATURES****GENERAL**

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 64Mb: 67,108,864 x 1 bit structure or 33,554,432 x 2 bits (two I/O mode) structure or 16,777,216 x 4 bits (four I/O mode) structure
128Mb: 134,217,728 x 1 bit structure or 67,108,864 x 2 bits (two I/O mode) structure or 33,554,432 x 4 bits (four I/O mode) structure
- 4096 Equal Sectors with 4K bytes each
 - Any Sector can be erased individually
- 512 Equal Blocks with 32K bytes each
 - Any Block can be erased individually
- 256 Equal Blocks with 64K bytes each
 - Any Block can be erased individually
- Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
VCC = 2.7~3.6V
 - Normal read
 - 50MHz
 - Fast read (Normal Serial Mode)
 - 1 I/O: 104MHz with 8 dummy cycles
 - 2 I/O: 70MHz with 4 dummy cycles
 - 4 I/O: 70MHz with 6 dummy cycles
 - Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
 - Byte program time: 9us (typical)
 - Continuously Program mode (automatically increase address under word program mode)
 - Fast erase time: 60ms (typ.)/sector (4K-byte per sector) ; 0.7s(typ.) /block (64K-byte per block); 50s(typ.) /chip for 64Mb, 80s(typ.) /chip for 128Mb
- Low Power Consumption
 - Low active read current: 45mA(max.) at 104MHz, 40mA(max.) at 66MHz and 30mA(max.) at 33MHz
 - Low active programming current: 25mA (max.)
 - Low active erase current: 25mA (max.)
 - Low standby current: 100uA (max.)
 - Deep power down current: 128Mb is 40uA (max.), 64Mb is 30uA (max.)
- Typical 100,000 erase/program cycles

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features

- BP0-BP3 block group protect
- Flexible individual block protect when OTP WPSEL=1
- Additional 4K bits secured OTP for unique identifier
- Auto Erase and Auto Program Algorithms
 - Automatically erases and verifies data at selected sector
 - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programmed should have page in the erased state first.)
- Status Register Feature
- Electronic Identification
 - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
 - RES command for 1-byte Device ID
 - Both REMS, REMS2 and REMS4 commands for 1-byte Manufacturer ID and 1-byte Device ID
- Support Common Flash Interface (CFI) (TBD)

HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI/SO0
 - Serial Data Input or Serial Data Multiple Output for 2 x I/O mode and 4 x I/O mode
- SO/SO1/PO7
 - Serial Data Output or Serial Data Multiple Output for 2 x I/O mode and 4 x I/O mode or Parallel Data
- WP#/SO2
 - Hardware write protection or serial data Multiple Output for 4 x I/O mode
- NC/SO3
 - NC pin or serial data Multiple Output for 4 x I/O mode
- PO0~PO6
 - For parallel mode data (only 128Mb provide parallel mode)
- PACKAGE
 - 16-pin SOP (300mil) only for MX25L12836E
 - 8-pin SOP (200mil) only for MX25L6436E
 - **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

MX25L6436E is 67,108,864 bits serial Flash memory, which is configured as 8,388,608 x 8 internally. When it is in two or four I/O mode, the structure becomes 33,554,432 bits x 2 or 16,777,216 bits x 4. MX25L12836E is 134,217,728 bits serial Flash memory, which is configured as 16,777,216 x 8 internally. When it is in two or four I/O mode, the structure becomes 67,108,864 bits x 2 or 33,554,432 bits x 4. The MX25L6436E/12836E features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L6436E/12836E provides high performance read mode, which may latch address and data on both rising and falling edge of clock. By using this high performance read mode, the data throughput may be doubling. Moreover, the performance may reach direct code execution, the RAM size of the system may be reduced and further saving system cost.

MX25L6436E/12836E, MXSMIO™ (Serial Multi I/O) flash memory, provides sequential read operation on whole chip and multi-I/O features.

When it is in dual I/O mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in quad I/O mode, the SI pin, SO pin, WP# pin and NC pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output. Parallel mode is also provided in this device. It features 8 bit input/output for increasing throughputs. This feature is recommended to be used for factory production purpose.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for Continuously Program mode, and erase command is executes on sector (4K-byte), block (32K-byte/64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 100uA DC current.

The MX25L6436E/12836E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Additional Features

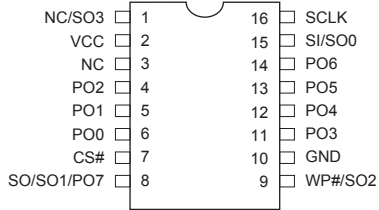
Additional Features Part Name	Protection and Security		Read Performance			
	Flexible or Individual block (or sector) protection	4K-bit secured OTP	1 I/O Read (104 MHz)	Dual Read (70 MHz)	Quad Read (70 MHz)	8 I/O Parallel Mode (6 MHz)
MX25L6436E MX25L12836E	V	V	V	V	V	V (Note 1)

Additional Features Part Name	Identifier				
	RES (command: AB hex)	REMS (command: 90 hex)	REMS2 (command: EF hex)	REMS4 (command: DF hex)	RDID (command: 9F hex)
MX25L6436E	16 (hex)	C2 16 (hex)	C2 16 (hex)	C2 16 (hex)	C2 20 17 (hex)
MX25L12836E	17 (hex)	C2 17 (hex)	C2 17 (hex)	C2 17 (hex)	C2 20 18 (hex)

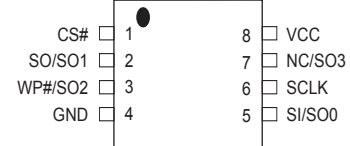
Note 1: Only MX25L12836E provide parallel mode.

PIN CONFIGURATION

16-PIN SOP (300mil) for MX25L12836E

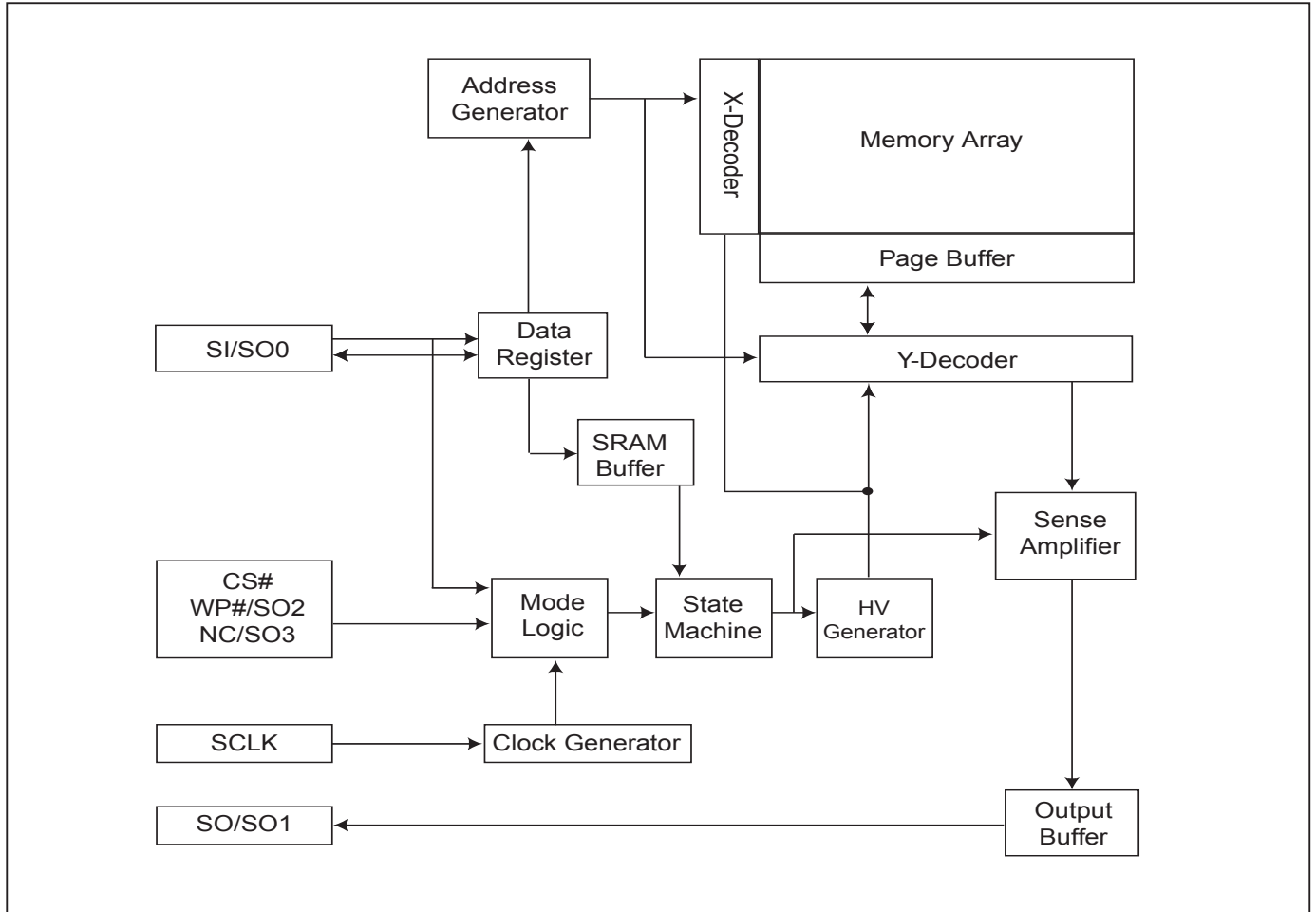


8-PIN SOP (200mil) for MX25L6436E



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SO0	Serial Data Input / Serial Data Multiple Output (for 2xI/O or 4xI/O mode)
SO/SO1/ PO7	Serial Data Output (for 1xI/O)/Serial Data Multiple Output (for 2xI/O or 4xI/O mode) / Parallel Data Output/Input
SCLK	Clock Input
WP#/SO2	Write protection: connect to GND or Serial Data Multiple Output (for 4xI/O mode)
NC/SO3	NC pin (Not connect) or Serial Data Multiple Output (for 4xI/O mode)
VCC	+ 3.3V Power Supply
GND	Ground
PO0~PO6	Parallel data output/input (PO0~PO6 can be connected to NC in Serial Mode), NC on MX25L6436E
NC	No Connection

BLOCK DIAGRAM

DATA PROTECTION

MX25L6436E/12836E is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the standby mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
 - Power-up
 - Write Disable (WRDI) command completion
 - Write Status Register (WRSR) command completion
 - Page Program (PP, 4PP) command completion
 - Continuously Program mode (CP) instruction completion
 - Sector Erase (SE) command completion
 - Block Erase (BE, BE32K) command completion
 - Chip Erase (CE) command completion
 - Single Block Lock/Unlock (SBLK/SBULK) instruction completion
 - Gang Block Lock/Unlock (GBLK/GBULK) instruction completion
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

I. Block lock protection

- The Software Protected Mode (SPM) uses (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits. Please refer to table of "Protected Area Sizes".
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O mode, the feature of HPM will be disabled.
- MX25L6436E/12836E provide individual block (or sector) write protect & unprotect. User may enter the mode with WPSEL command and conduct individual block (or sector) write protect with SBLK instruction, or SBULK for individual block (or sector) unprotect. Under the mode, user may conduct whole chip (all blocks) protect with GBLK instruction and unlock the whole chip with GBULK instruction.

Table 2. Protected Area Sizes

Status bit				Protection Area	
BP3	BP2	BP1	BP0	64Mb	128Mb
0	0	0	0	0 (none)	0 (none)
0	0	0	1	1 (2 blocks, block 126th-127th)	1 (2 blocks, block 254th-255th)
0	0	1	0	2 (4 blocks, block 124th-127th)	2 (4 blocks, block 252nd-255th)
0	0	1	1	3 (8 blocks, block 120th-127th)	3 (8 blocks, block 248th-255th)
0	1	0	0	4 (16 blocks, block 112nd-127th)	4 (16 blocks, block 240th-255th)
0	1	0	1	5 (32 blocks, block 96th-127th)	5 (32 blocks, block 224th-255th)
0	1	1	0	6 (64 blocks, block 64th-127th)	6 (64 blocks, block 192nd-255th)
0	1	1	1	7 (128 blocks, all)	7 (128 blocks, block 128th-255th)
1	0	0	0	8 (128 blocks, all)	8 (256 blocks, all)
1	0	0	1	9 (128 blocks, all)	9 (256 blocks, all)
1	0	1	0	10 (128 blocks, all)	10 (256 blocks, all)
1	0	1	1	11 (128 blocks, all)	11 (256 blocks, all)
1	1	0	0	12 (128 blocks, all)	12 (256 blocks, all)
1	1	0	1	13 (128 blocks, all)	13 (256 blocks, all)
1	1	1	0	14 (128 blocks, all)	14 (256 blocks, all)
1	1	1	1	15 (128 blocks, all)	15 (256 blocks, all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker. Please refer to Table 3. 4K-bit Secured OTP Definition.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR (write security register) command to set customer lock-down bit1 as "1". Please refer to table of "Security Register Definition" for security register bit definition and table of "4K-bit Secured OTP Definition" for address range definition.
- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxxFFF	3968-bit	N/A	

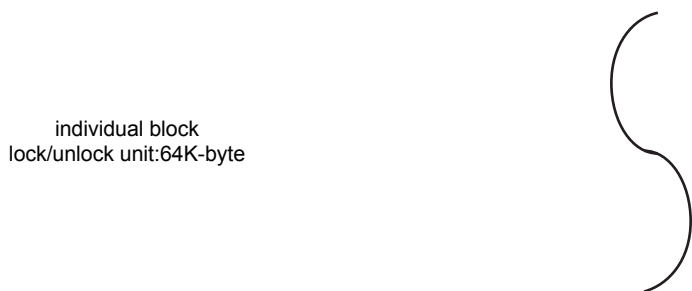
Memory Organization

Table 4-1. Memory Organization for MX25L6436E

Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range	
127	255	2047	7FF000h	7FFFFFFh
		⋮		
		2040	7F8000h	7F8FFFFh
		2039	7F7000h	7F7FFFFh
	254	⋮		
		2032	7F0000h	7F0FFFFh
		2031	7EF000h	7EFFFFFFh
		⋮		
126	253	2024	7E8000h	7E8FFFFh
		⋮		
		2023	7E7000h	7E7FFFFh
		⋮		
	252	2016	7E0000h	7E0FFFFh
		⋮		
		2015	7DF000h	7DFFFFFFh
		⋮		
125	251	2008	7D8000h	7D8FFFFh
		⋮		
		2007	7D7000h	7D7FFFFh
		⋮		
	250	2000	7D0000h	7D0FFFFh
		⋮		
		⋮		
		⋮		

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte



2	5	47	02F000h	02FFFFFFh
		⋮		
		40	028000h	028FFFFh
	4	39	027000h	027FFFFh
		⋮		
1	3	32	020000h	020FFFFh
		⋮		
		31	01F000h	01FFFFFFh
	2	24	018000h	018FFFFh
		⋮		
		23	017000h	017FFFFh
		⋮		
0	1	16	010000h	010FFFFh
		⋮		
		15	00F000h	00FFFFFFh
	0	8	008000h	008FFFFh
		7	007000h	007FFFFh
⋮				
0	0	000000h	000FFFFh	

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

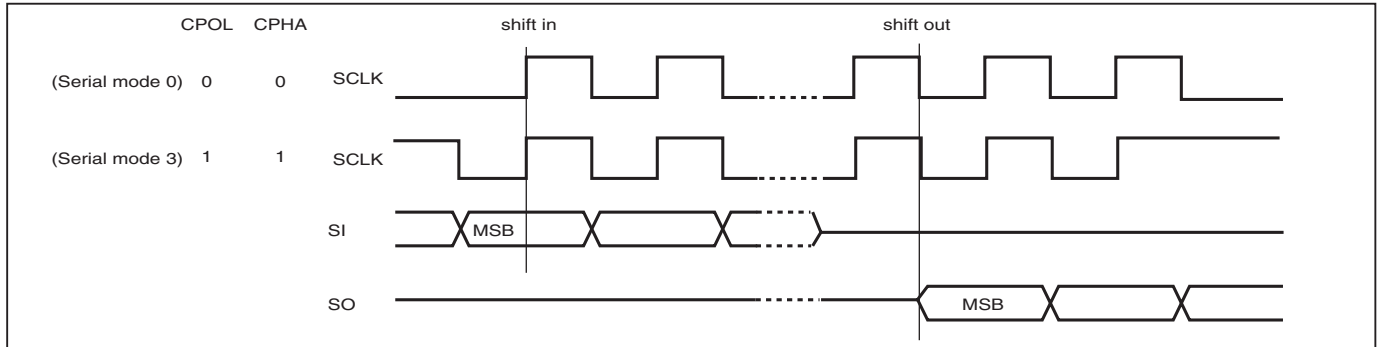
Table 4-2. Memory Organization for MX25L12836E

Block(64K-byte)	Block(32K-byte)	Sector	Address Range			
255	511	4095	FFF000h	FFFFFFh	individual 16 sectors lock/unlock unit:4K-byte	
		⋮				
		4088	FF8000h	FF8FFFh		
	510	4087	FF7000h	FF7FFFh		
		⋮				
		4080	FF0000h	FF0FFFh		
254	509	4079	FEF000h	FEFFFFh	individual block lock/unlock unit:64K-byte	
		⋮				
		4072	FE8000h	FE8FFFh		
	508	4071	FE7000h	FE7FFFh		
		⋮				
		4064	FE0000h	FE0FFFh		
253	507	4063	FDF000h	FDFFFFh		individual block lock/unlock unit:64K-byte
		⋮				
		4056	FD8000h	FD8FFFh		
	506	4055	FD7000h	FD7FFFh		
		⋮				
		4048	FD0000h	FD0FFFh		
2	5	47	02F000h	02FFFFh	individual block lock/unlock unit:64K-byte	
		⋮				
		40	028000h	028FFFh		
	4	39	027000h	027FFFh		
		⋮				
		32	020000h	020FFFh		
1	3	31	01F000h	01FFFFh		individual 16 sectors lock/unlock unit:4K-byte
		⋮				
		24	018000h	018FFFh		
	2	23	017000h	017FFFh		
		⋮				
		16	010000h	010FFFh		
0	1	15	00F000h	00FFFFh	individual 16 sectors lock/unlock unit:4K-byte	
		⋮				
		8	008000h	008FFFh		
	0	7	007000h	007FFFh		
		⋮				
		0	000000h	000FFFh		

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.
4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as Figure 1-1.
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, DREAD, QREAD, RDBLOCK, RES, REMS, REMS2, REMS4 and RDCFI the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, CE, PP, CP, 4PP, RDP, DP, WPSEL, SBLK, SBULK, GBLK, GBULK, ENSO, EXSO, WRSCUR, ENPLM, EXPLM, ESRY, DSRV and CLSR the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported (for Normal Serial mode)



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

COMMAND DESCRIPTION

Table 5. Command Sets

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)	DREAD (11 20 read)
Command (hex)	06	04	9F	05	01	03	0B	3B
Input Cycles					Data(8)	ADD(24)	ADD(24)	ADD(24)
Dummy Cycles							8	8
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	to write new values to the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by Dual output until CS# goes high

COMMAND (byte)	QREAD (11 40 read)	4PP (quad page program)	SE (sector erase)	BE (block erase 64KB)	BE 32K (block erase 32KB)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)
Command (hex)	6B	38	20	D8	52	60 or C7	02	AD
Input Cycles	ADD(24)	ADD(6)+ Data(512)	ADD(24)	ADD(24)	ADD(24)		ADD(24)+ Data(2048)	ADD(24)+ Data(16)
Dummy Cycles	8							
Action	n bytes read out by Quad output until CS# goes high	quad input to program the selected page	to erase the selected sector	to erase the selected 64KB block	to erase the selected 32KB block	to erase whole chip	to program the selected page	continuously program whole chip, the address is automatically increase

COMMAND (byte)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Command (hex)	B9	AB	AB	90	EF	DF	B1	C1
Input Cycles				ADD(24)	ADD(24)	ADD(24)		
Dummy Cycles			24					
Action	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & device ID	to enter the 4K-bit Secured OTP mode	to exit the 4K-bit Secured OTP mode

COMMAND (byte)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/ BY#)	DSRY (disable SO to output RY/ BY#)	ENPLM (Enter Parallel Mode)	EXPLM (EXIT Parallel Mode)	CLSR (Clear SR Fail Flags)	WPSEL (write protection selection)
Command (hex)	2B	2F	70	80	55	45	30	68
Input Cycles								
Dummy Cycles								
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/ BY# during CP mode	to disable SO to output RY/ BY# during CP mode	8xI/O parallel programming mode	to exit 8xI/O parallel programming mode	clear security register bit 6 and bit 5	to enter and enable individual block protect mode

COMMAND (byte)	SBLK (single block lock) *Note 2	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)	GBULK (gang block unlock)	RDCFI (Read CFI)
Command (hex)	36	39	3C	7E	98	5A
Input Cycles	ADD(24)	ADD(24)	ADD(24)			ADD(24)
Dummy Cycles						8
Action	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect	Read CFI mode

Note 1: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 2: In individual block write protection mode, all blocks/sectors is locked as default.

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, CP, SE, BE, BE32K, CE, WRSR, SBLK, SBULK, GBLK and GBULK, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high. (Please refer to Figure 8)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high. (Please refer to Figure 9)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP, 4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE, BE32K) instruction completion
- Chip Erase (CE) instruction completion
- Continuously Program mode (CP) instruction completion
- Single Block Lock/Unlock (SBLK/SBULK) instruction completion
- Gang Block Lock/Unlock (GBLK/GBULK) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte Device ID, and the individual Device ID of second-byte ID are listed as table of "ID Definitions". (Please refer to Table 6)

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (Please refer to Figure 10)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO (Please refer to Figure 11).

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in Table 2) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP# is enable. While QE is "1", it performs Quad I/O mode and WP# is disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0". SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1= Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the Table 2 "Protected Area Size" in page 11.

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in Table 2). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high. (Please refer to Figure 12)

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 2.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

If the system goes into four I/O mode, the feature of HPM will be disabled.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency f_R . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low → sending READ instruction code → 3-byte address on SI → data out on SO → to end READ operation can use CS# to high at any time during data out. (Please refer to Figure 13)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency f_C . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low → sending FAST_READ instruction code → 3-byte address on SI → 1-dummy byte (default) address on SI → data out on SO → to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to Figure 14)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency f_T . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out (Please refer to Figure 15 for Dual Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(9) Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency f_Q . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction,

the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low → sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO3, SO2, SO1 & SO0 → to end QREAD operation can use CS# to high at any time during data out (Please refer to Figure 16 for Quad Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(10) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Table 4-1 & 4-2) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code → 3-byte address on SI → CS# goes high. (Please refer to Figure 17)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(11) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Table 4-1 & 4-2) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte address on SI → CS# goes high. (Please refer to Figure 18)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(12) Block Erase (BE32K)

The Block Erase (BE32) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32). Any address of the block (Table 4-1 & 4-2) is a valid address for Block Erase (BE32) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte

been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32 instruction is: CS# goes low → sending BE32 instruction code → 3-byte address on SI → CS# goes high. (Please refer to Figure 18)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(13) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low → sending CE instruction code → CS# goes high. (Please refer to Figure 19)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected the Chip Erase (CE) instruction will not be executed, but WEL will be reset.

(14) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low → sending PP instruction code → 3-byte address on SI → at least 1-byte on data on SI → CS# goes high. (Please refer to Figure 20)

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise, the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

(15) 4 x I/O Page Program (4PP)

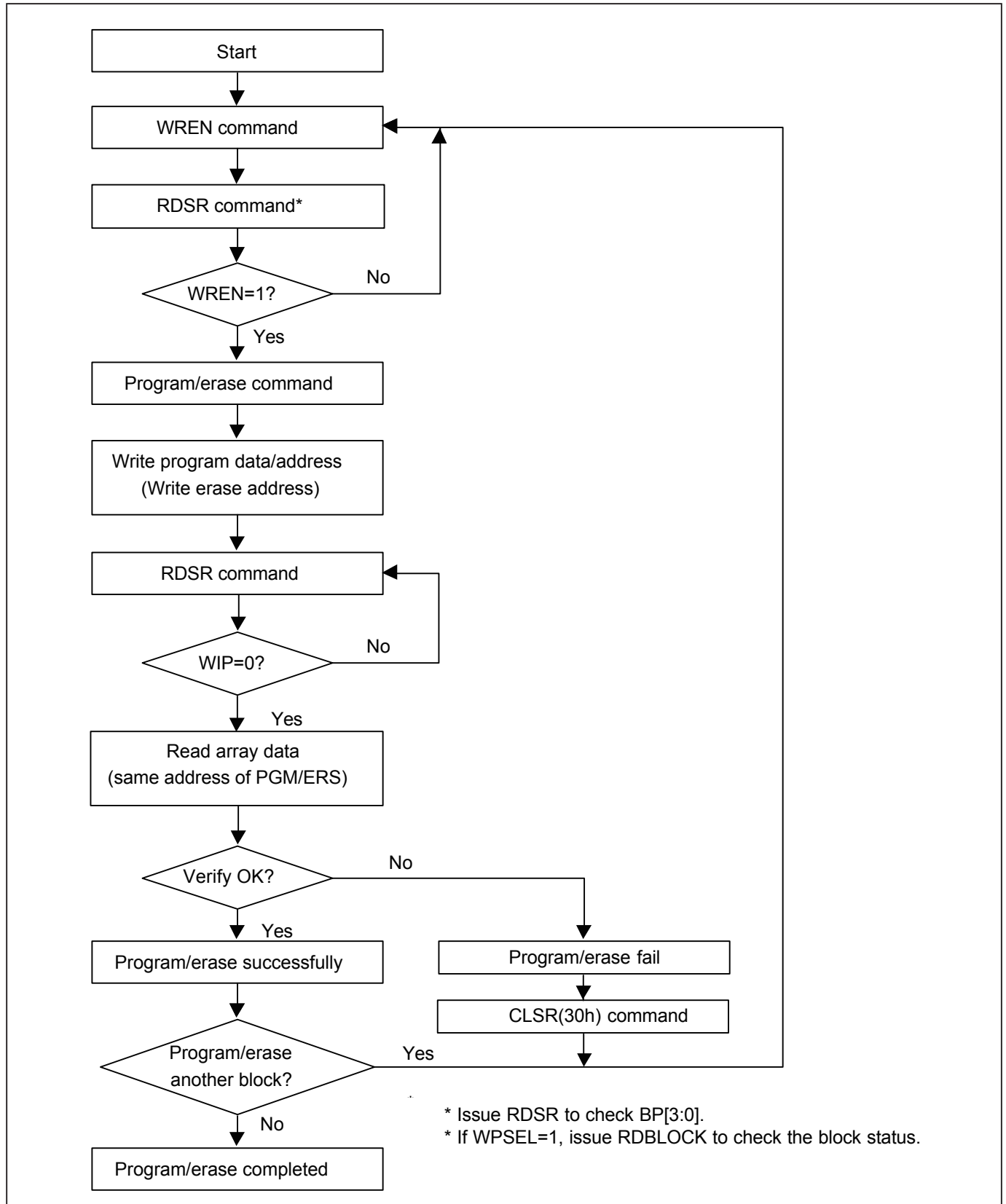
The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3, which can raise programmer performance and the effectiveness of application of lower clock less than 20MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 20MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high. (Please refer to Figure 21)

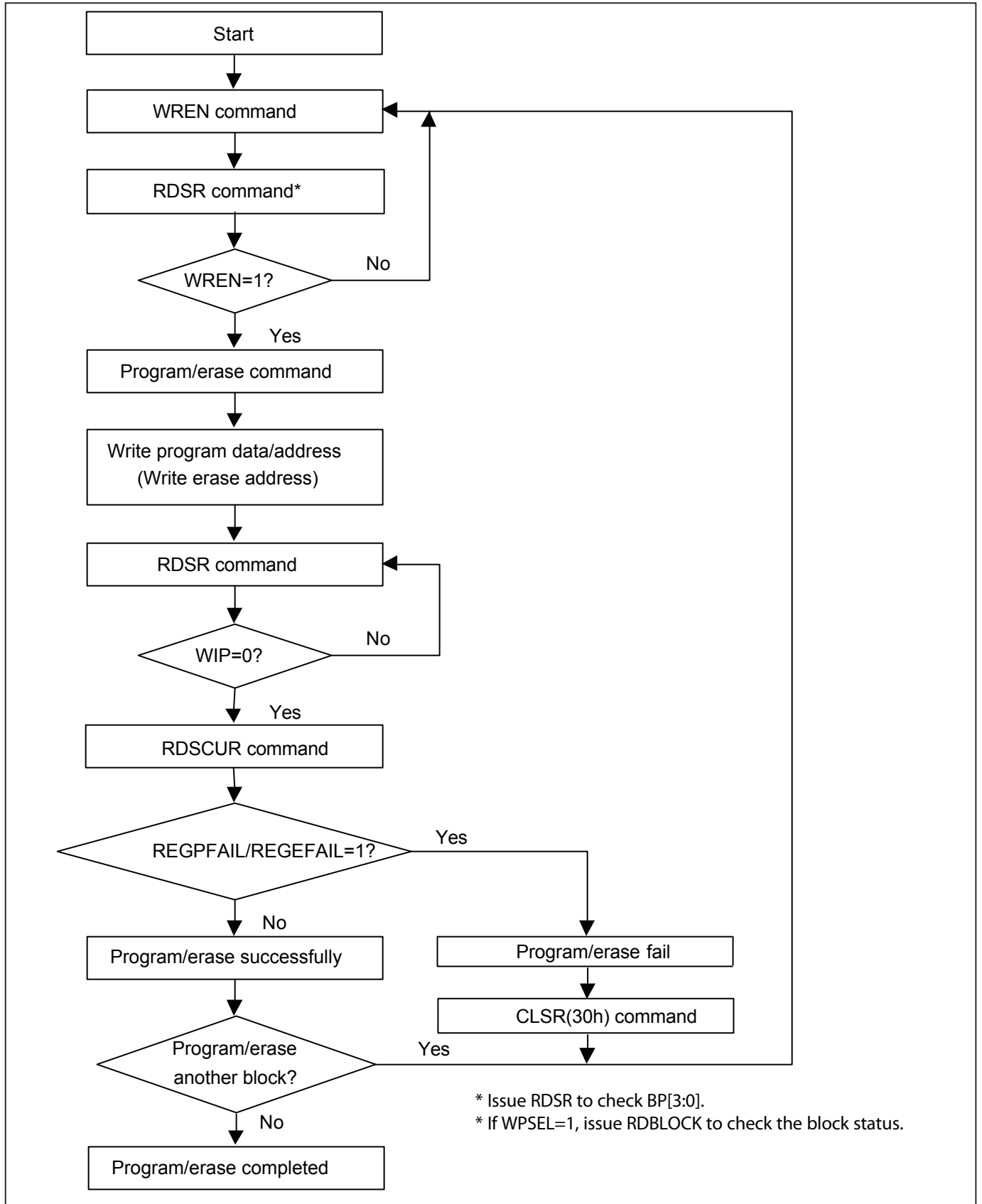
If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

The Program/Erase function instruction function flow is as follows:

Program/Erase Flow(1) with read array data



Program/Erase Flow(2) without read array data



(16) Continuously program mode (CP mode)

The CP mode may enhance program performance by automatically increasing address to the next higher address after each byte data has been programmed.

The Continuously program (CP) instruction is for multiple byte program to Flash. A write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Continuously program (CP) instruction. CS# requires to go high before CP instruction is executing. After CP instruction and address input, two bytes of data is input sequentially from MSB(bit7) to LSB(bit0). The first byte data will be programmed to the initial address range with A0=0 and second byte data with A0=1. If only one byte data is input, the CP mode will not process. If more than two bytes data are input, the additional data will be ignored and only two byte data are valid. Any byte to be programmed should be in the erase state (FF) first. It will not roll over during the CP mode, once the last unprotected address has been reached, the chip will exit CP mode and reset write Enable Latch bit (WEL) as "0" and CP mode bit as "0". Please check the WIP bit status if it is not in write progress before entering next valid instruction. During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex). And the WRDI command is valid after completion of a CP programming cycle, which means the WIP bit=0.

The sequence of issuing CP instruction is : CS# goes low → sending CP instruction code → 3-byte address on SI pin → two data bytes on SI → CS# goes high to low → sending CP instruction and then continue two data bytes are programmed → CS# goes high to low → till last desired two data bytes are programmed → CS# goes high to low → sending WRDI (Write Disable) instruction to end CP mode → send RDSR instruction to verify if CP mode word program ends, or send RDSCUR to check bit4 to verify if CP mode ends. (Please refer to Figure 22 of CP mode timing waveform)

Three methods to detect the completion of a program cycle during CP mode:

- 1) Software method-I: by checking WIP bit of Status Register to detect the completion of CP mode.
- 2) Software method-II: by waiting for a tBP time out to determine if it may load next valid command or not.
- 3) Hardware method: by writing ESRY (enable SO to output RY/BY#) instruction to detect the completion of a program cycle during CP mode. The ESRY instruction must be executed before CP mode execution. Once it is enable in CP mode, the CS# goes low will drive out the RY/BY# status on SO, "0" indicates busy stage, "1" indicates ready stage, SO pin outputs tri-state if CS# goes high. DSRY (disable SO to output RY/BY#) instruction to disable the SO to output RY/BY# and return to status register data output during CP mode. Please note that the ESRY/DSRY command are not accepted unless the completion of CP mode.

If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

(17) Parallel Mode (Highly recommended for production throughputs increasing)

The parallel mode provides 8 bit inputs/outputs for increasing throughputs of factory production purpose. The parallel mode requires 55h command code, after writing the parallel mode command and then CS# going high, after that, the Memory can be available to accept RDID/RES & REMS/READ/PP command as the normal writing command procedure. To exit parallel mode, it requires 45h command code, or power-off/on sequence. The sequence of issuing Parallel Mode instruction is : CS# goes low→sending Parallel Mode Code→CS# goes high (Please refer to Figure 23-1, Other parallel mode please refer to Figure 23-2~23-7).

- a. For normal write command (by SI), No effect
- b. Under parallel mode, the fastest access clock freq. will be changed to 6MHz (SCLK pin clock freq.)
- c. For parallel mode, the tV will be changed to 70ns.

(18) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→ CS# goes high. (Please refer to Figure 24)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

(19) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the standby Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in Table 10. Once in the standby mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycles; there's no effect on the current program/erase/write cycles in progress. The sequence is shown as Figure 25, 26.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-down Mode.

(20) Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4)

The REMS, REMS2 and REMS4 instruction provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the CS# pin low and shift the instruction code "90h", "CFh", "DFh" or "EFh" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 27. The Device ID values are listed in table of ID Definitions. If the one-byte address is initially set to 01h, then the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table 6. ID Definitions

Command Type	MX25L6436E			MX25L12836E		
	manufacturer ID	memory type	memory density	manufacturer ID	memory type	memory density
RDID	C2	20	17	C2	20	18
RES	electronic ID			electronic ID		
	16			17		
REMS/REMS2/ REMS4	manufacturer ID	device ID		manufacturer ID	device ID	
	C2	16		C2	17	

(21) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit Secured OTP mode. The additional 4K-bit Secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low → sending ENSO instruction to enter Secured OTP mode → CS# goes high.

Please note that WRSR/WRSCUR/WPSEL/SBLK/GBLK/SBULK/GBULK/CE/BE/SE/BE32K commands are not acceptable during the access of secure OTP region, once Security OTP is lock down, only read related commands are valid.

(22) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit Secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low → sending EXSO instruction to exit Secured OTP mode → CS# goes high.

(23) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low → sending RDSCUR instruction → Security Register data out on SO → CS# goes high.

The definition of the Security Register is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be update any more. While it is in 4K-bit Secured OTP mode, array access is not allowed.

Continuously Program Mode(CP mode) bit. The Continuously Program Mode bit indicates the status of CP mode, "0" indicates not in CP mode; "1" indicates in CP mode.

Program Fail Flag bit. While a program failure happened, the Program Fail Flag bit would be set. This bit will also be set when the user attempts to program a protected main memory region or a locked OTP region. This bit can indicate whether one or more of program operations fail, and can be reset by command CLSR (30h).

Erase Fail Flag bit. While a erase failure happened, the Erase Fail Flag bit would be set. This bit will also be set when the user attempts to erase a protected main memory region or a locked OTP region. This bit can indicate whether one or more of erase operations fail, and can be reset by command CLSR (30h).

Write Protection Select bit. The Write Protection Select bit indicates that WPSEL has been executed successfully. Once this bit has been set (WPSEL=1), all the blocks or sectors will be write-protected after the power-on every time. Once WPSEL has been set, it cannot be changed again, which means it's only for individual WP mode.

Under the individual block protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SRAM lock bits.

Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Continuously Program mode (CP mode)	x	x	LDSO (lock-down 4K-bit Secured OTP)	4K-bit Secured OTP
0=normal WP mode 1=individual WP mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	0=normal Program mode 1=CP mode (default=0)	reserved	reserved	0 = not lockdown 1 = lock-down (cannot program/erase OTP)	0 = nonfactory lock 1 = factory lock
non-volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit
OTP	Read Only	Read Only	Read Only	Read Only	Read Only	OTP	Read Only

(24) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

(25) Write Protection Selection (WPSEL)

There are two write protection methods, (1) BP protection mode (2) individual block protection mode. If WPSEL=0, flash is under BP protection mode. If WPSEL=1, flash is under individual block protection mode. The default value of WPSEL is "0". WPSEL command can be used to set WPSEL=1. **Please note that WPSEL is an OTP bit. Once WPSEL is set to 1, there is no chance to recovery WPSEL back to "0".** If the flash is put on BP mode, the individual block protection mode is disabled. Contrarily, if flash is on the individual block protection mode, the BP mode is disabled.

Every time after the system is powered-on, and the Security Register bit 7 is checked to be WPSEL=1, all the blocks or sectors will be write protected by default. User may only unlock the blocks or sectors via SBULK and GBULK instruction. Program or erase functions can only be operated after the Unlock instruction is conducted.

BP protection mode. WPSEL=0:

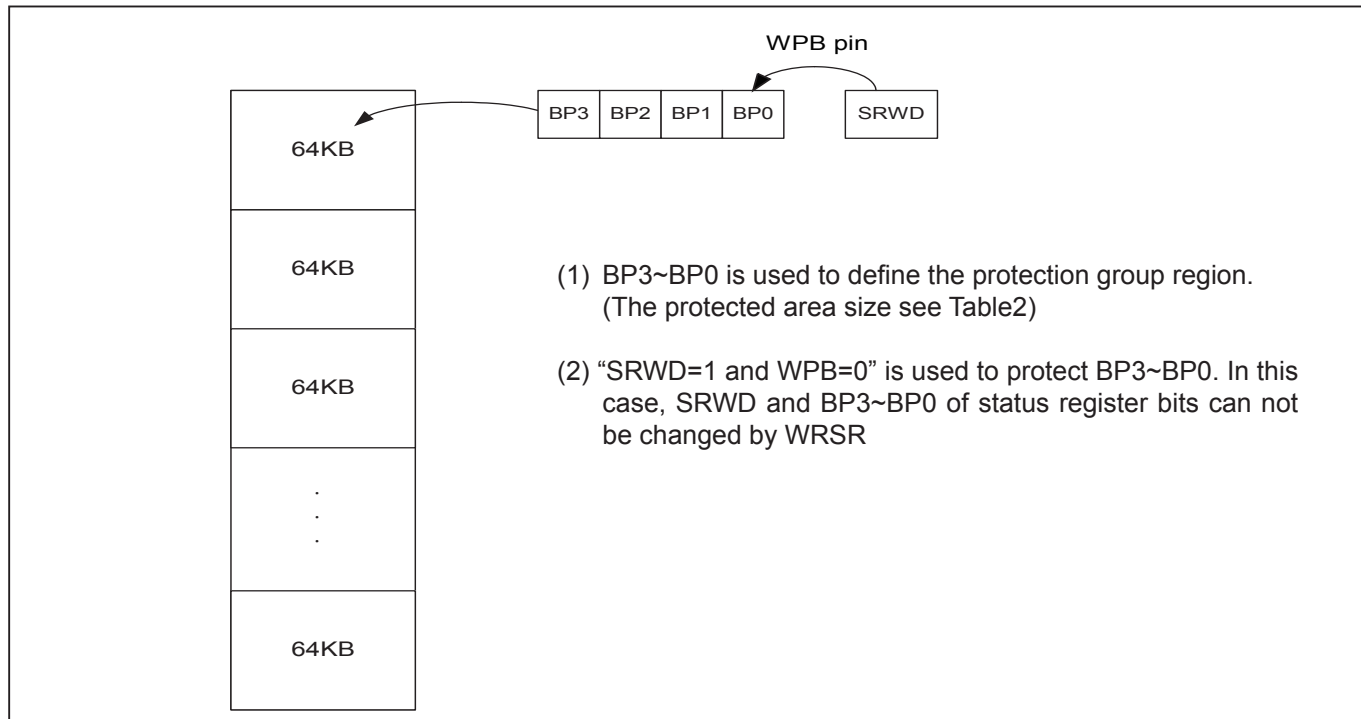
ARRAY is protected by BP3~BP0 and BP3~BP0 bits are protected by "SRWD=1 and WP#=0", where SRWD is bit 7 of status register that can be set by WRSR command.

Individual block protection mode. WPSEL=1:

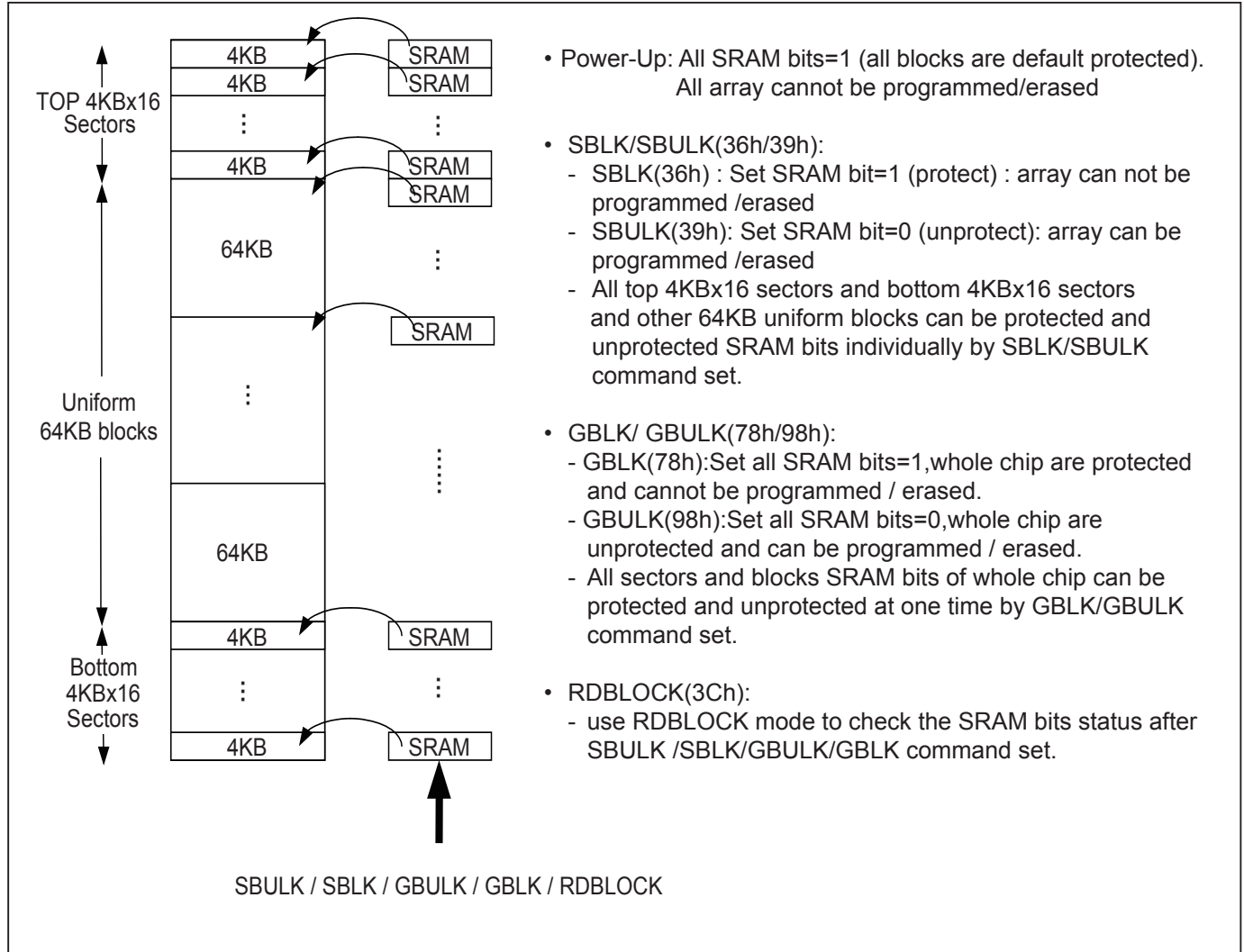
Blocks are individually protected by their own SRAM lock bits which are set to "1" after power up. SBULK and SBLK command can set SRAM lock bit to "0" and "1". When the system accepts and executes WPSEL instruction, the bit 7 in security register will be set. It will activate SBLK, SBULK, RDBLOCK, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3~BP0) indicated block methods. Under the individual block protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SRAM lock bits.

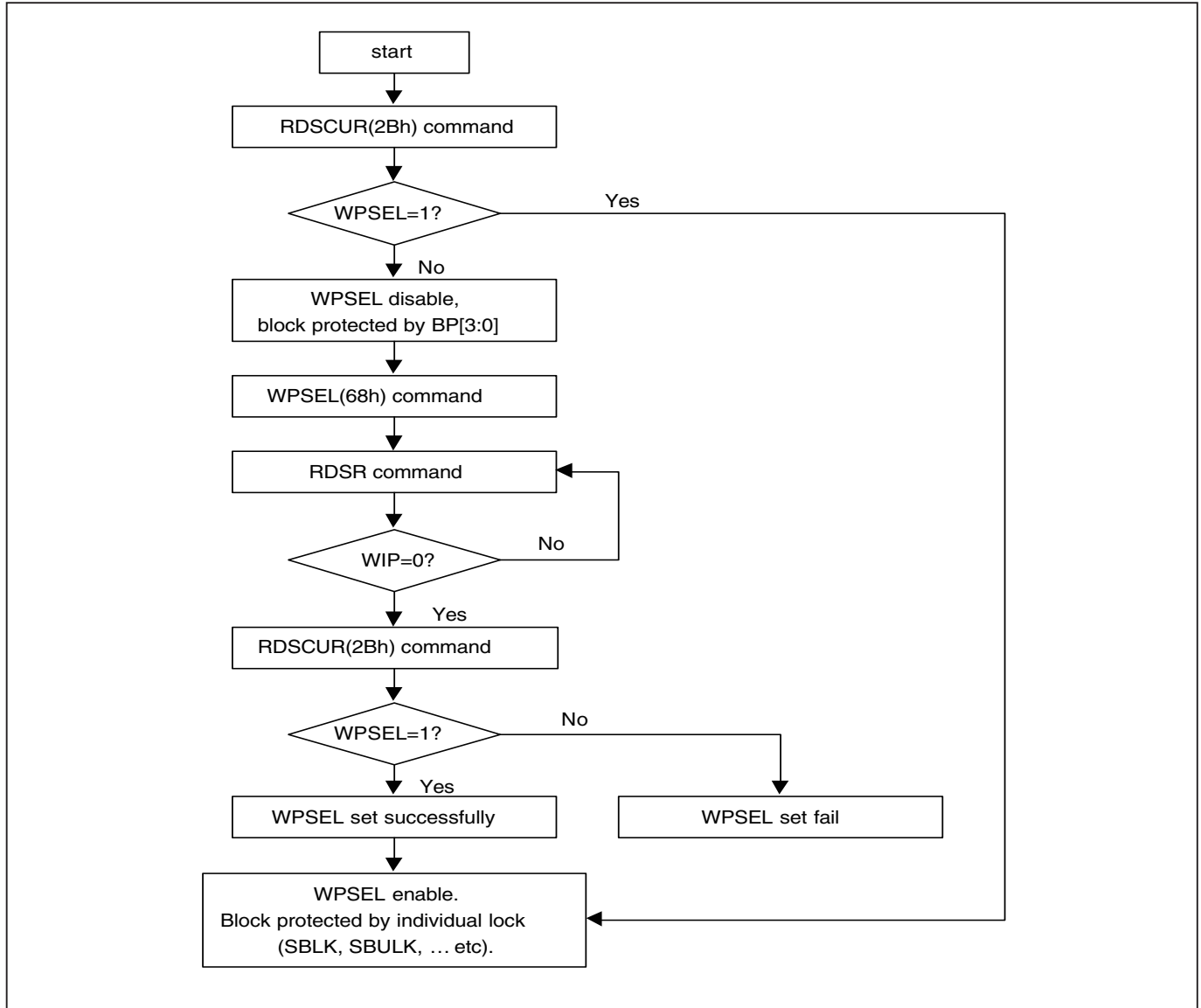
The sequence of issuing WPSEL instruction is: CS# goes low → sending WPSEL instruction to enter the individual block protect mode → CS# goes high. (Figure 28)

WPSEL instruction function flow is as follows:

BP and SRWD if WPSEL=0

The individual block lock mode is effective after setting WPSEL=1



WPSEL Flow

(26) Single Block Lock/Unlock Protection (SBLK/SBULK)

These instructions are only effective after WPSEL was executed. The SBLK instruction is for write protection a specified block (or sector) of memory, using A23-A16 or (A23-A12) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

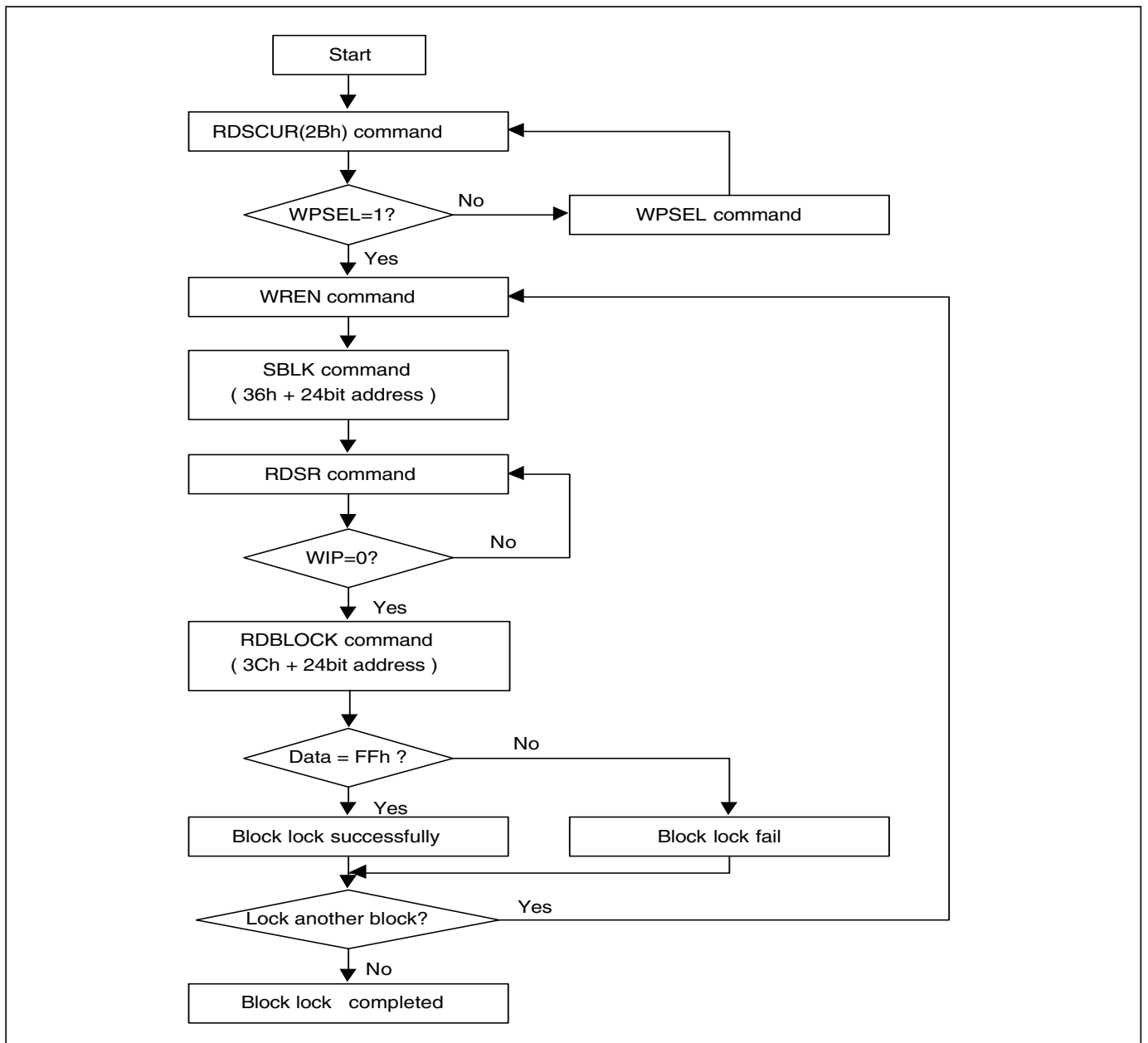
The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.

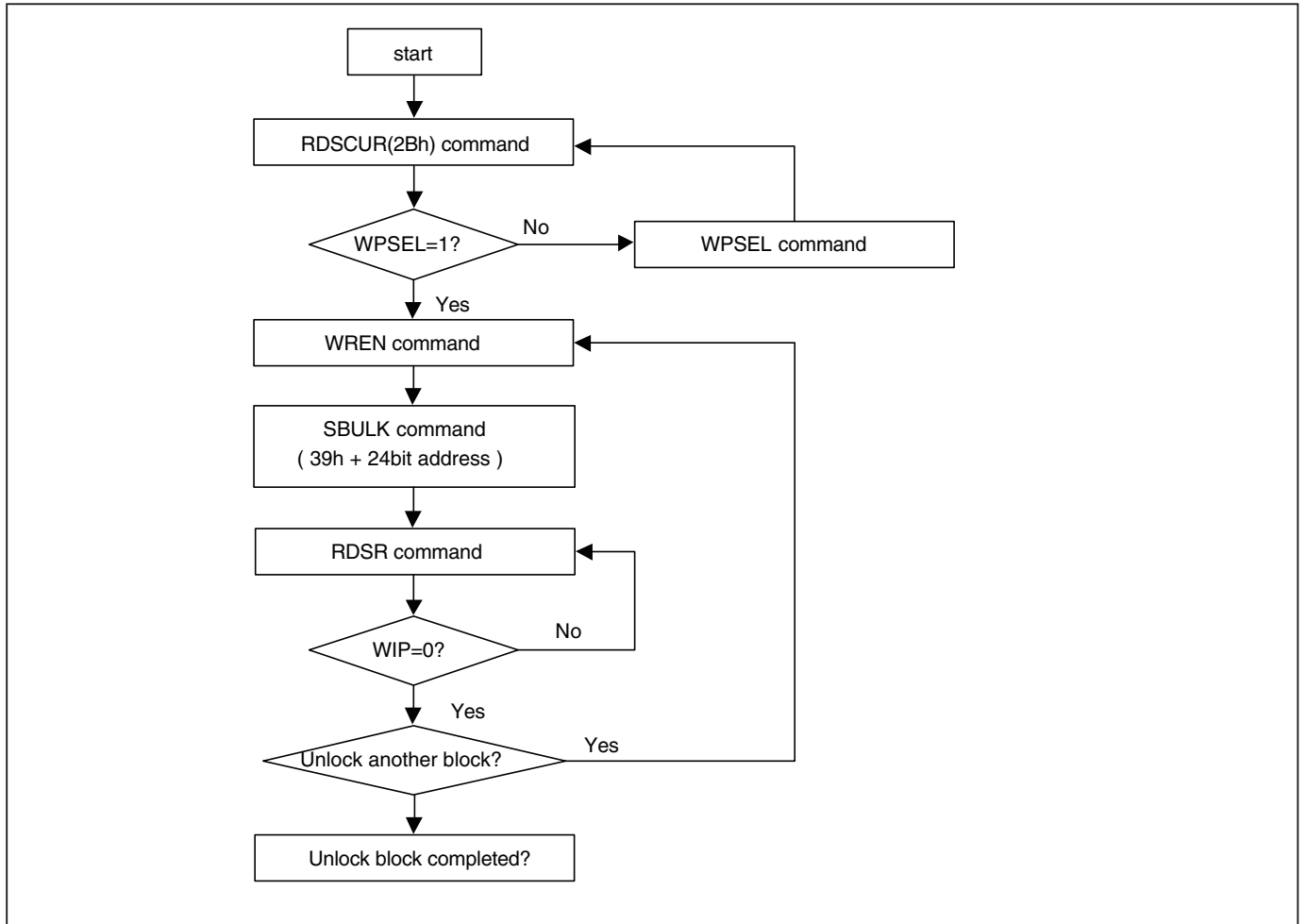
The sequence of issuing SBLK/SBULK instruction is: CS# goes low → send SBLK/SBULK (36h/39h) instruction → send 3 address bytes assign one block (or sector) to be protected on SI pin → CS# goes high. (Figure 29)

The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

SBLK/SBULK instruction function flow is as follows:

Block Lock Flow



Block Unlock Flow

(27) Read Block Lock Status (RDBLOCK)

This instruction is only effective after WPSEL was executed. The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using A23-A16 (or A23-A12) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is "1" to indicate that this block has been protected, that user can read only but cannot write/program/erase this block. The status bit is "0" to indicate that this block hasn't been protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Ch) instruction → send 3 address bytes to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high. (Please refer to Figure 30)

(28) Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is for enable/disable the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.

The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction → CS# goes high. (Please refer to Figure 31)

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

(29) Clear SR Fail Flags (CLSR)

The CLSR instruction is for resetting the Program/Erase Fail Flag bit of Security Register. It should be executed before program/erase another block during programming/erasing flow without read array data.

The sequence of issuing CLSR instruction is: CS# goes low → send CLSR instruction code → CS# goes high.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

(30) Enable SO to Output RY/BY# (ESRY)

The ESRY instruction is for outputting the ready/busy status to SO during CP mode.

The sequence of issuing ESRY instruction is: CS# goes low → sending ESRY instruction code → CS# goes high.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

(31) Disable SO to Output RY/BY# (DSRY)

The DSR Y instruction is for resetting ESRY during CP mode. The ready/busy status will not output to SO after DSR Y issued.

The sequence of issuing DSR Y instruction is: CS# goes low → send DSR Y instruction code → CS# goes high.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

(32) Read CFI mode (RDCFI)

MX25L6436E/12836E features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, operating voltages and timing information of this device by CFI mode. Writes the CFI Query command "5AH". The system can read CFI information at the addresses given. A reset command is required to exit CFI mode and go back to ready array mode. The system can write the CFI Query command only when the device is in read mode.

The identification data values in under TBD status. The sequence of issuing RDCFI instruction is CS# goes low → send RDCFI (5A) instruction → send 3 address bytes on SI pin → send 1 dummy byte on SI pin → read CFI code → CS# goes high.

CFI mode identification data value is under TBD.

POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not Deep Power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal Power-on Reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the figure of "Power-up Timing".

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-55°C to 125°C
Applied Input Voltage		-0.5V to 4.6V
Applied Output Voltage		-0.5V to 4.6V
VCC to Ground Potential		-0.5V to 4.6V

NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figure 2, 3.

Figure 2. Maximum Negative Overshoot Waveform

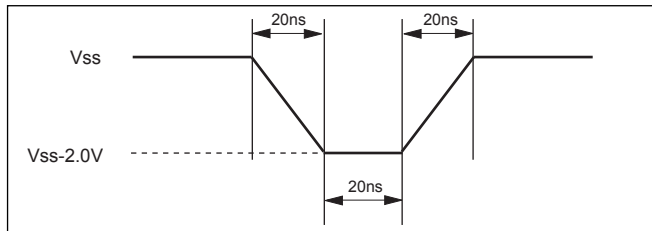
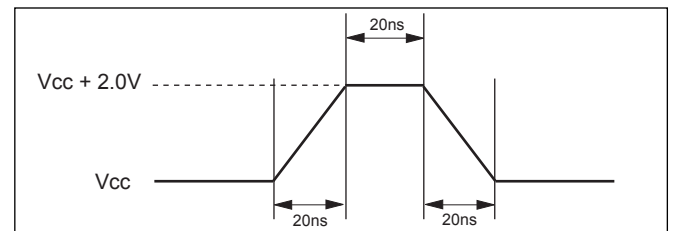


Figure 3. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COU	Output Capacitance			8	pF	VOU = 0V

Figure 4. OUTPUT LOADING

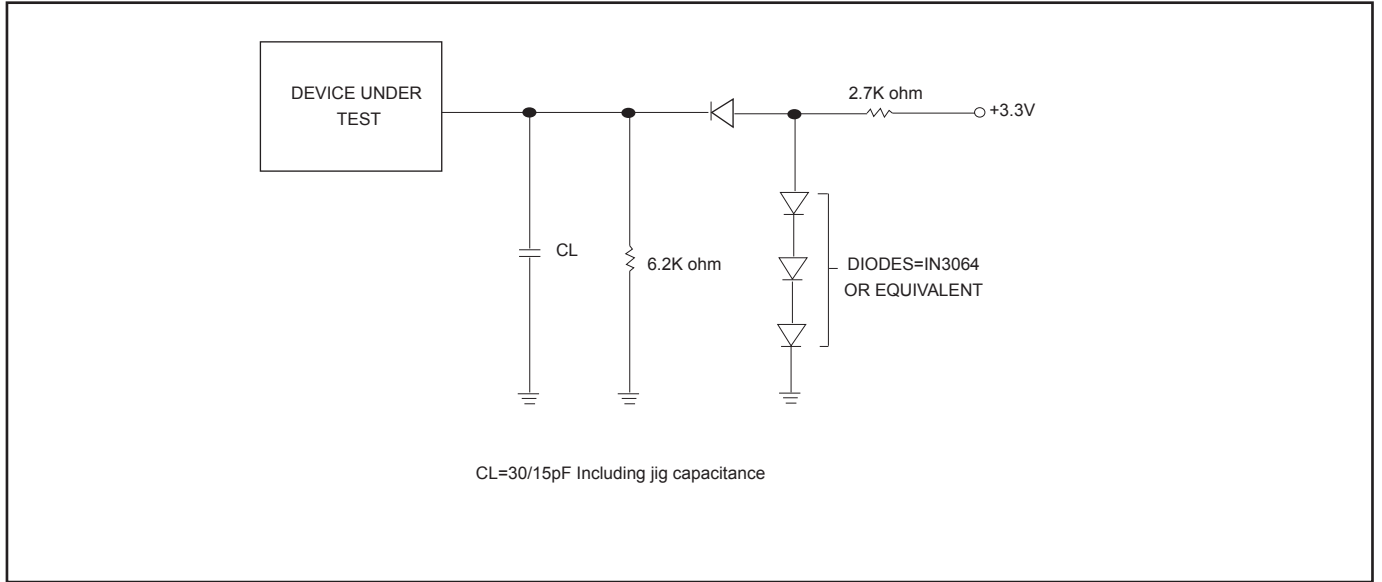


Table 7-1. MX25L6436E DC CHARACTERISTICS

(Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1		± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1		± 2	uA	VCC = VCC Max, VIN = VCC or GND
ISB1	VCC Standby Current	1		100	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			30	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		45	mA	f=104MHz, fQ=75MHz (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				40	mA	f=66MHz, fT=75MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				30	mA	f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5	0.8	V	
VIH	Input High Voltage		0.7VCC	VCC+0.4	V	
VOL	Output Low Voltage			0.4	V	IOL = 1.6mA; IOL = 140uA for parallel mode
VOH	Output High Voltage		VCC-0.2		V	IOH = -100uA; IOH = 65uA for parallel mode

Notes :

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 7-2. MX25L12836E DC CHARACTERISTICS

(Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1		± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1		± 2	uA	VCC = VCC Max, VIN = VCC or GND
ISB1	VCC Standby Current	1		100	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			40	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		45	mA	f=104MHz, fQ=75MHz (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				40	mA	f=66MHz, fT=75MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				30	mA	f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5	0.8	V	
VIH	Input High Voltage		0.7VCC	VCC+0.4	V	
VOL	Output Low Voltage			0.4	V	IOL = 1.6mA; IOL = 140uA for parallel mode
VOH	Output High Voltage		VCC-0.2		V	IOH = -100uA; IOH = 65uA for parallel mode

Notes :

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 8-1. MX25L6436E AC CHARACTERISTICS

(Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit	
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES,RDP WREN, WRDI, RDID, RDSR, WRSR			104	MHz	
fRSCLK	fR	Clock Frequency for READ instructions			50	MHz	
fTCLK	fT	Clock Frequency for DREAD instructions			70	MHz	
	fQ	Clock Frequency for QREAD instructions			70	MHz	
f4PP		Clock Frequency for 4PP (Quad page program)			20	MHz	
tCH(1)	tCLH	Clock High Time	Fast_Read	4.5		ns	
			Read	9		ns	
tCL(1)	tCLL	Clock Low Time	Fast_Read	4.5		ns	
			Read	9		ns	
tCLCH(2)		Clock Rise Time (3) (peak to peak)	0.1			V/ns	
tCHCL(2)		Clock Fall Time (3) (peak to peak)	0.1			V/ns	
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	8			ns	
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns	
tDVCH	tDSU	Data In Setup Time	2			ns	
tCHDX	tDH	Data In Hold Time	5			ns	
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns	
tSHCH		CS# Not Active Setup Time (relative to SCLK)	8			ns	
tSHSL(3)	tCSH	CS# Deselect Time	Read	15		ns	
			Write/Erase/ Program	50		ns	
tSHQZ(2)	tDIS	Output Disable Time	2.7V-3.6V		10	ns	
			3.0V-3.6V		8	ns	
tCLQV	tV	Clock Low to Output Valid VCC=2.7V~3.6V	Loading: 15pF	1 I/O		9	ns
				2 I/O & 4 I/O		9.5	ns
				2 I/O & 4 I/O		12	ns
tCLQX	tHO	Output Hold Time	2			ns	
tWHSL(4)		Write Protect Setup Time	20			ns	
tSHWL(4)		Write Protect Hold Time	100			ns	
tDP(2)		CS# High to Deep Power-down Mode			10	us	
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read			100	us	
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read			100	us	
tW		Write Status Register Cycle Time		40	100	ms	
tBP		Byte-Program		9	300	us	
tPP		Page Program Cycle Time		1.4	5	ms	
tSE		Sector Erase Cycle Time (4KB)		60	300	ms	
tBE		Block Erase Cycle Time (32KB)		0.5	2	s	
tBE		Block Erase Cycle Time (64KB)		0.7	2	s	
tCE		Chip Erase Cycle Time		50	80	s	
tWPS		Write Protection Selection Time			1	ms	
tWSR		Write Security Register Time			1	ms	

Notes:

1. tCH + tCL must be greater than or equal to 1/ fC.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

Table 8-2. MX25L12836E AC CHARACTERISTICS

(Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter	Min.	Max.	Unit		
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR	Serial		104	MHz	
			Parallel		6	MHz	
fRSCLK	fR	Clock Frequency for READ instructions		50	MHz		
fTCLK	fT	Clock Frequency for DREAD instructions		70	MHz		
	fQ	Clock Frequency for QREAD instructions		70	MHz		
f4PP		Clock Frequency for 4PP (Quad page program)		20	MHz		
tCH(1)	tCLH	Clock High Time	Serial	4.5 (Fast_Read)		ns	
			Serial	9 (Read)		ns	
			Parallel	30		ns	
tCL(1)	tCLL	Clock Low Time	Serial	4.5 (Fast_Read)		ns	
			Serial	9 (Read)		ns	
			Parallel	30		ns	
tCLCH(2)		Clock Rise Time (3) (peak to peak)	Serial	0.1		V/ns	
			Parallel	0.25		V/ns	
tCHCL(2)		Clock Fall Time (3) (peak to peak)	Serial	0.1		V/ns	
			Parallel	0.25		V/ns	
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	8		ns		
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5		ns		
tDVCH	tDSU	Data In Setup Time	Serial	2		ns	
			Parallel	10		ns	
tCHDX	tDH	Data In Hold Time	Serial	5		ns	
			Parallel	10		ns	
tCHSH		CS# Active Hold Time (relative to SCLK)	Serial	5		ns	
			Parallel	30		ns	
tSHCH		CS# Not Active Setup Time (relative to SCLK)	8		ns		
tSHSL(3)	tCSH	CS# Deselect Time	Read	15		ns	
			Write/Erase/Program	50		ns	
tSHQZ(2)	tDIS	Output Disable Time	2.7V-3.6V Serial		10	ns	
			3.0V-3.6V Serial		8	ns	
			Parallel		20	ns	
tCLQV	tV	Clock Low to Output Valid VCC=2.7V~3.6V	Loading: 15pF	1 I/O		9	ns
				2 I/O & 4 I/O		9.5	ns
			Loading: 30pF	2 I/O & 4 I/O		12	ns
				Parallel		70	ns



Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tCLQX	tHO	Output Hold Time	2			ns
tWHSL(4)		Write Protect Setup Time	20			ns
tSHWL(4)		Write Protect Hold Time	100			ns
tDP(2)		CS# High to Deep Power-down Mode			10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read			100	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read			100	us
tW		Write Status Register Cycle Time		40	100	ms
tBP		Byte-Program		9	300	us
tPP		Page Program Cycle Time		1.4	5	ms
tSE		Sector Erase Cycle Time (4KB)		60	300	ms
tBE		Block Erase Cycle Time (32KB)		0.5	2	s
tBE		Block Erase Cycle Time (64KB)		0.7	2	s
tCE		Chip Erase Cycle Time		80	200	s
tWPS		Write Protection Selection Time			1	ms
tWSR		Write Security Register Time			1	ms

Notes:

1. tCH + tCL must be greater than or equal to 1/ fC.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

Timing Analysis

Figure 5. Serial Input Timing

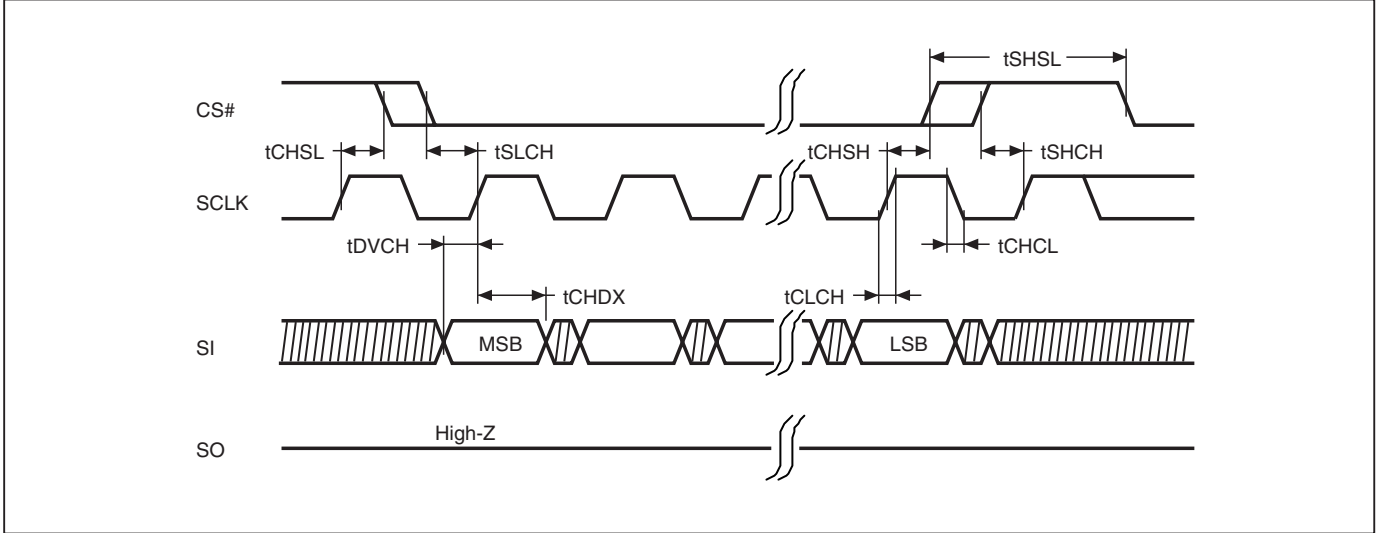


Figure 6. Output Timing

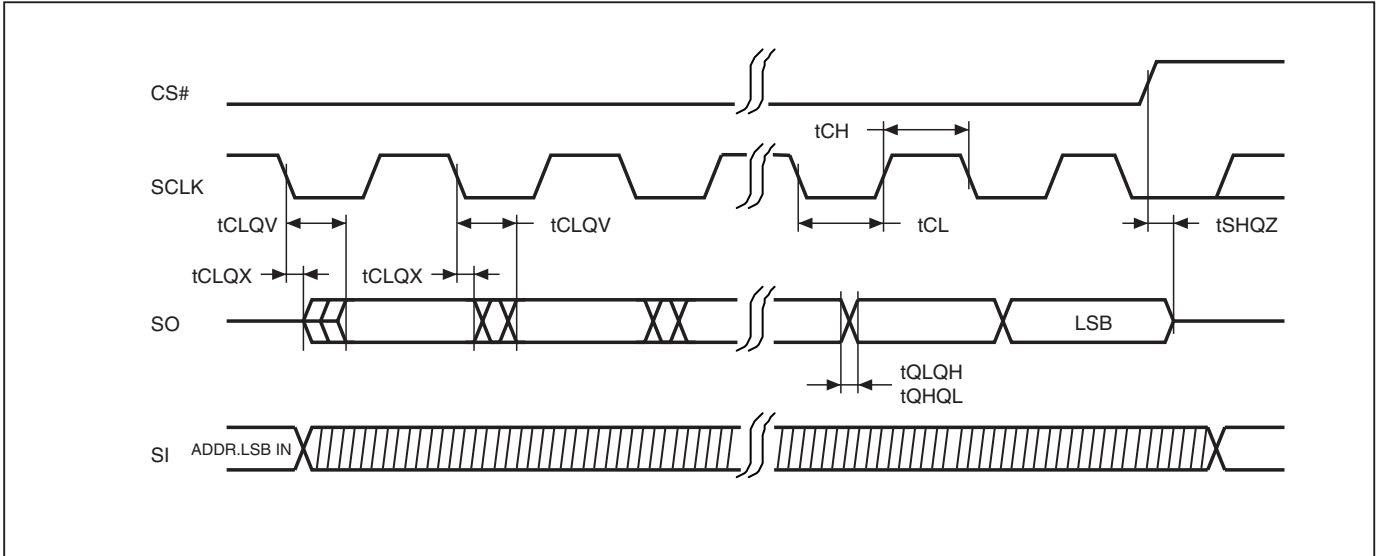


Figure 7. WP# Setup Timing and Hold Timing during WRSR when SRWD=1

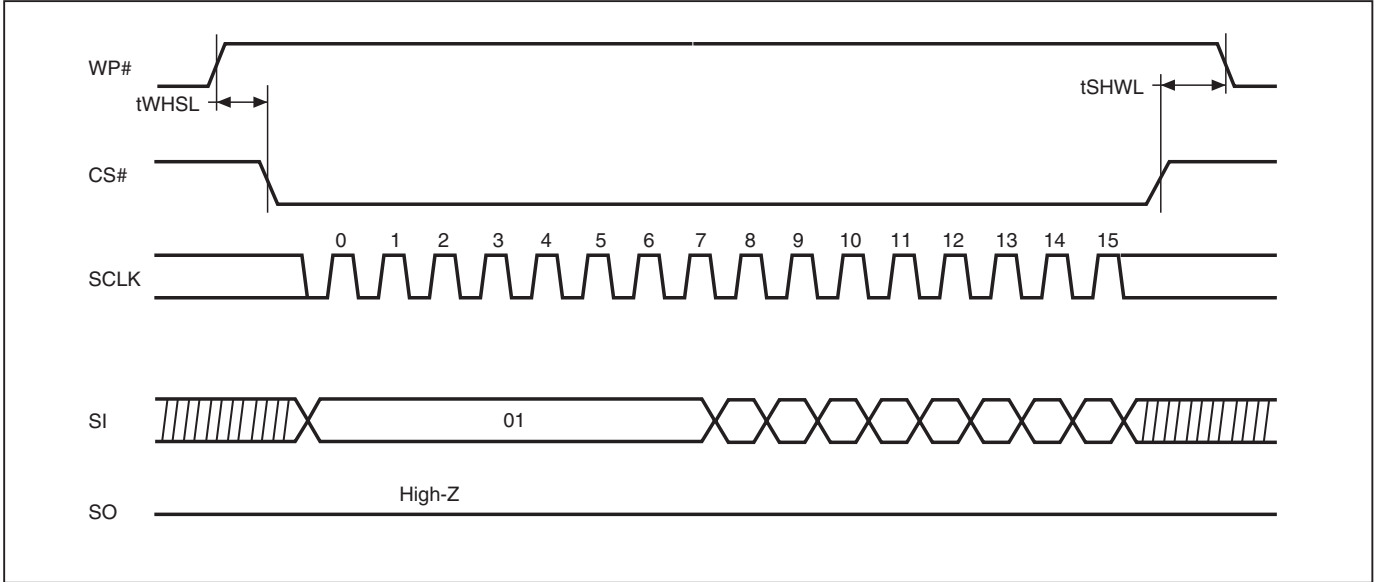


Figure 8. Write Enable (WREN) Sequence (Command 06)

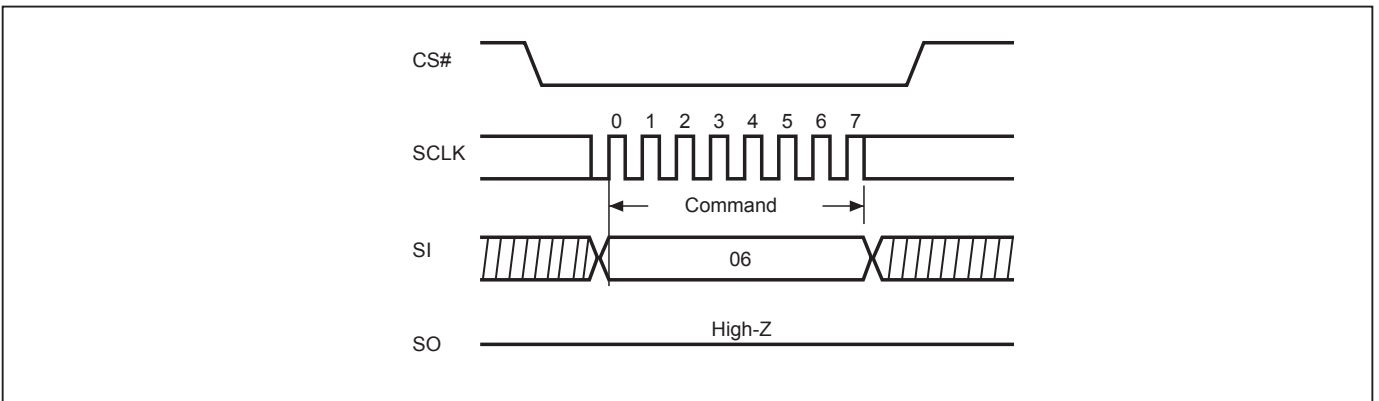


Figure 9. Write Disable (WRDI) Sequence (Command 04)

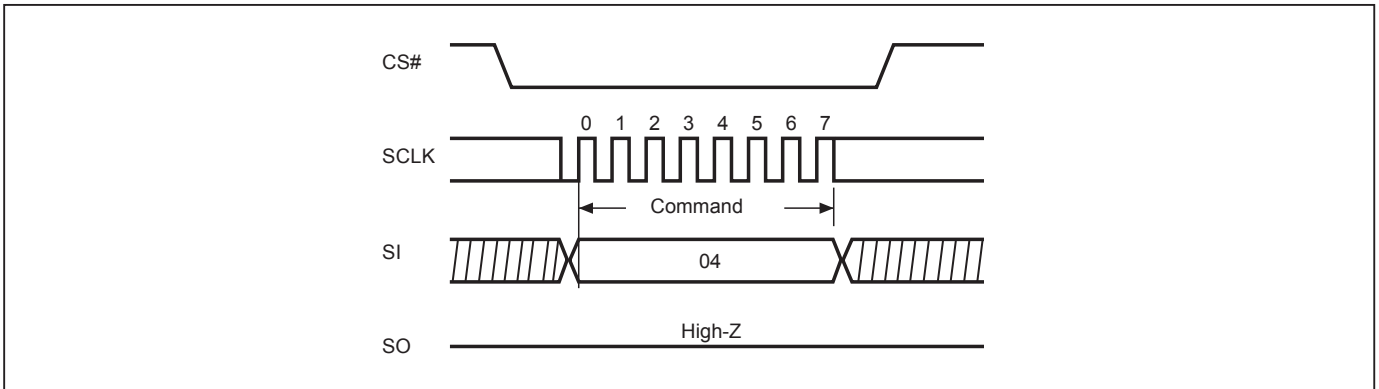


Figure 10. Read Identification (RDID) Sequence (Command 9F)

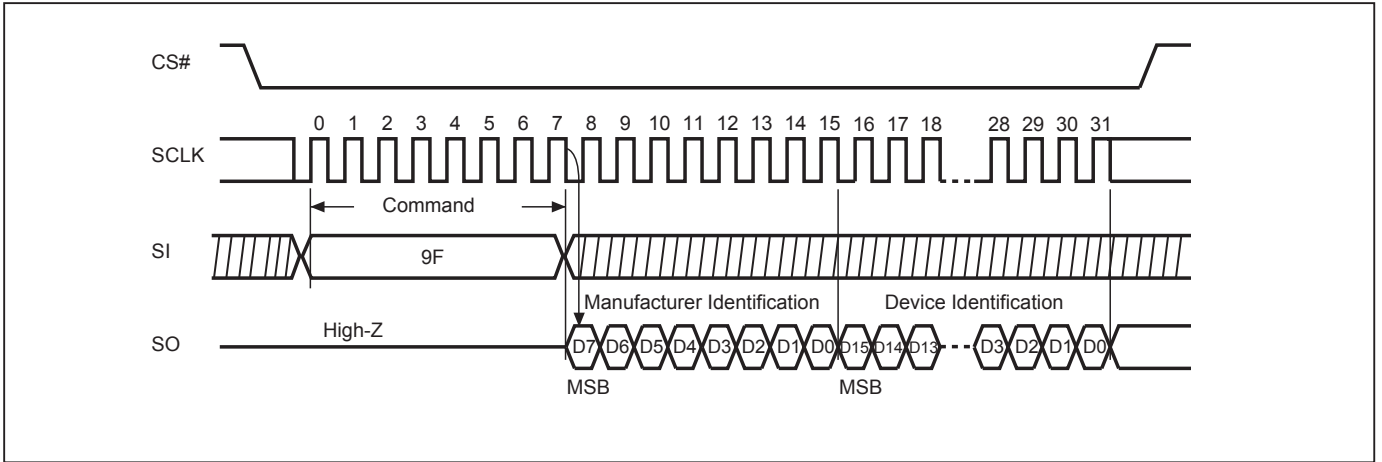


Figure 11. Read Status Register (RDSR) Sequence (Command 05)

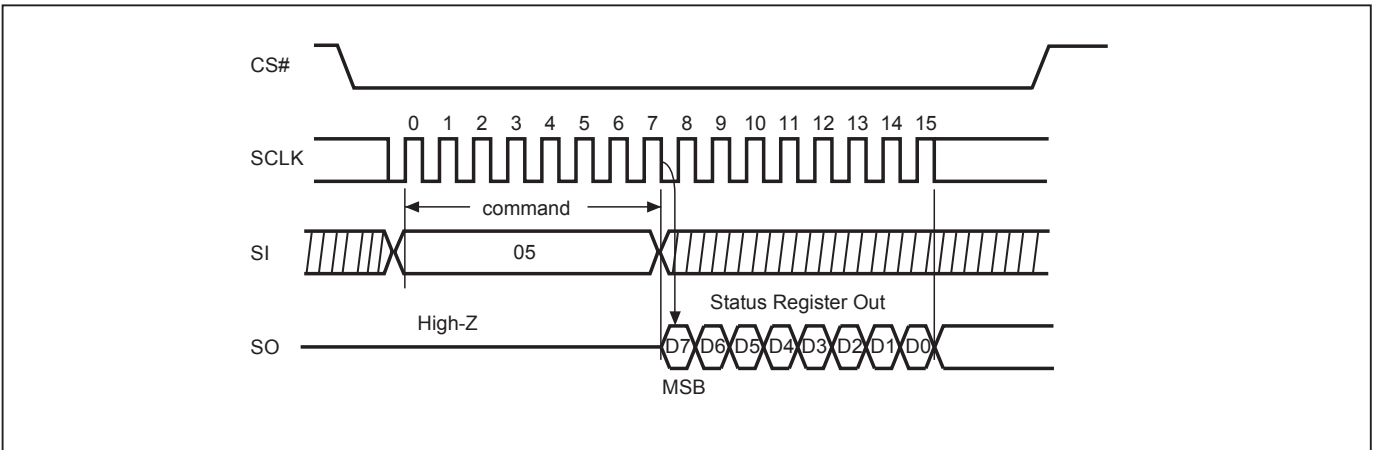


Figure 12. Write Status Register (WRSR) Sequence (Command 01)

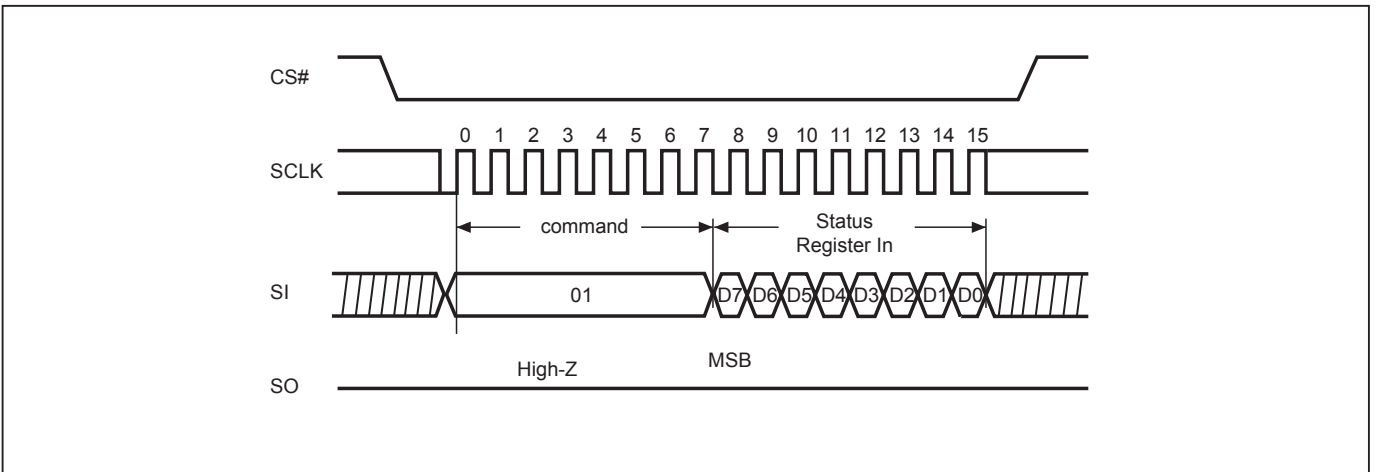


Figure 13. Read Data Bytes (READ) Sequence (Command 03)

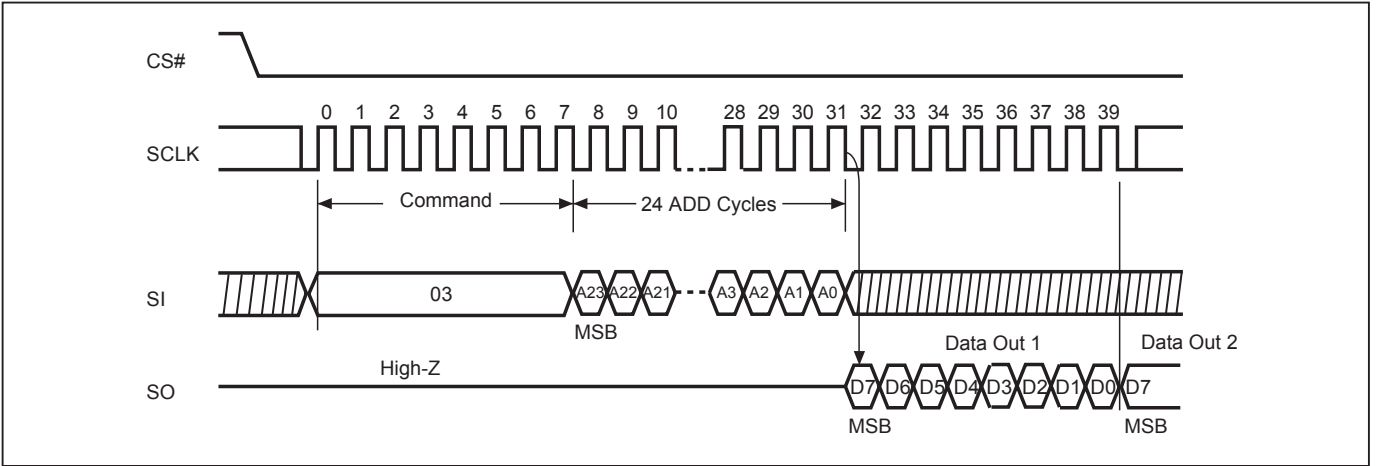


Figure 14. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

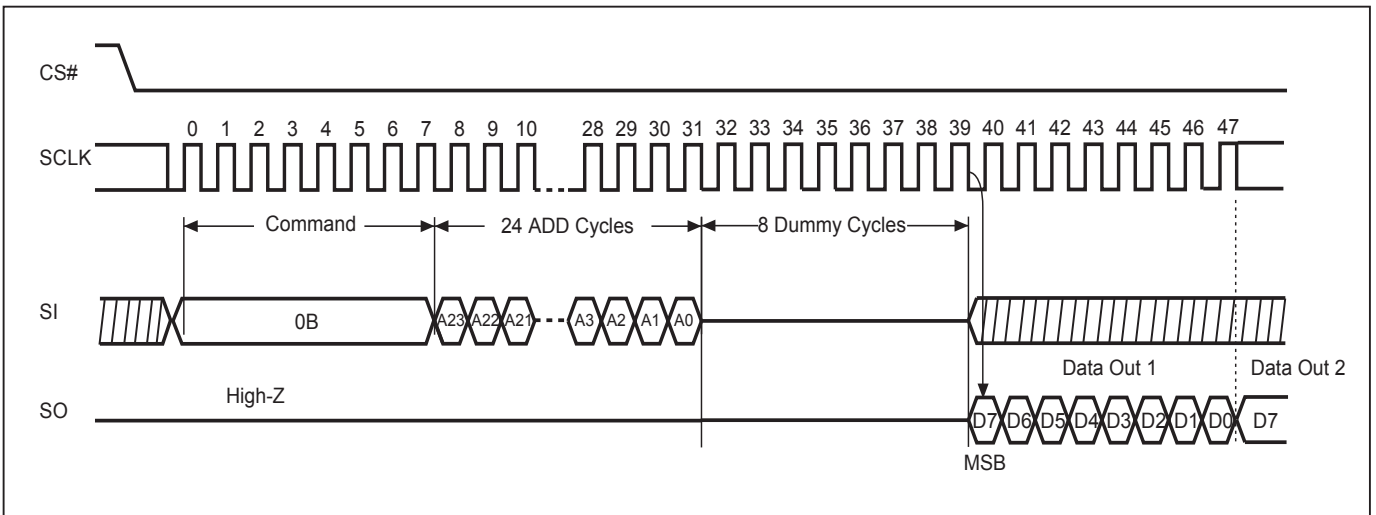


Figure 15. Dual Read Mode Sequence (Command 3B)

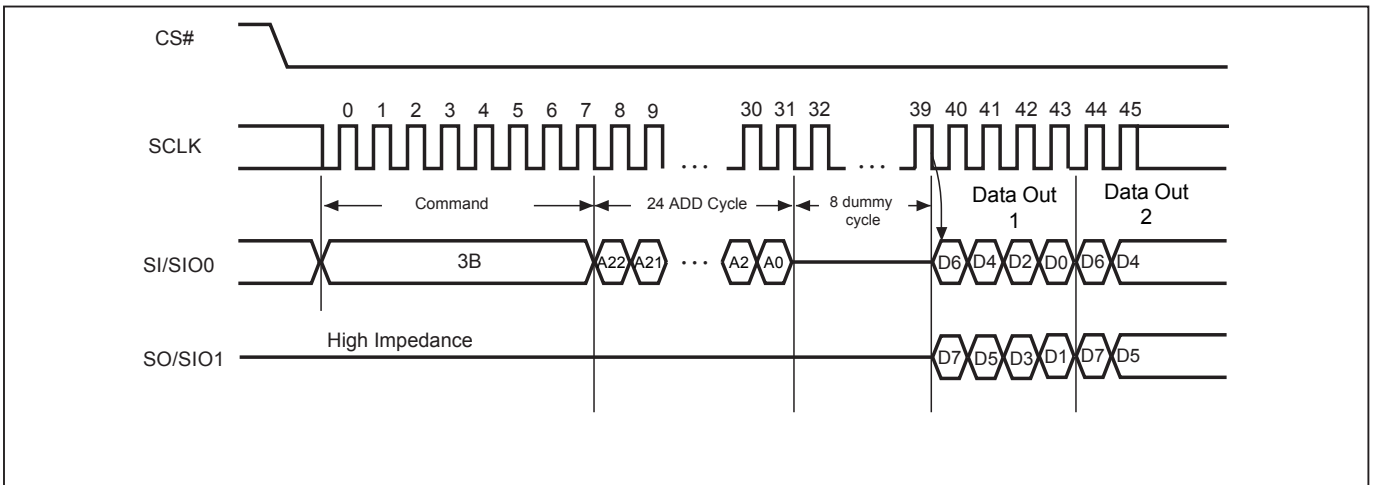


Figure 16. Quad Read Mode Sequence (Command 6B)

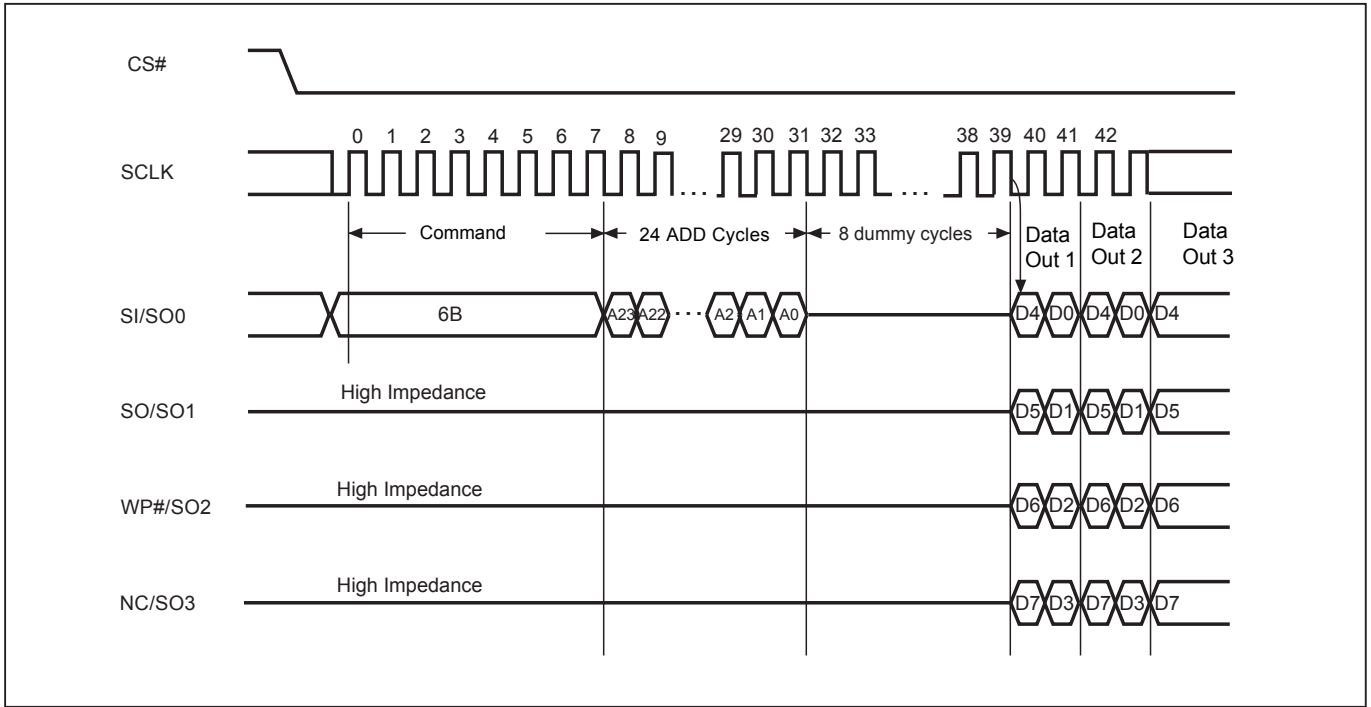


Figure 17. Sector Erase (SE) Sequence (Command 20)

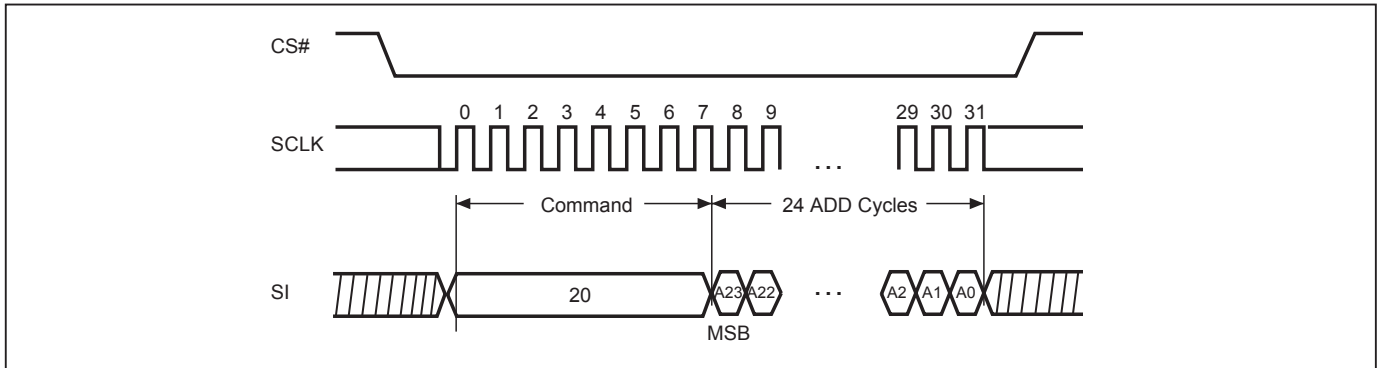


Figure 18. Block Erase (BE/EB32K) Sequence (Command D8/52)

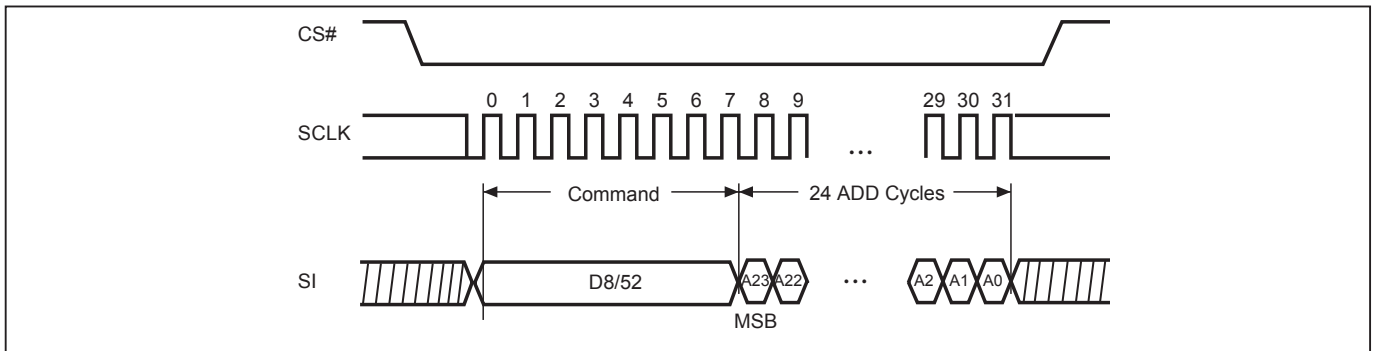


Figure 19. Chip Erase (CE) Sequence (Command 60 or C7)

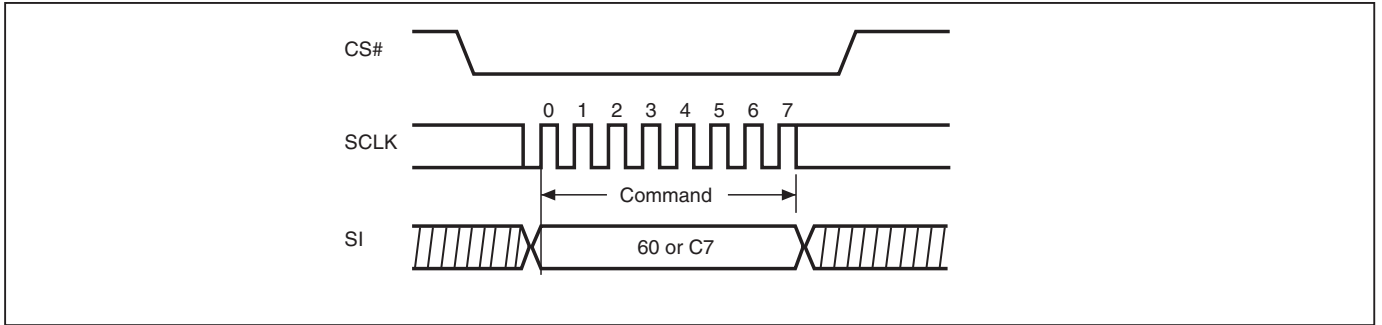


Figure 20. Page Program (PP) Sequence (Command 02)

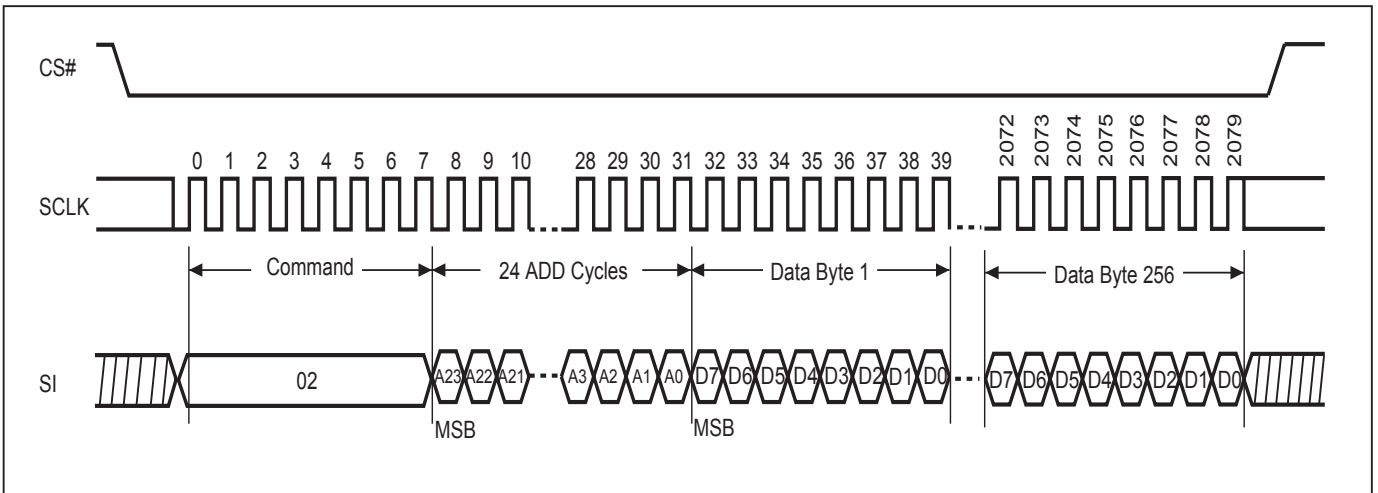


Figure 21. 4 x I/O Page Program (4PP) Sequence (Command 38)

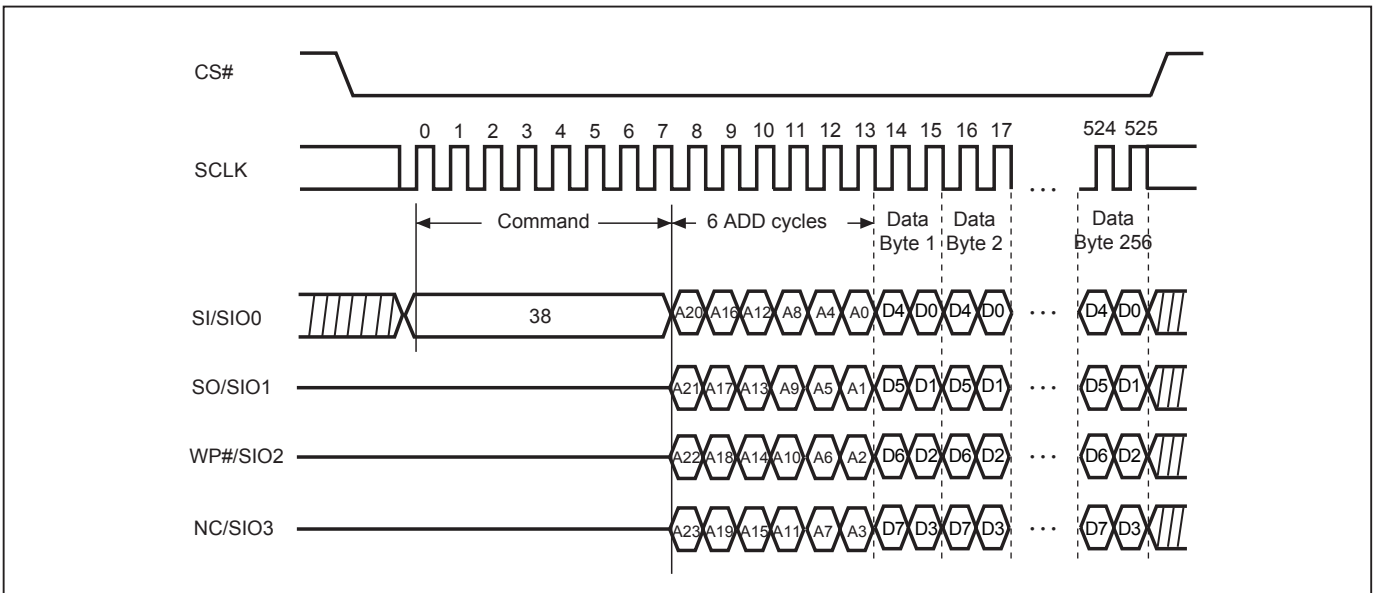
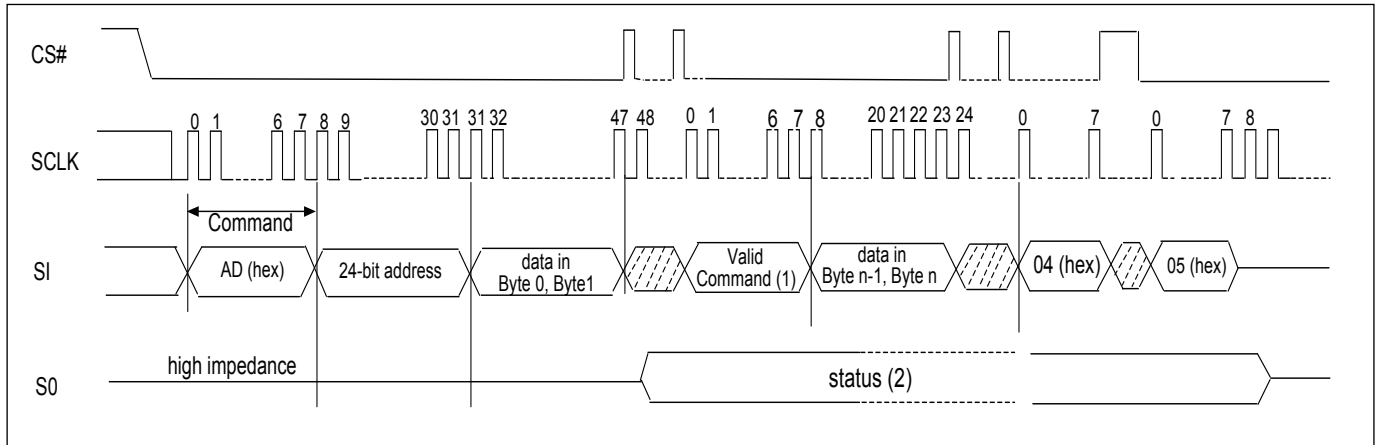
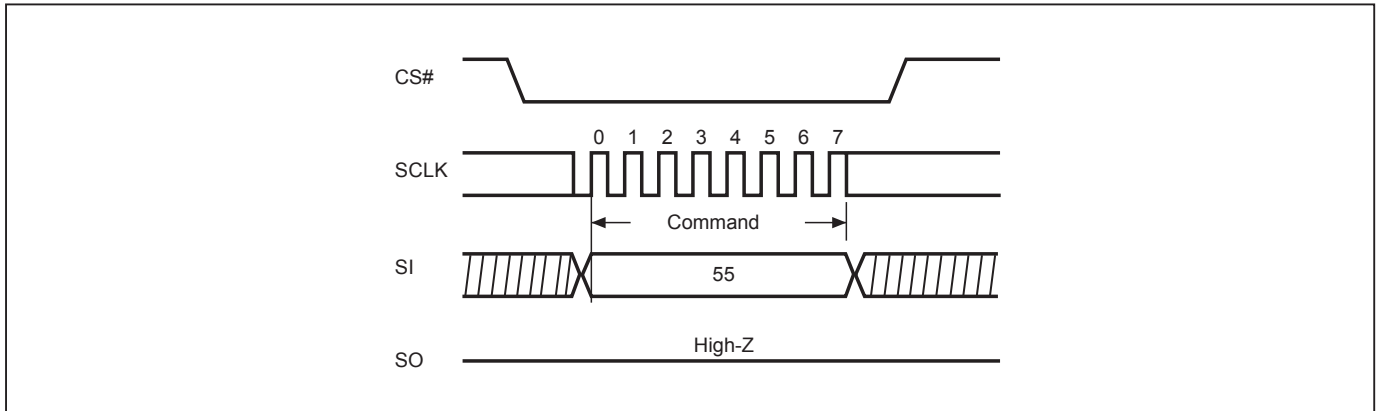
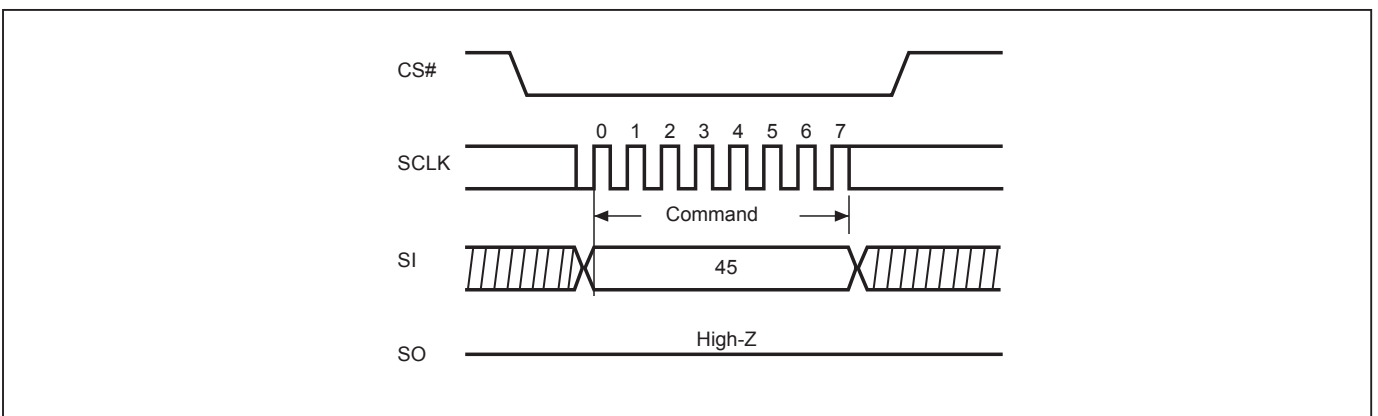
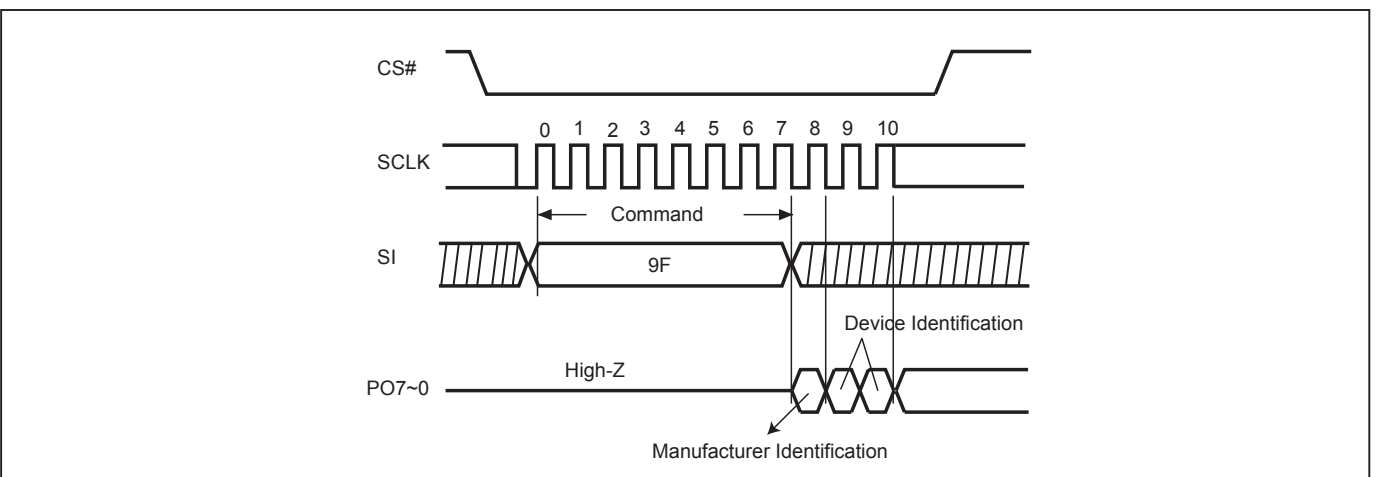


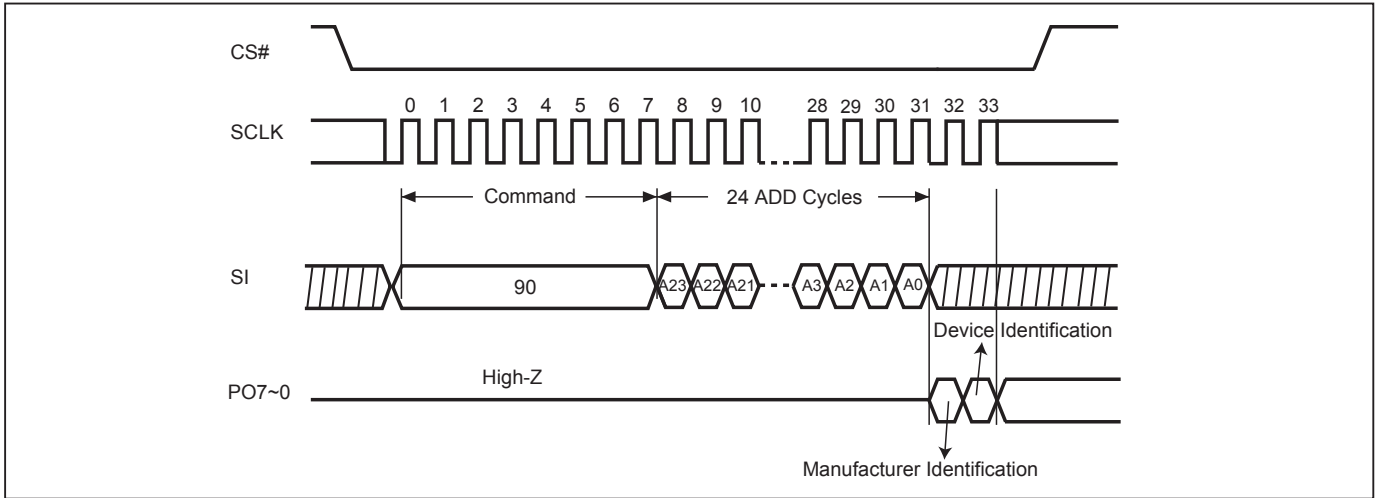
Figure 22. Continuously Program (CP) Mode Sequence with Hardware Detection (Command AD)**Note:**

- (1) During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex).
- (2) Once an internal programming operation begins, CS# goes low will drive the status on the SO pin and CS# goes high will return the SO pin to tri-state.
- (3) To end the CP mode, either reaching the highest unprotected address or sending Write Disable (WRDI) command (04 hex) may achieve it and then it is recommended to send RDSR command (05 hex) to verify if CP mode is ended.

Figure 23-1. Enter Parallel Mode (ENPLM) Sequence (Command 55)**Figure 23-2. Exit Parallel Mode (EXPLM) Sequence (Command 45)****Figure 23-3. Parallel Mode Read Identification (Parallel RDID) Sequence (Command 9F)****Notes :**

1. There are 3 data bytes which would be output sequentially for Manufacturer and Device ID 1'st byte (Memory Type) and Device ID 2'nd byte (Memory Density).

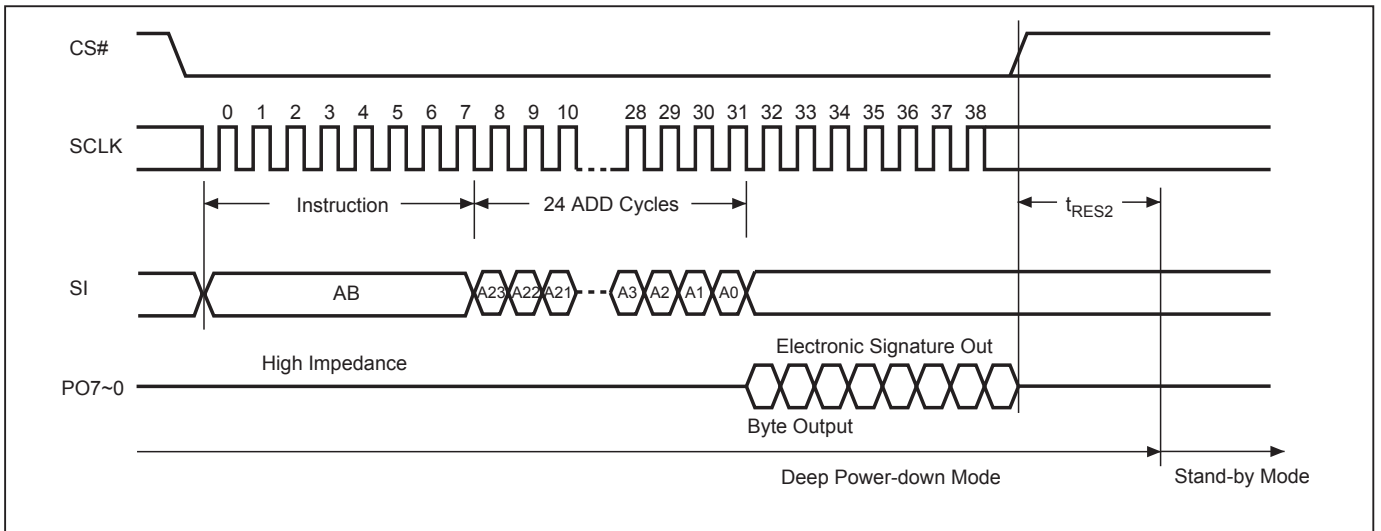
Figure 23-4. Parallel Mode Read Electronic Manufacturer & Device ID (Parallel REMS) Sequence (Command 90)



Notes :

1. A0=0 will output the Manufacturer ID first and A0=1 will output Device ID first. A1~A23 don't care.

Figure 23-5. Parallel Mode Release from Deep Power-down (RDP) and Read Electronic Signature (RES) Sequence



Notes :

1. Under parallel mode, the fastest access clock freq. will be changed to 6MHz(SCLK pin clock freq.)
To release from Deep Power-down mode and read ID in parallel mode, which requires a parallel mode command (55h) before the read status register command.
To exit parallel mode, it requires a (45h) command or power-off/on sequence.

Figure 23-6. Parallel Mode Read Array (Parallel READ) Sequence (Command 03)

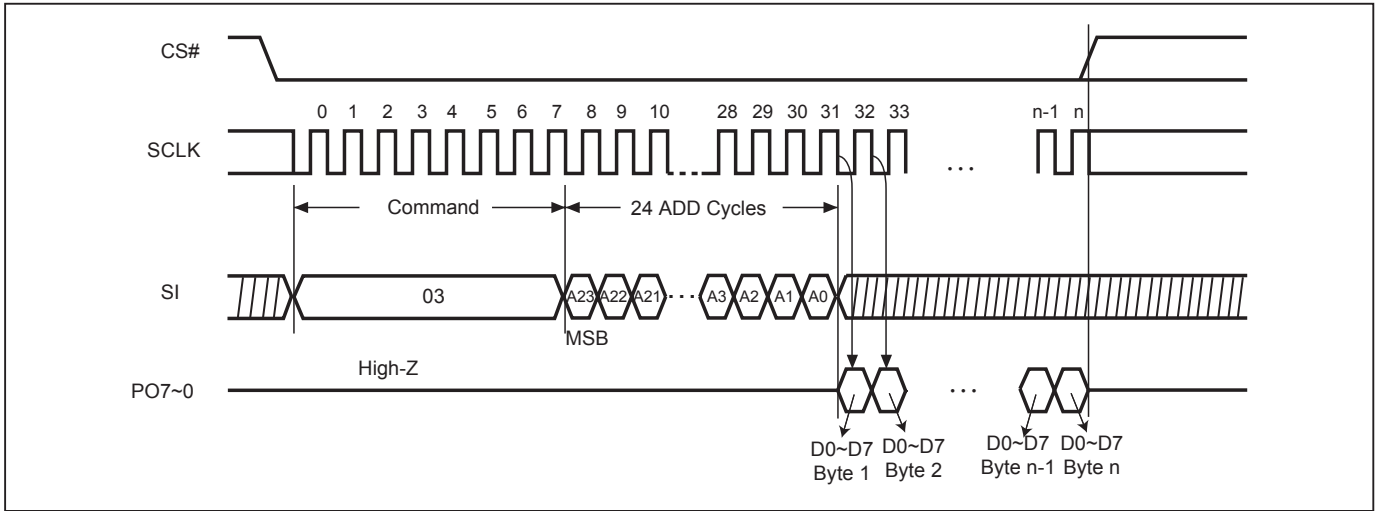


Figure 23-7. Parallel Mode Page Program (Parallel PP) Sequence (Command 02)

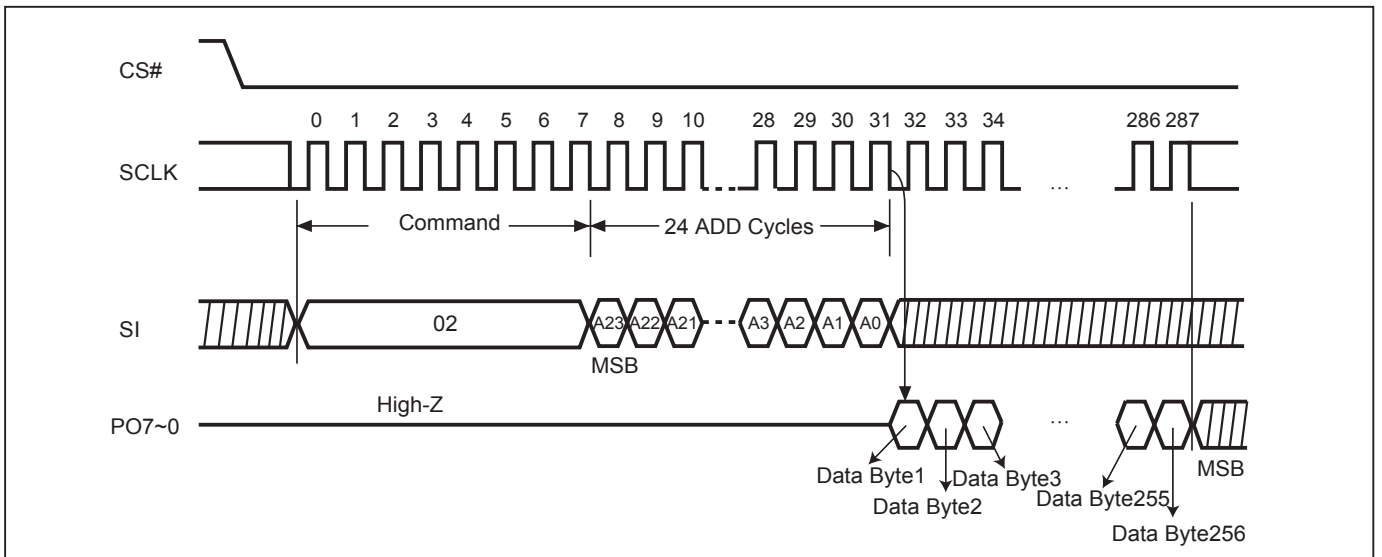


Figure 24. Deep Power-down (DP) Sequence (Command B9)

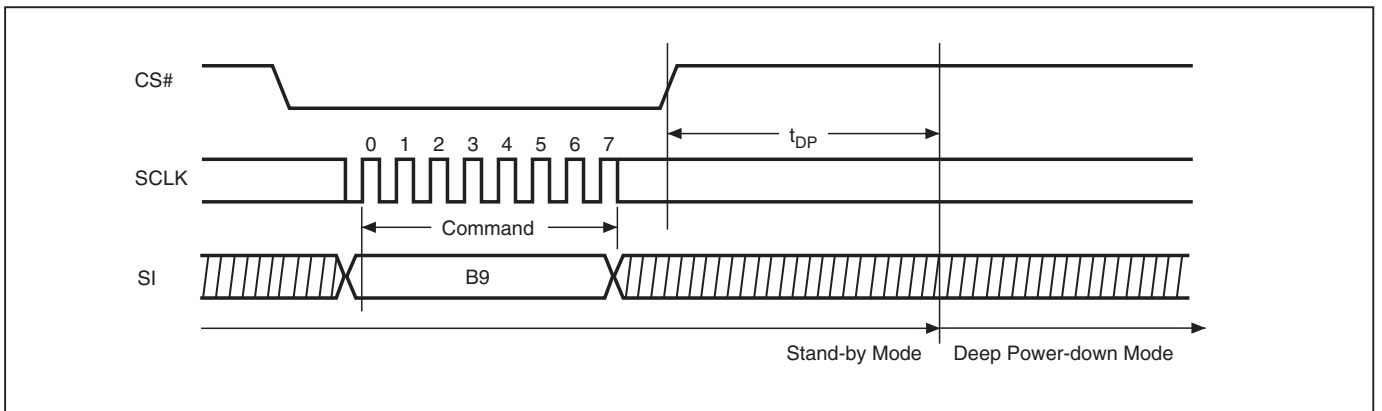


Figure 25. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

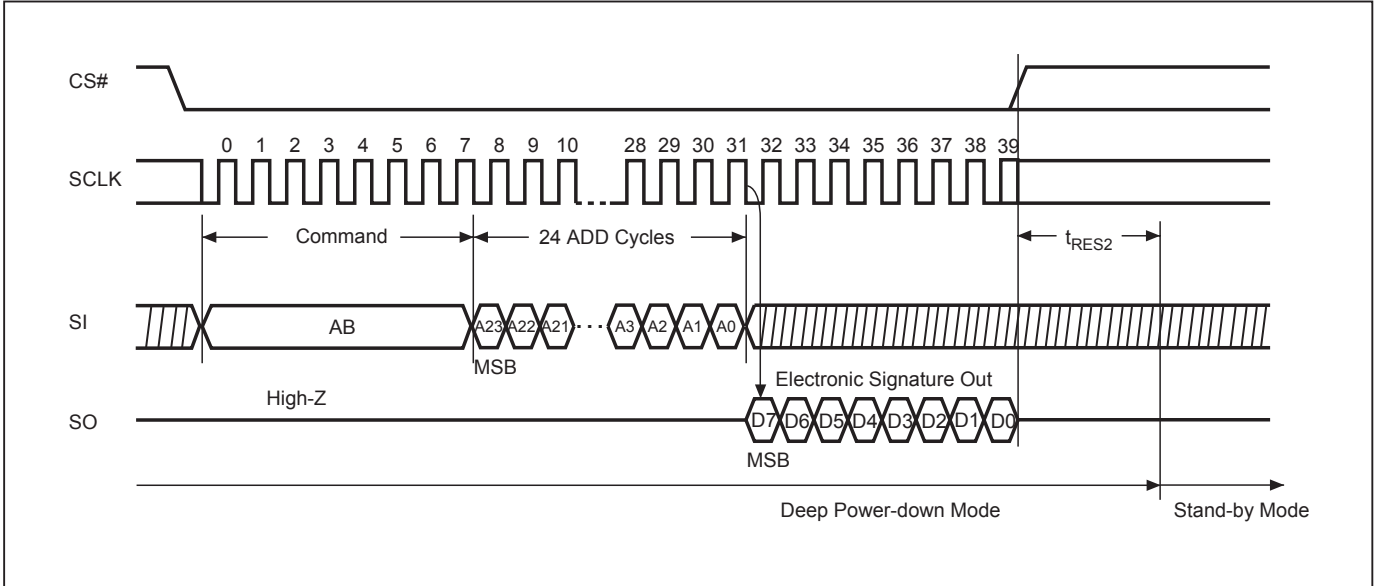


Figure 26. Release from Deep Power-down (RDP) Sequence (Command AB)

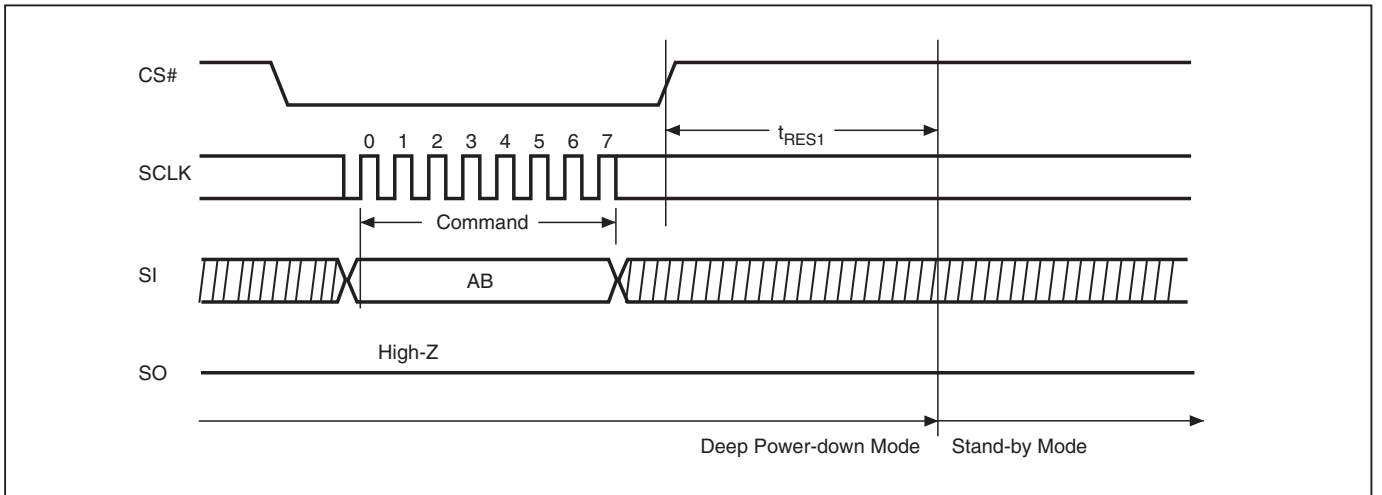
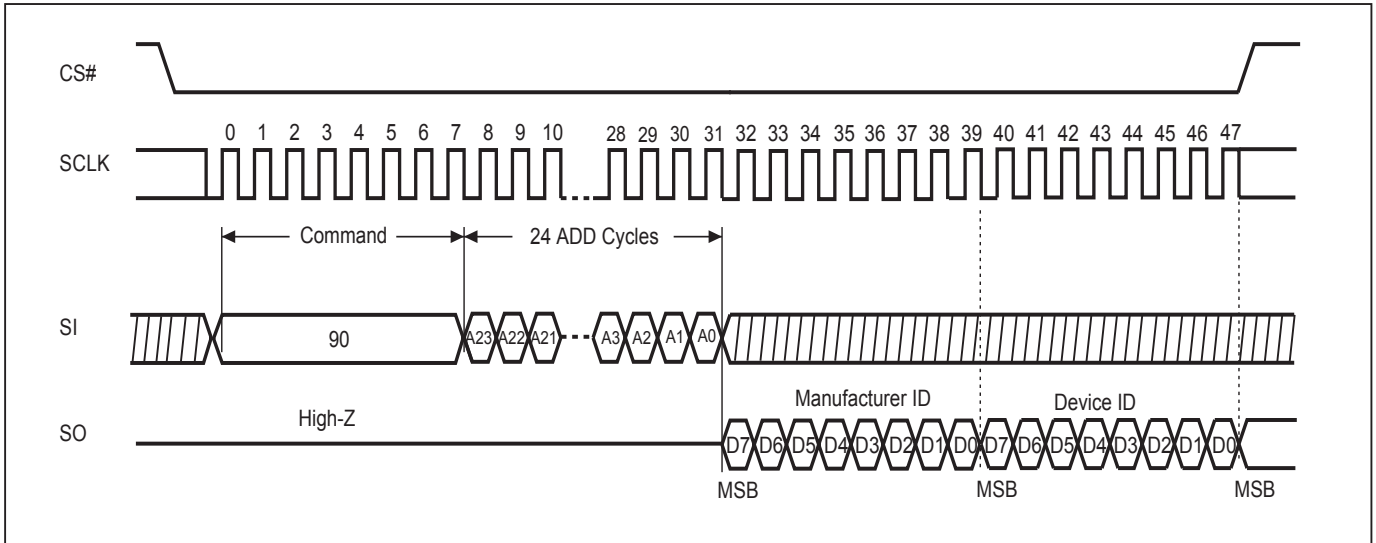


Figure 27. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90 or EF or DF or CF)



Notes:

1. A0=0 will output the Manufacturer ID first and A0=1 will output Device ID first. A1~A23 is don't care.
2. Instruction is either 90(hex) or EF(hex) or DF(hex) or CF(hex).

Figure 28. Write Protection Selection (WPSEL) Sequence (Command 68)

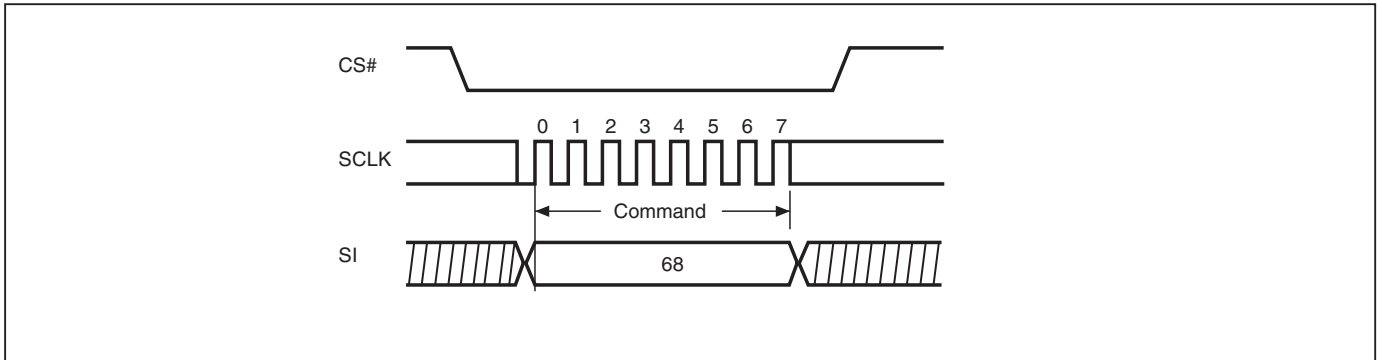


Figure 29. Single Block Lock/Unlock Protection (SBLK/SBULK) Sequence (Command 36/39)

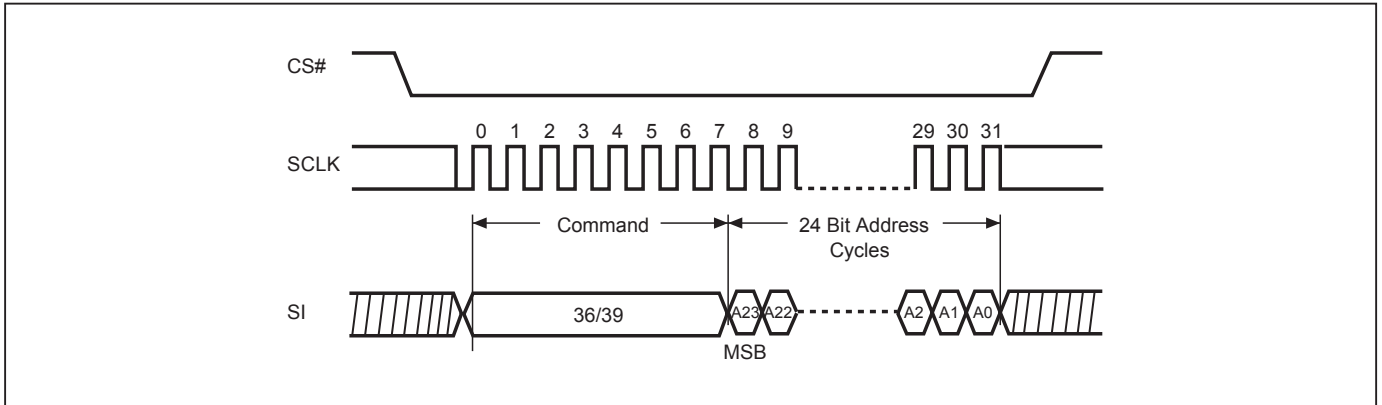


Figure 30. Read Block Protection Lock Status (RDBLOCK) Sequence (Command 3C)

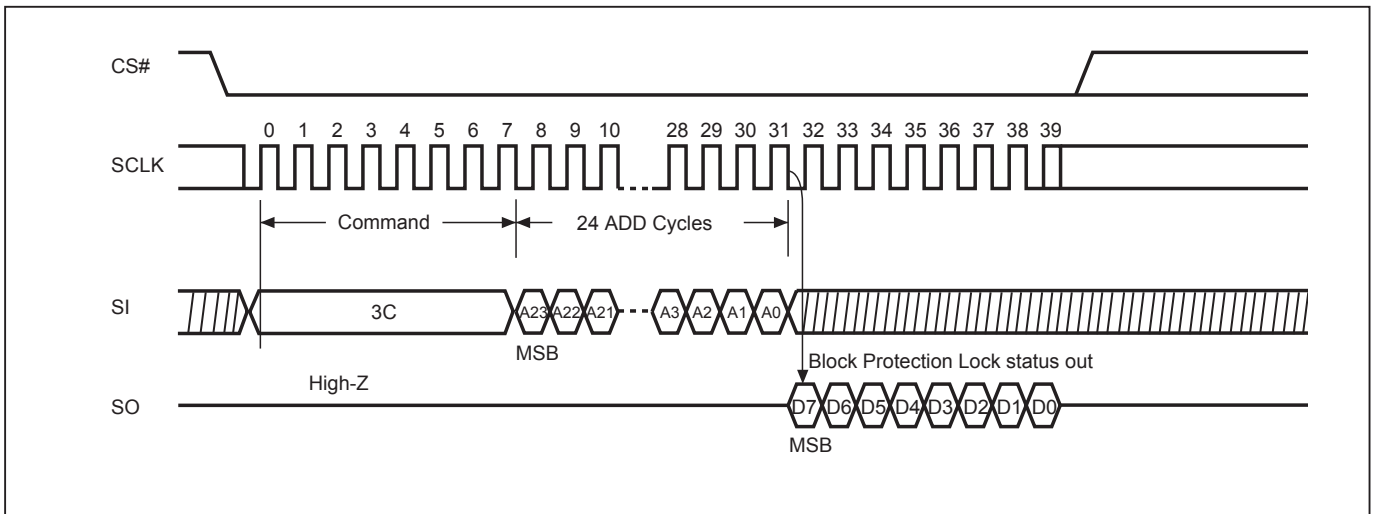


Figure 31. Gang Block Lock/Unlock (GBLK/GBULK) Sequence (Command 7E/98)

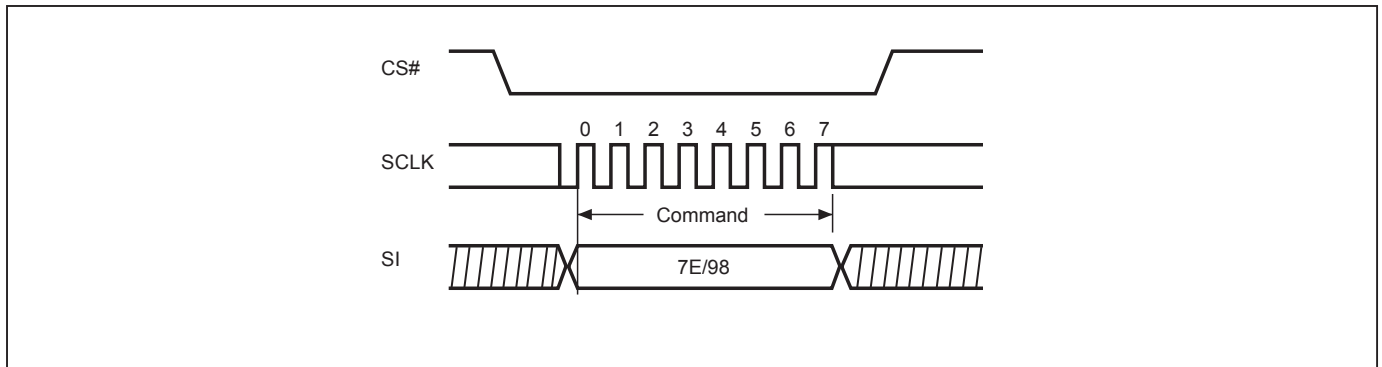
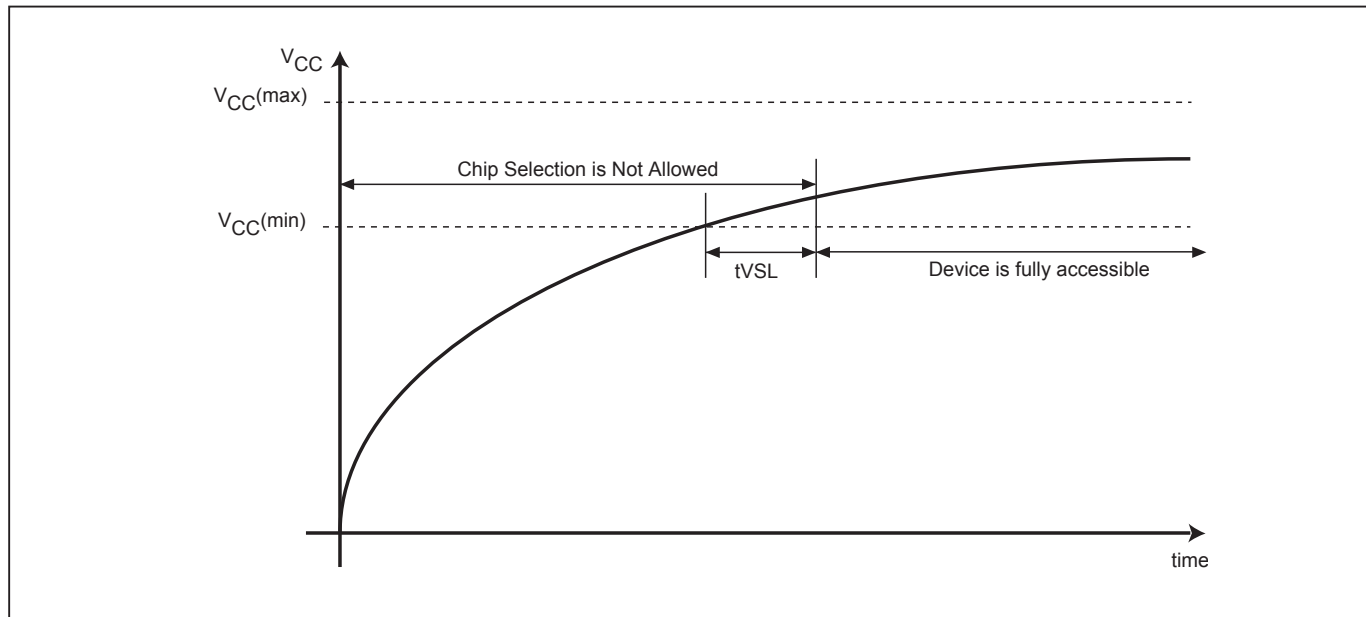


Figure 32. Power-up Timing

Note: VCC (max.) is 3.6V and VCC (min.) is 2.7V.

Table 9. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	300		us

Note: 1. The parameter is characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

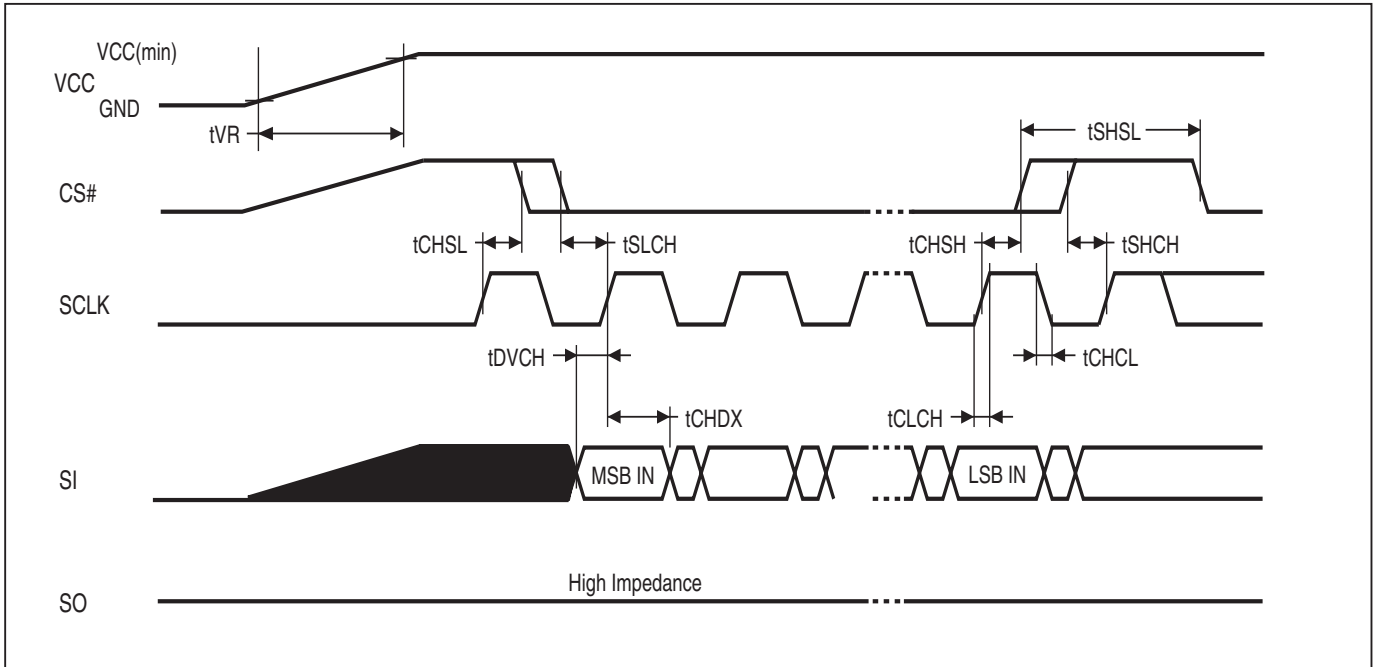


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	TYP. (1)	Max. (2)	UNIT	
Write Status Register Cycle Time	40	100	ms	
Sector Erase Time (4KB)	60	300	ms	
Block Erase Time (64KB)	0.7	2	s	
Block Erase Time (32KB)	0.5	2	s	
Chip Erase Time	64Mb	50	80	s
	128Mb	80	200	s
Byte Program Time (via page program command)	9	300	us	
Page Program Time	1.4	5	ms	
Erase/Program Cycle	100,000		cycles	

Note:

1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0°C, VCC=3.0V, and 100K cycle with 90% confidence level.

DATA RETENTION

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55°C	20		years

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		



ORDERING INFORMATION

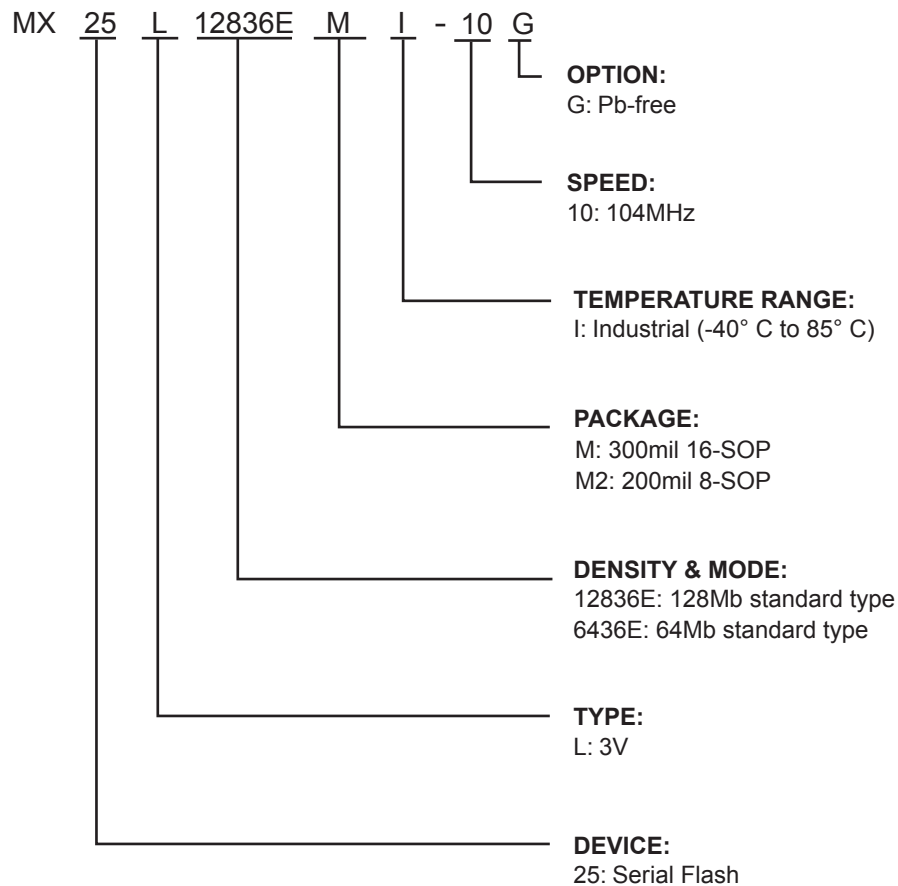
64Mb

PART NO.	CLOCK (MHz)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (uA)	TEMPERATURE	PACKAGE	Remark
MX25L6436EM2I-10G	104	45	100	-40°C~85°C	8-SOP (200mil)	Pb-free

128Mb

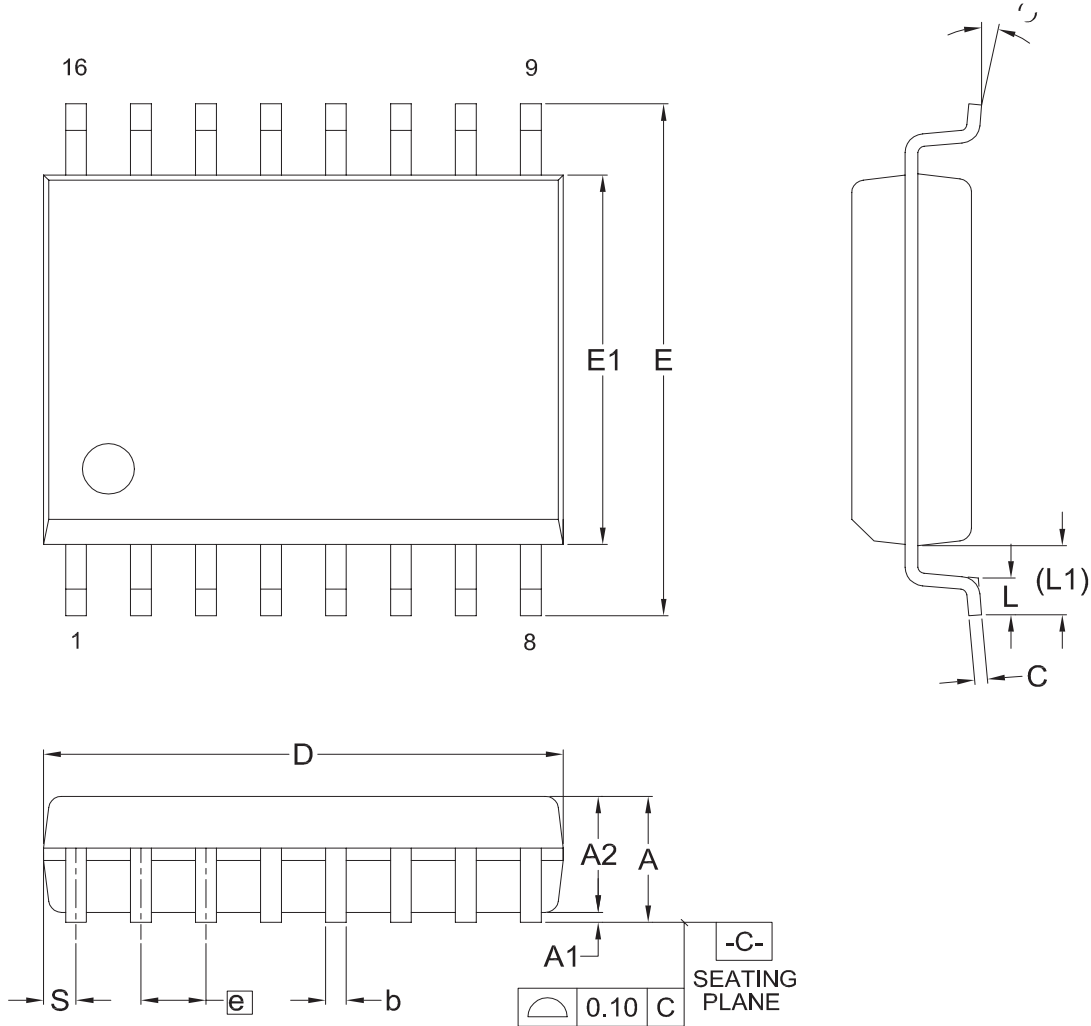
PART NO.	CLOCK (MHz)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (uA)	TEMPERATURE	PACKAGE	Remark
MX25L12836EMI-10G	104	45	100	-40°C~85°C	16-SOP (300mil)	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Doc. Title: Package Outline for SOP 16L (300MIL)

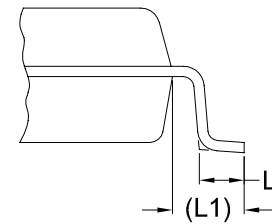
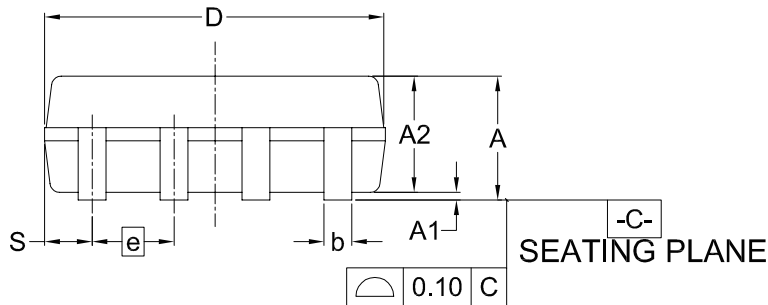
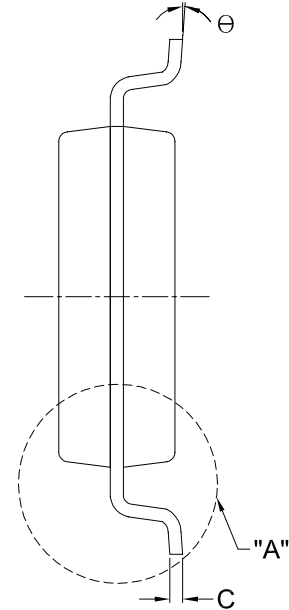
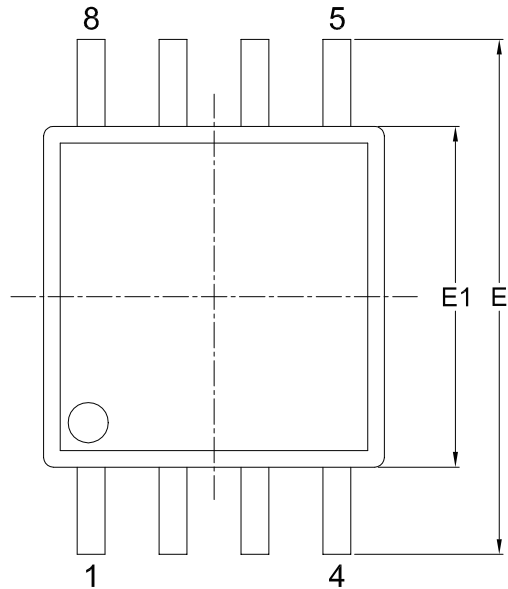


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	2.34	0.36	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0
	Nom.	---	0.20	2.39	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5
	Max.	2.65	0.30	2.44	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8
Inch	Min.	---	0.004	0.092	0.014	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0
	Nom.	---	0.008	0.094	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8

Dwg. No.	Revision	Reference		
		JEDEC	EIAJ	
6110-1402	9	MS-013		

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)



DETAIL "A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
UNIT														
mm	Min.	---	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0
	Nom.	---	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8
Inch	Min.	---	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0
	Nom.	---	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1406	2				



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