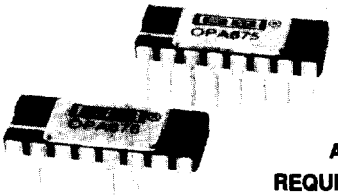
BURR-BROWN®

MILITARY
VERSION
AVAILABLE



OPA675
OPA676

ABRIDGED DATA SHEET
REQUEST COMPLETE DATA SHEET
FROM BURR-BROWN SALES OFFICE

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 185MHz (A_V = 10)
- LOW OFFSET VOLTAGE: ±250µV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 6ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

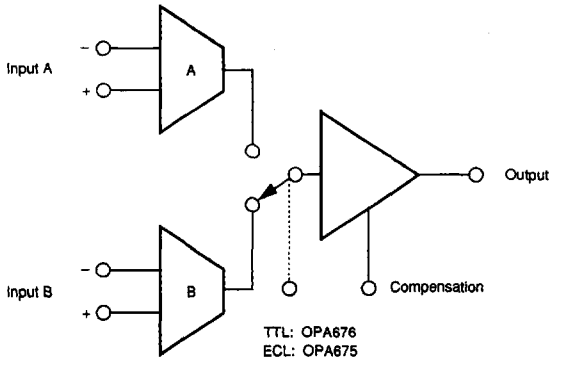
- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with differential ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op-amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (–55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-864

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	JG			SG			KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE[1]											
Voltage: f_O = 10Hz	R_S = 0Ω		27			*			*		nV/√Hz
f_O = 100 Hz			10			*			*		nV/√Hz
f_O = 1kHz			3.8			*			*		nV/√Hz
f_O = 10kHz			2.6			*			*		nV/√Hz
f_O = 100kHz			2.4			*			*		nV/√Hz
f_B = 10Hz to 10MHz			7.9			*			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±500	±2mV		*	*		±250	±1mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		*	*		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	65	86		*	*		70	*		dB
BIAS CURRENT[1]											
Input Bias Current	V_{CM} = 0VDC		23	35		*	*		*	30	µA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC		0.8	5		*	*		*	*	µA
INPUT IMPEDANCE[1]											
Differential			10^4 || 2			*			*		Ω || pF
Common-Mode			10^8 || 5			*			*		Ω || pF
INPUT VOLTAGE RANGE[1]											
Common-Mode Input Range		±2.1	±2.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC	75	100		*	*		85	*		dB
OPEN LOOP GAIN, DC[1]											
Open-Loop Voltage Gain		65	70		*	*		*	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth	Gain = +2V/V		100			*			*		MHz
	Gain = +5V/V		145			*			*		MHz
	Gain = +10V/V		185			*			*		MHz
	Gain = +50V/V		60			*			*		MHz
Crosstalk	Gain = +10V/V, f = 100kHz		–100			*			*		dBC[2]
	f = 1MHz		–80			*			*		dBC
	f = 10MHz		–68			*			*		dBC
	f = 100MHz		–35			*			*		dBC
Harmonic Distortion: 10MHz	G= +10V/V,R_L=50Ω,V_O=0.5Vp-p										
	second harmonic		–61			*			*		dBC
	third harmonic		–73			*			*		dBC
Full Power Response	V_O = 2.5Vp-p, Gain = +16V/V	25	44		*	*		30	*		MHz
Slew Rate	Gain = +16V/V	200	350		*	*		240	*		V/µs
Settling Time: 1%			9			*			*		ns
0.1%	Gain = +16 V/V		15			*			*		ns
0.01%	0.625V step		25			*			*		ns
INPUT SELECTION[3]											
Transition Time	ECL: OPA675		4			*			*		ns
50% In to 50% Out	TTL: OPA676		6			*			*		ns
DIGITAL INPUT											
TTL Logic Levels: V_{IL}	Logic "LO", I_{IL} = –6.4mA	0		+0.8	*		*	*		*	V
V_{IH}	Logic "HI", I_{IH} = 160µA	+2.0		+5	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = +0.8V		–0.05	–0.2		*	*		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.8V		1	20		*	*		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.15		–0.88	*		*	*		*	V
V_{IH}	Logic "HI"	–1.81		–1.475	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		0.05			*			*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		50			*			*		µA
RATED OUTPUT											
Voltage Output	R_L = 150Ω	±2.1	±2.6		*	*		*	*		V
	R_L = 50Ω	+1.25	+1.8		*	*		*	*		V
		–0.95	–1.1		*	*		–1.0	*		V
Current Output			±30			*			*		mA
Output Resistance	1MHz, Open Loop, C_C = 5pF		5			*			*		Ω
Load Capacitance Stability	Gain = +2V/V		50			*			*		pF
Short Circuit Current	Momentary	±30	±50		*	*		±30	*		mA

* Same specifications as for JG.

SPECIFICATIONS (Cont)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	JG			SG			KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage	$\pm V_{CC}$		5			*			*		VDC
Derated Performance	$\pm V_{CC}$	4.5		6.5	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		22	30		*	*		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient temp	0		+70	–55		+125	*		*	°C
Operating:	Ambient temp	–55		+125	*		*	*		*	°C
θ_{JA}			125			*			*		°C/W

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

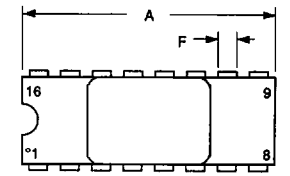
PARAMETER	CONDITIONS	JG			SG			KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification	Ambient temp	0		+70	–55		+125	*		*	°C
OFFSET VOLTAGE											
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		*	*		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	60	85		*	*		65	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		29	50		*	*		*	*	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.8	10		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.0	±2.3		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC	60	80		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain		60	68		*	*		63	69		dB
DIGITAL INPUT											
TTL Logic Levels: V_{IL}	Logic "LO", I_{IL} = –6.4mA	0		+0.8	*		*	*		*	V
V_{IH}	Logic "HI", I_{IH} = 160µA	+2.0		+5	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = +0.8V		–0.08	–0.4		*	*		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.8V		5	50		*	*		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.15		–0.88	*		*	*		*	V
V_{IH}	Logic "HI"	–1.81		–1.475	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		0.05			*			*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		50			*			*		µA
RATED OUTPUT											
Voltage Output	R_L = 150Ω	±2.0	±2.5		*	*		*	*		V
	R_L = 50Ω	+1.25	+1.6		*	*		*	*		V
		–0.8	–1.0		*	*		–0.9	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		25	35		*	*		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

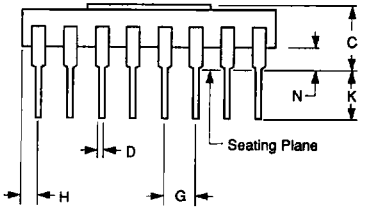
MECHANICAL

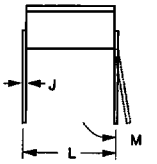
G Package— 16 Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	$\overline{CHA}$ (ECL)
5	Compensation Capacitor	12	$\overline{CHA}$ (ECL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	$\overline{DNC}$
5	Compensation Capacitor	12	$\overline{CHA}$ (TTL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation	1000mW
Differential Input Voltage	Total V_{cc}
Input Voltage Range	$\pm V_{cc}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

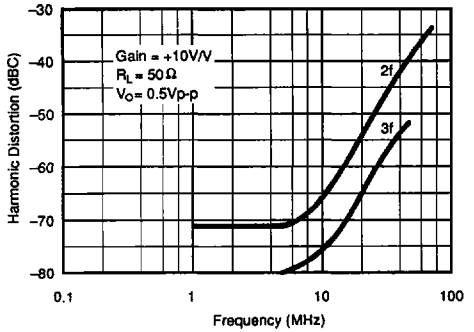
ORDERING INFORMATION

OPA675 ( ) ( ) Q
OPA676 ( ) ( ) Q

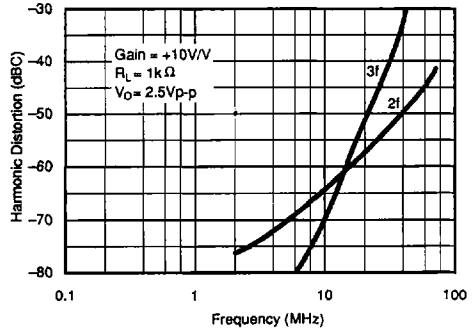
Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C
S: –55°C to +125°C
Package Code
G: 16-pin Ceramic DIP
Reliability Screening
Q: Q-Screened

TYPICAL PERFORMANCE CURVES

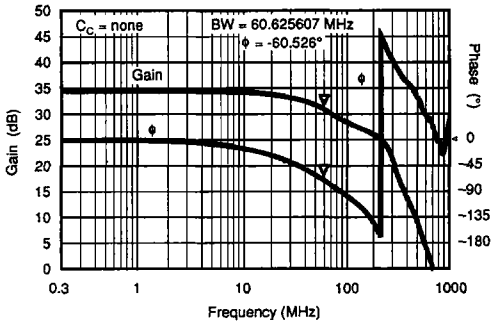
SMALL SIGNAL
HARMONIC DISTORTION vs FREQUENCY



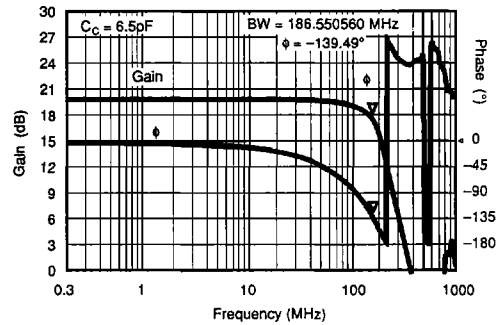
LARGE SIGNAL
HARMONIC DISTORTION vs FREQUENCY



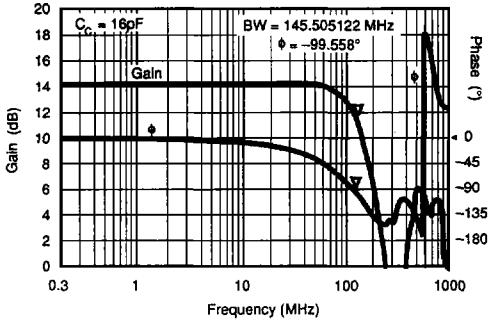
A_V = +50V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



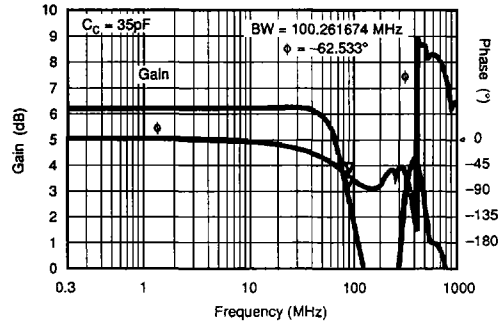
A_V = +10V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

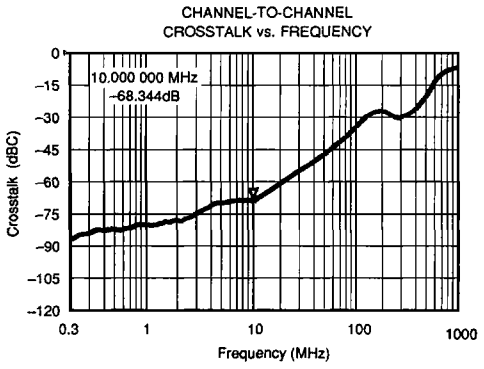


A_V = +5V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

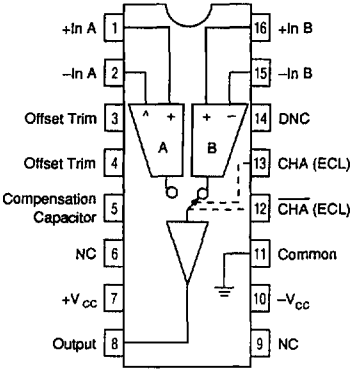


A_V = +2V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

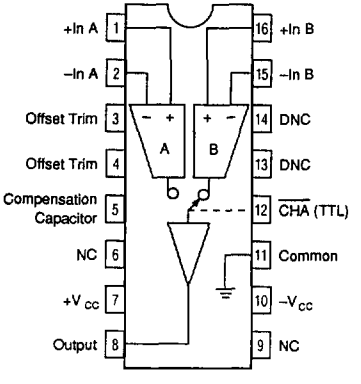


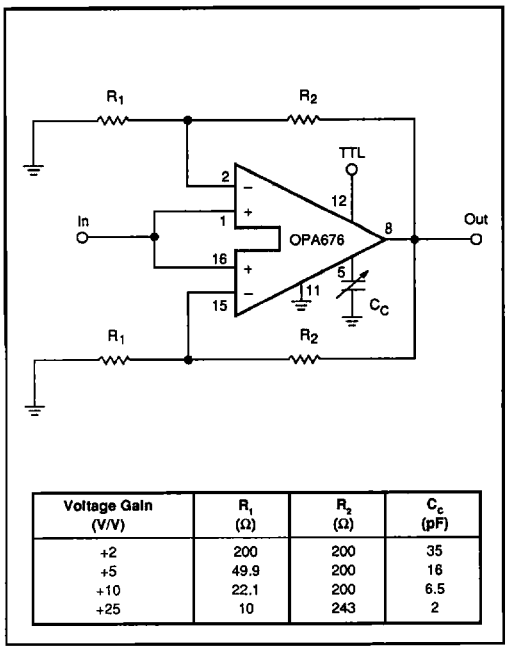


OPA675



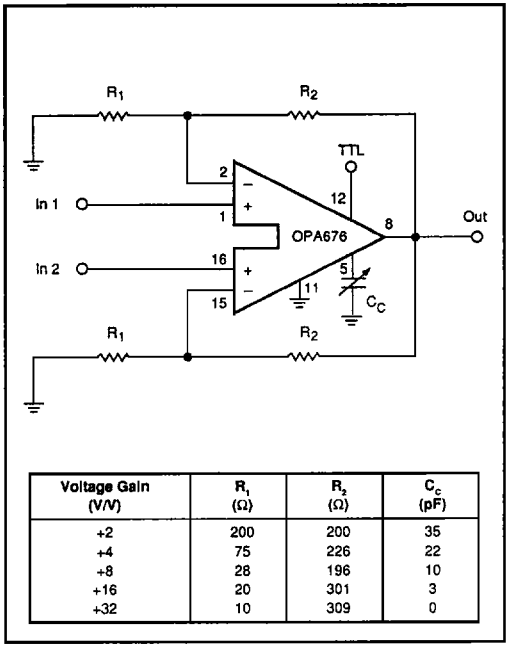
OPA676





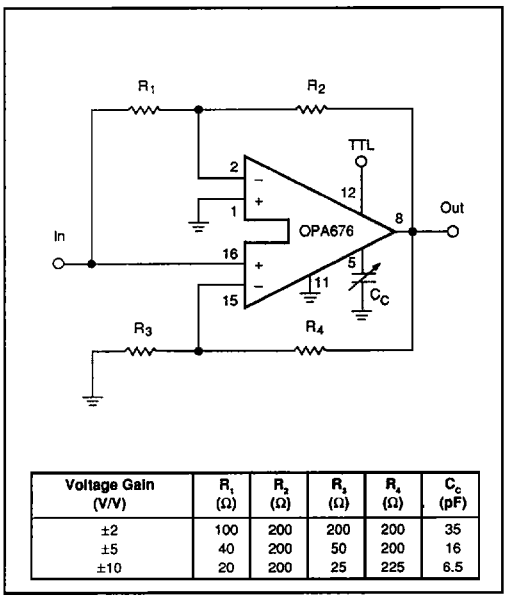
Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	C_C (pF)
+2	200	200	35
+5	49.9	200	16
+10	22.1	200	6.5
+25	10	243	2

FIGURE 1. Programmable-Gain Amplifier.



Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	C_C (pF)
+2	200	200	35
+4	75	226	22
+8	28	196	10
+16	20	301	3
+32	10	309	0

FIGURE 2. Two-Input Multiplexer (with gain).



Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	C_C (pF)
±2	100	200	200	200	35
±5	40	200	50	200	16
±10	20	200	25	225	6.5

FIGURE 3. Synchronous Modulator/Demodulator (with gain).

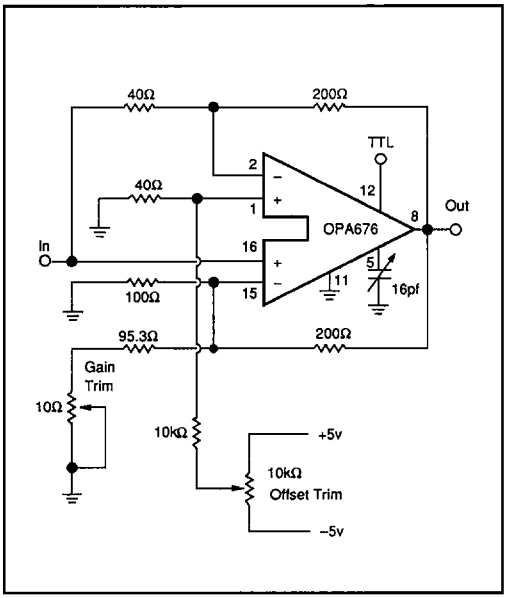


FIGURE 4. Synchronous Modulator/Demodulator with Carrier Balance Trim (gain = ±5V/V).