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RTL8363SB-CG

LAYER 2 MANAGED 2+2-PORT 10/100/1000M SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211 Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8363SB IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2011/06/09	First release.

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1. General Description

The RTL8363SB-CG is an LQFP128, high-performance 2+2-port 10/100/1000M Ethernet switch. It features low-power integrated dual-port Gigabit PHYs that support 1000Base-T, 100Base-TX, and 10Base-T.

For specific applications, the RTL8363SB supports two extra interfaces that can be configured as GMII/RGMII/MII interfaces. The RTL8363SB integrates all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8363SB features superior memory management technology to efficiently utilize memory space. The RTL8363SB integrates a 2K-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the EEPROM Serial Management Interface (SMI), Media Independent Interface Management (MIIM), or SPI Interface. Each of the entries can be configured as a static entry. Normal entry aging time is between 200 and 400 seconds. Eight Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The Extension GMAC0 and Extension GMAC1 of the RTL8363SB implement dual GMII/RGMII/MII interfaces. These interfaces could be connected to an external PHY, MAC, CPU, or RISC for specific applications. In router applications, the RTL8363SB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. When using this function, VID information carried in the VLAN tag will be changed to PVID.

Note: The RTL8363SB Extra Interface (Extension GMAC0 and Extension GMAC1) supports:

Dual-Port Gigabit Media Independent Interface (GMII)

Dual-Port Reduced Gigabit Media Independent Interface (RGMII)

Dual-Port Media Independent Interface (MII)

The RTL8363SB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8363SB supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast applications, the RTL8363SB supports IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping.

In order to support flexible traffic classification, the RTL8363SB supports 64-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

In Bridge operation the RTL8363SB supports 16 sets of port configurations: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol. To meet security and management application requirements, the RTL8363SB supports IEEE 802.1x Port-based/MAC-based Access Control. For those ports that do not pass IEEE 802.1x authentication, the RTL8363SB provides a

Port-based/MAC-based Guest VLAN function for them to access limited network resources. A 1-set Port Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time and multimedia networking applications, the RTL8363SB supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or mixed.

The RTL8363SB provides a 4K-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8363SB supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or EEPROM SMI Slave after reset.

In router applications, the router may want to know the input port of the incoming packet. The RTL8363SB supports an option to insert a VLAN tag with VID=Port VID (PVID) on each egress port. The RTL8363SB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, the RTL8363SB will drop all non-tagged packets and packets with an incorrect PVID.

2. Features

- Single-chip 2+2-port gigabit non-blocking switch architecture
  - Embedded Dual-port 10/100/1000Base-T PHY
  - Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Extra Interface (Extension GMAC0 and Extension GMAC1) supports
  - Dual-port Media Independent Interface (MII)
  - Dual-port Reduced Gigabit Media Independent Interface (RGMII)
  - Dual-port Gigabit Media Independent Interface (GMII)
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Supports Realtek Cable Test (RTCT)
- Supports 64-entry ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions include mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment GPIO control, interrupt and logging counter
  - Supports 5 types of user defined ACL rule format for 64 ACL rules
  - Optional per-port enable/disable of ACL function
  - Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
  - Supports 4K VLANs and 32 Extra Enhanced VLANs
  - Supports Un-tag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
  - Supports 2K-entry MAC address table with 4-way hash algorithm
  - Up to 2K L2/L3 Filtering Database
  - Per-port MAC learning limitation
- Supports Spanning Tree port behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Supports Auto Denial-of-Service Protection
- Supports H/W IGMP/MLD Snooping
  - IGMPv1/v2/3 and MLD v1/v2
  - Supports Fast Leave

- Static router port configuration
- Dynamic router port learning and aging

- Supports Quality of Service (QoS)
  - Supports per-port Input Bandwidth Control
  - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority and SVLAN based priority
  - Eight Priority Queues per port
  - Per queue flow control
  - Min-Max Scheduling
  - Strict Priority and Weighted Fair Queue (WFQ) to provide minimum bandwidth
  - One leaky bucket to constrain the average packet rate of each queue
- Supports rate limiting (64 shared meters, with 8kpbs granulation)
- RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
- Supports Stacking VLAN and Port Isolation with 8 Enhanced Filtering Databases
- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLANs
  - Supports 32 L2/IPv4 Multicast mappings to SVLAN
  - Supports MAC-based 1:N VLAN
- Supports 2 IEEE 802.3ad Link aggregation port groups
- Supports Port Mirror function for one source port to multiple destination ports
- Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
- Supports Loop Detection
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports Realtek Green Ethernet
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving
- Supports 1 interrupt output to external CPU for notification
- Each port supports 3 LED outputs
- Management Interface Supports
  - EEPROM SMI Slave interface
  - Media Independent Interface Management (MIIM)
  - SPI Slave Interface
- Supports 32K-byte EEPROM space for configuration
- Integrated 8051 microprocessor.
- 25MHz crystal or 3.3V OSC input
- LQFP 128-pin package

3. System Applications

- 2-Port 1000Base-T Router with Dual MII/RGMII/GMII Interfaces

4. Application Examples

4.1. 2-Port 1000Base-T Router with Dual MII/RGMII/GMII

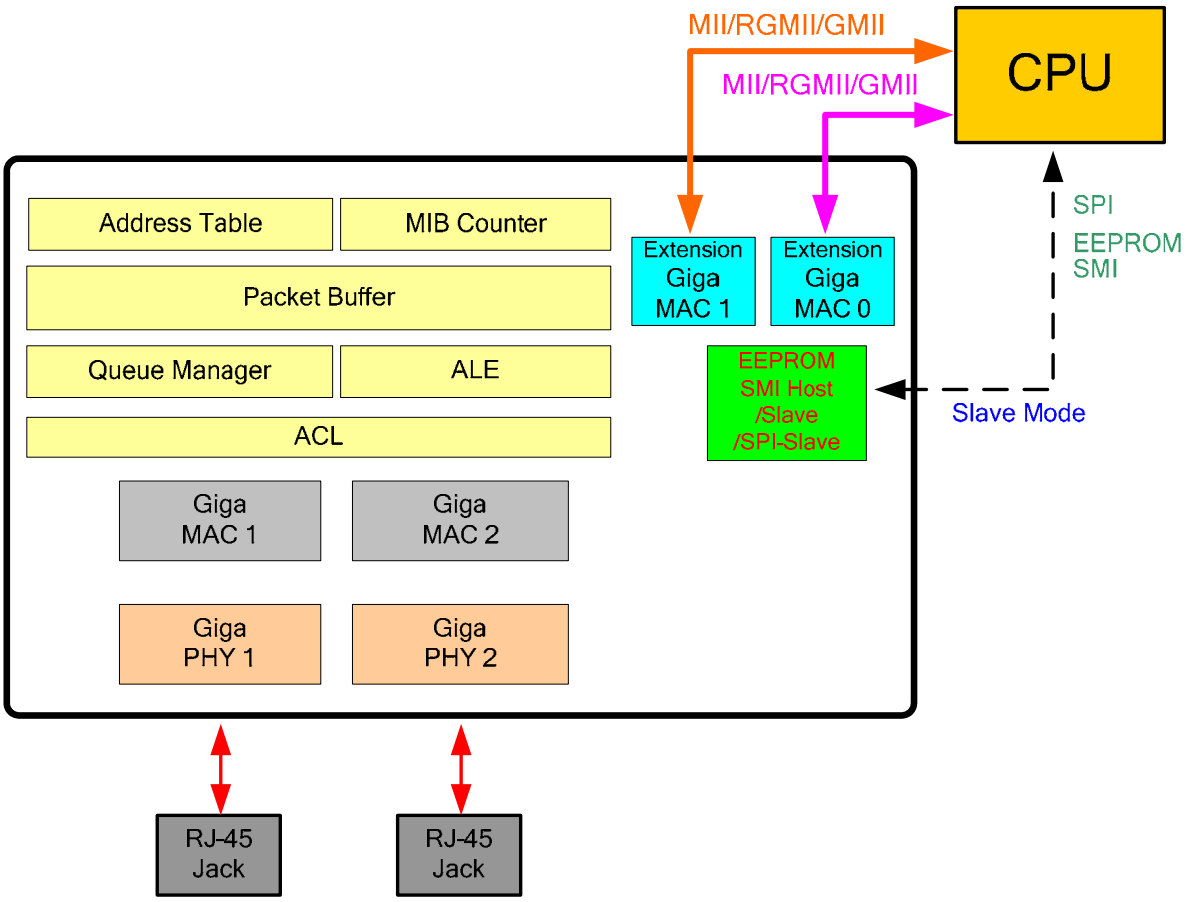


Figure 1. 2-Port 1000Base-T Router with Dual MII/RGMII/GMII

Note: Extra Interface (Extension GMAC0 and Extension GMAC1) in MII/RGMII/GMII Mode.

5. Block Diagram

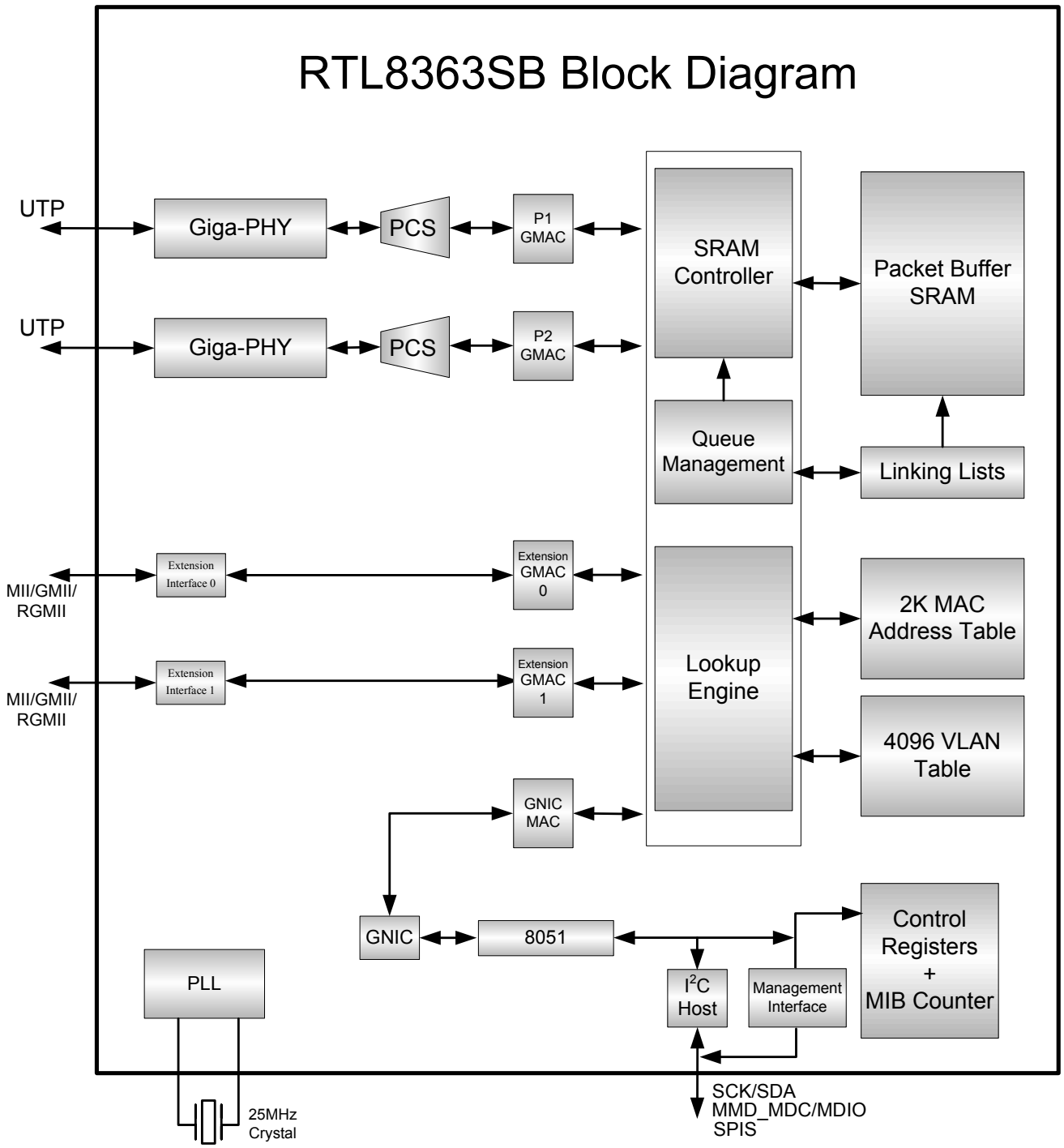
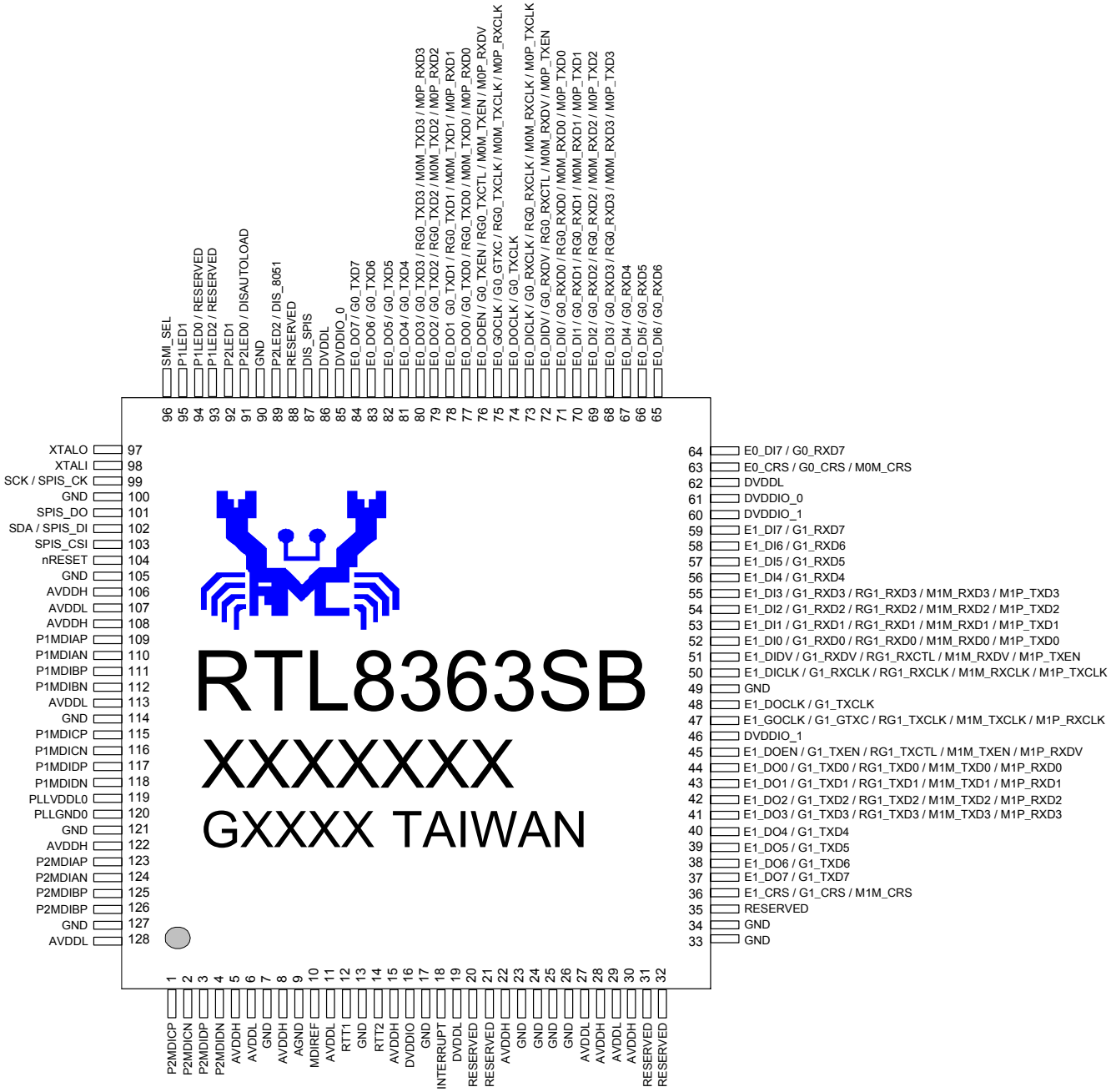


Figure 2. Block Diagram

6. Pin Assignments



LQFP 128 Package Size 14mm x 14mm

Figure 3. Pin Assignments (LQFP-128)

6.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 3).

6.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

I_S: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Assignment Table

Name	Pin No.	Type
P2MDICP	1	AI/O
P2MDICN	2	AI/O
P2MDIDP	3	AI/O
P2MDIDN	4	AI/O
AVDDH	5	AP
AVDDL	6	AP
GND	7	G
AVDDH	8	AP
AGND	9	AG
MDIREF	10	AO
AVDDL	11	AP
RTT1	12	AO
GND	13	G
RTT2	14	AO
AVDDH	15	AP
DVDDIO	16	P
GND	17	G
INTERRUPT	18	O_{PU}
DVDDL	19	P
RESERVED	20	I
RESERVED	21	I
AVDDH	22	AP

Name	Pin No.	Type
GND	23	G
GND	24	G
GND	25	G
GND	26	G
AVDDL	27	AP
AVDDH	28	AP
AVDDL	29	AP
AVDDH	30	AP
RESERVED	31	AO
RESERVED	32	AO
GND	33	G
GND	34	G
RESERVED	35	I
E1_CRS/G1_CRS/M1M_CRS	36	I
E1_DO7/G1_TXD7	37	O
E1_DO6/G1_TXD6	38	O
E1_DO5/G1_TXD5	39	O
E1_DO4/G1_TXD4	40	O
E1_DO3/G1_TXD3/RG1_TXD3/ M1M_TXD3/M1P_RXD3	41	O
E1_DO2/G1_TXD2/RG1_TXD2/ M1M_TXD2/M1P_RXD2	42	O

Name	Pin No.	Type
E1_DO1/G1_TXD1/RG1_TXD1/ M1M_TXD1/M1P_RXD1	43	O
E1_DO0/G1_TXD0/RG1_TXD0/ M1M_TXD0/M1P_RXD0	44	O
E1_DOEN/G1_TXEN/ RG1_TXCTL/M1M_TXEN/ M1P_RXDV	45	O
DVDDIO_1	46	P
E1_GOCLK/G1_GTXC/ RG1_TXCLK/M1M_TXCLK/ M1P_RXCLK	47	I/O
E1_DOCLK /G1_TXCLK	48	I
GND	49	G
E1_DICLK/G1_RXCLK/ RG1_RXCLK/M1M_RXCLK/ M1P_TXCLK	50	I/O
E1_DIDV/G1_RXDV/ RG1_RXCTL/M1M_RXDV/ M1P_TXEN	51	I
E1_DI0/G1_RXD0/RG1_RXD0/ M1M_RXD0/M1P_TXD0	52	I
E1_DI1/G1_RXD1/RG1_RXD1/ M1M_RXD1/M1P_TXD1	53	I
E1_DI2/G1_RXD2/RG1_RXD2/ M1M_RXD2/M1P_TXD2	54	I
E1_DI3/G1_RXD3/RG1_RXD3/ M1M_RXD3/M1P_TXD3	55	I
E1_DI4/G1_RXD4	56	I
E1_DI5/G1_RXD5	57	I
E1_DI6/G1_RXD6	58	I
E1_DI7/G1_RXD7	59	I
DVDDIO_1	60	P
DVDDIO_0	61	P
DVDDL	62	P
E0_CRS/G0_CRS/M0M_CRS	63	I
E0_DI7/G0_RXD7	64	I
E0_DI6/G0_RXD6	65	I
E0_DI5/G0_RXD5	66	I
E0_DI4/G0_RXD4	67	I
E0_DI3/G0_RXD3/RG0_RXD3/ M0M_RXD3/M0P_TXD3	68	I
E0_DI2/G0_RXD2/RG0_RXD2/ M0M_RXD2/M0P_TXD2	69	I
E0_DI1/G0_RXD1/RG0_RXD1/ M0M_RXD1/M0P_TXD1	70	I
E0_DI0/G0_RXD0/RG0_RXD0/ M0M_RXD0/M0P_TXD0	71	I

Name	Pin No.	Type
E0_DIDV/G0_RXDV/ RG0_RXCTL/M0M_RXDV/ M0P_TXEN	72	I
E0_DICLK/G0_RXCLK/ RG0_RXCLK/M0M_RXCLK/ M0P_TXCLK	73	I/O
E0_DOCLK/G0_TXCLK	74	I
E0_GOCLK/G0_GTXC/ RG0_TXCLK/M0M_TXCLK/ M0P_RXCLK	75	I/O
E0_DOEN/G0_TXEN/ RG0_TXCTL/M0M_TXEN/ M0P_RXDV	76	O
E0_DO0/G0_TXD0/RG0_TXD0/ M0M_TXD0/M0P_RXD0	77	O
E0_DO1/G0_TXD1/RG0_TXD1/ M0M_TXD1/M0P_RXD1	78	O
E0_DO2/G0_TXD2/RG0_TXD2/ M0M_TXD2/M0P_RXD2	79	O
E0_DO3/G0_TXD3/RG0_TXD3/ M0M_TXD3/M0P_RXD3	80	O
E0_DO4/G0_TXD4	81	O
E0_DO5/G0_TXD5	82	O
E0_DO6/G0_TXD6	83	O
E0_DO7/G0_TXD7	84	O
DVDDIO_0	85	P
DVDDL	86	P
DIS_SPIS	87	I/O_{PU}
RESERVED	88	I/O_{PU}
P2LED2/DIS_8051	89	I/O_{PU}
GND	90	G
P2LED0/DISAUTOLOAD	91	I/O_{PU}
P2LED1/GPIO12	92	I/O_{PU}
P1LED2/RESERVED	93	I/O_{PU}
P1LED0/RESERVED	94	I/O_{PU}
P1LED1	95	I/O_{PU}
LED_CK/SMI_SEL	96	I/O_{PU}
XTALO	97	AO
XTALI	98	AI
SPIS_CK/SCK/MMD_MDC	99	I/O_{PU}
GND	100	G
SPIS_DO	101	O
SPIS_DI /SDA/MMD_MDIO	102	I/O_{PU}
SPIS_CSI	103	I
nRESET	104	I_S
GND	105	G

Name	Pin No.	Type
AVDDH	106	AP
AVDDL	107	AP
AVDDH	108	AP
P1MDIAP	109	AI/O
P1MDIAN	110	AI/O
P1MDIBP	111	AI/O
P1MDIBN	112	AI/O
AVDDL	113	AP
GND	114	G
P1MDICP	115	AI/O
P1MDICN	116	AI/O
P1MDIDP	117	AI/O

Name	Pin No.	Type
P1MDIDN	118	AI/O
PLLVDDL0	119	AP
PLLGND0	120	AG
GND	121	G
AVDDH	122	AP
P2MDIAP	123	AI/O
P2MDIAN	124	AI/O
P2MDIBP	125	AI/O
P2MDIBN	126	AI/O
GND	127	G
AVDDL	128	AP

7. Pin Descriptions

7.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	109 110 111 112 115 116 117 118	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	123 124 125 126 1 2 3 4	AI/O	10	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

7.2. General Purpose Interfaces

The RTL8363SB supports multi-function General Purpose Interfaces that can be configured as MII/RGMII/GMII mode for extension GMAC interfaces. The RTL8363SB supports two extension interfaces (Extension GMAC0 and Extension GMAC1) for connecting with an external PHY, MAC, or CPU in specific applications. These extension interfaces support GMII, RGMII, MII MAC mode, or MII PHY mode via register configuration.

7.2.1. GMII Interface Pins

The Extension GMAC0 and Extension GMAC1 of the RTL8363SB support two GMII interfaces when register configuration is set to GMII mode interface. When the extension interface operates at 1Gbps, the interface will be GMII. When the extension interfaces operate at 100Mbps/10Mbps, the interface will be MII. Note that 1Gbps Half Duplex is not supported in this configuration.

Table 3. Extension GMAC0 GMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
G0_CRS	63	I	-	G0_CRS Carrier Sense Input when the Extension GMAC0 GMII interface operates in 10/100 MII half duplex mode. G0_CRS is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a valid carrier is detected on the media. This pin must be pulled low with a 1K ohm resistor when not used.
G0_RXD7 G0_RXD6 G0_RXD5 G0_RXD4 G0_RXD3 G0_RXD2 G0_RXD1 G0_RXD0	64 65 66 67 68 69 70 71	I	-	G0_RXD[7:0] Extension GMAC0 GMII Receive Data Input. Received data is received synchronously at the rising edge of G0_RXCLK. In 10/100Mbps MII mode, only G0_RXD[3:0] are available. These pins must be pulled low with a 1K ohm resistor when not used.
G0_RXDV	72	I	-	G0_RXDV Extension GMAC0 GMII Receive Data Valid Input. Receive Data Valid is received synchronously at the rising edge of G0_RXCLK in both 1Gbps GMII and 10/100Mbps MII MAC mode. This pin must be pulled low with a 1K ohm resistor when not used.
G0_RXCLK	73	I	-	G0_RXCLK Extension GMAC0 GMII Receive Clock Input. In GMII mode: 125MHz receive clock. Used to synchronize G0_RXD[7:0] and G0_RXDV. In MII 10/100Mbps mode: G0_RXCLK is 2.5/25MHz. Used to synchronize G0_RXD[3:0], G0_RXDV, and G0_CRS. This pin must be pulled low with a 1K ohm resistor when not used.
G0_TXCLK	74	I	-	G0_TXCLK 2.5/25MHz Transmit Clock Input when the Extension GMAC0 GMII interface operates in 10/100 MII mode. 2.5/25MHz clock driven by PHY when operating in 10/100Mbps MII mode. Used to synchronize G0_TX[3:0] and G0_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.
G0_GTXC	75	O	-	G0_GTXC Extension GMAC0 GMII Transmit Clock Output. 125MHz transmit clock output when GMII is operating at 1Gbps. Used to synchronize G0_TXD[7:0] and G0_TXEN.
G0_TXEN	76	O	-	G0_TXEN Extension GMAC0 GMII Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of G0_GTXC in GMII mode. Transmit enable that is sent synchronously at the rising edge of G0_TXCLK in 10/100Mbps MII mode.
G0_TXD0 G0_TXD1 G0_TXD2 G0_TXD3 G0_TXD4 G0_TXD5 G0_TXD6 G0_TXD7	77 78 79 80 81 82 83 84	O	-	G0_TXD [7:0] Extension GMAC0 GMII Transmit Data Output. In 1000Mbps GMII mode, G0_TXD [7:0] transmitted data is sent synchronously at the rising edge of G0_GTXC. In 10/100Mbps MII mode, only G0_TXCLK [3:0] are available for transmitting and receiving data at the rising edge of G0_TXCLK.

Table 4. Extension GMAC1 GMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
G1_CRS	36	I	-	G1_CRS Carrier Sense Input when the Extension GMAC1 GMII interface operates in 10/100 MII half duplex mode. G1_CRS is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a valid carrier is detected on the media. This pin must be pulled low with a 1K ohm resistor when not used.
G1_TXD7 G1_TXD6 G1_TXD5 G1_TXD4 G1_TXD3 G1_TXD2 G1_TXD1 G1_TXD0	37 38 39 40 41 42 43 44	O	-	G1_TXD [7:0] Extension GMAC1 GMII Transmit Data Output. In 1000Mbps GMII mode, G1_TXD [7:0] transmitted data is sent synchronously at the rising edge of G1_GTXC. In 10/100Mbps MII mode, only G1_TXCLK [3:0] are available for transmitting and receiving data at the rising edge of G1_TXCLK.
G1_TXEN	45	O	-	G1_TXEN Extension GMAC1 GMII Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of G1_GTXC in GMII mode. Transmit enable that is sent synchronously at the rising edge of G1_TXCLK in 10/100Mbps MII mode.
G1_GTXC	47	O	-	G1_GTXC Extension GMAC1 GMII Transmit Clock Output. 125MHz transmit clock output when GMII is operating at 1Gbps. Used to synchronize G1_TXD[7:0] and G1_TXEN.
G1_TXCLK	48	I	-	G1_TXCLK 2.5/25MHz Transmit Clock Input when the Extension GMAC1 GMII interface operates in 10/100 MII mode. 2.5/25MHz clock driven by PHY when operating in 10/100Mbps MII mode. Used to synchronize G1_TX[3:0] and G1_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.
G1_RXCLK	50	I	-	G1_RXCLK Extension GMAC1 GMII Receive Clock Input. In GMII mode: 125MHz receive clock. Used to synchronize G1_RXD[7:0], and G1_RXDV. In MII 10/100Mbps mode: G1_RXCLK is 2.5/25MHz. Used to synchronize G1_RXD[3:0], G1_RXDV, and G1_CRS. This pin must be pulled low with a 1K ohm resistor when not used.
G1_RXDV	51	I	-	G1_RXDV Extension GMAC1 GMII Receive Data Valid Input. Receive Data Valid is received synchronously at the rising edge of G1_RXCLK in both 1Gbps GMII and 10/100Mbps MII MAC mode. This pin must be pulled low with a 1K ohm resistor when not used.
G1_RXD0 G1_RXD1 G1_RXD2 G1_RXD3 G1_RXD4 G1_RXD5 G1_RXD6 G1_RXD7	52 53 54 55 56 57 58 59	I	-	G1_RXD[7:0] Extension GMAC1 GMII Receive Data Input. Received data is received synchronously at the rising edge of G1_RXCLK. In 10/100Mbps MII mode, only G1_RXD[3:0] are available. These pins must be pulled low with a 1K ohm resistor when not used.

7.2.2. RGMII Pins

The Extension GMAC0 and Extension GMAC1 of the RTL8363SB support two RGMII interfaces to connect with an external MAC or PHY device when register configuration is set to RGMII mode interface.

Table 5. Extension GMAC0 RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG0_RXD3 RG0_RXD2 RG0_RXD1 RG0_RXD0	68 69 70 71	I	-	RG0_RXD[3:0] Extension GMAC0 RGMII Receive Data Input. Received data is received synchronously by RG0_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.
RG0_RXCTL	72	I	-	RG0_RXCTL Extension GMAC0 RGMII Receive Control signal input. The RG0_RXCTL indicates RX_DV at the rising of RG0_RXCLK and RX_ER at the falling edge of RG0_RXCLK. At RG0_RXCLK falling edge, RG0_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG0_RXCLK	73	I	-	RG0_RXCLK Extension GMAC0 RGMII Receive Clock Input. RG0_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG0_RXD[3:0] and RG0_RXCTL synchronization at both RG0_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG0_TXCLK	75	O	-	RG0_TXCLK Extension GMAC0 RGMII Transmit Clock Output. RG0_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG0_TXD[3:0] and RG0_TXCTL synchronization at RG0_TXCLK on both rising and falling edges.
RG0_TXCTL	76	O	-	RG0_TXCTL Extension GMAC0 RGMII Transmit Control signal Output. The RG0_TXCTL indicates TX_EN at the rising edge of RG0_TXCLK, and TX_ER at the falling edge of RG0_TXCLK. At the RG0_TXCLK falling edge, RG0_TXCTL= TX_EN (XOR) TX_ER.
RG0_TXD0 RG0_TXD1 RG0_TXD2 RG0_TXD3	77 78 79 80	O	-	RG0_TXD[3:0] Extension GMAC0 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG0_TXCLK.

Table 6. Extension GMAC1 RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG1_TXD3 RG1_TXD2 RG1_TXD1 RG1_TXD0	41 42 43 44	O	-	RG1_TXD[3:0] Extension GMAC1 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG1_TXCLK.
RG1_TXCTL	45	O	-	RG1_TXCTL Extension GMAC1 RGMII Transmit Control signal Output. The RG1_TXCTL indicates TX_EN at the rising edge of RG1_TXCLK, and TX_ER at the falling edge of RG1_TXCLK. At the RG1_TXCLK falling edge, RG1_TXCTL= TX_EN (XOR) TX_ER.
RG1_TXCLK	47	O	-	RG1_TXCLK Extension GMAC1 RGMII Transmit Clock Output. RG1_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_TXD[3:0] and RG1_TXCTL synchronization at RG1_TXCLK on both rising and falling edges.
RG1_RXCLK	50	I	-	RG1_RXCLK Extension GMAC1 RGMII Receive Clock Input. RG1_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_RXD[3:0] and RG1_RXCTL synchronization at both RG1_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXCTL	51	I	-	RG1_RXCTL Extension GMAC1 RGMII Receive Control signal input. The RG1_RXCTL indicates RX_DV at the rising of RG1_RXCLK and RX_ER at the falling edge of RG1_RXCLK. At RG1_RXCLK falling edge, RG1_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXD0 RG1_RXD1 RG1_RXD2 RG1_RXD3	52 53 54 55	I	-	RG1_RXD[3:0] Extension GMAC1 RGMII Receive Data Input. Received data is received synchronously by RG1_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

7.2.3. MII Pins

The Extension GMAC0 and Extension GMAC1 of the RTL8363SB support two MII interfaces to connect with an external MAC or PHY device when register configuration is set to MII mode interface. These two MII interfaces also can be configured as MII MAC mode or MII PHY mode by register.

Table 7. Extension GMAC0 MII Pins (MII MAC Mode or MII PHY Mode)

Pin Name	Pin No.	Type	Drive (mA)	Description
M0M_CRS	63	I	-	M0M_CRS Extension GMAC0 MII MAC Mode Carrier Sense Input when operating in 10/100 MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
M0M_RXD3/ M0P_TXD3 M0M_RXD2/ M0P_TXD2 M0M_RXD1/ M0P_TXD1 M0M_RXD0/ M0P_TXD0	68 69 70 71	I	-	M0M_RXD[3:0] Extension GMAC0 MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M0M_RXCLK. M0P_TXD[3:0] Extension GMAC0 MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M0P_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.
M0M_RXDV/ M0P_TXEN	72	I	-	M0M_RXDV Extension GMAC0 MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M0M_RXCLK. M0P_TXEN Extension GMAC0 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M0P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M0M_RXCLK/ M0P_TXCLK	73	I/O	-	M0M_RXCLK Extension GMAC0 MII MAC Mode Receive Clock Input. In MII 100Mbps, M0M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M0M_RXCLK is 2.5MHz Clock Input. Used to synchronize M0M_RXD[3:0], M0M_RXDV, and M0M_CRS. M0P_TXCLK Extension GMAC0 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M0P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M0P_TXCLK is 2.5MHz Clock Output. Used to synchronize M0P_TXD[3:0], and M0P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.
M0M_TXCLK/ M0P_RXCLK	75	I/O	-	M0M_TXCLK Extension GMAC0 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M0M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M0M_TXCLK is 2.5MHz Clock Input. Used to synchronize M0M_TXD[3:0], and M0M_TXEN. M0P_RXCLK Extension GMAC0 MII PHY Mode Receive Clock Output. In MII 100Mbps, M0P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M0P_RXCLK is 2.5MHz Clock Output. Used to synchronize M0P_RXD[3:0], and M0P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No.	Type	Drive (mA)	Description
M0M_TXEN/ M0P_RXDV/	76	O	-	M0M_TXEN Extension GMAC0 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M0M_TXCLK. M0P_RXDV Extension GMAC0 MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M0P_RXCLK.
M0M_TXD0/ M0P_RXD0 M0M_TXD1/ M0P_RXD1 M0M_TXD2/ M0P_RXD2 M0M_TXD3/ M0P_RXD3	77 78 79 80	O	-	M0M_TXD[3:0] Extension GMAC0 MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M0M_TXCLK. M0P_RXD[3:0] Extension GMAC0 MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M0P_RXCLK.

Table 8. Extension GMAC1 MII Pins (MII MAC Mode or MII PHY Mode)

Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_CRS	36	I	-	M1M_CRS Extension GMAC1 MII MAC Mode Carrier Sense Input when operating in 10/100 MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_TXD3/ M1P_RXD3 M1M_TXD2/ M1P_RXD2 M1M_TXD1/ M1P_RXD1 M1M_TXD0/ M1P_RXD0	41 42 43 44	O	-	M1M_TXD[3:0] Extension GMAC1 MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXD[3:0] Extension GMAC1 MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M1P_RXCLK.
M1M_TXEN/ M1P_RXDV	45	O	-	M1M_TXEN Extension GMAC1 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXDV Extension GMAC1 MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M1P_RXCLK.

Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_TXCLK/ M1P_RXCLK	47	I/O	-	M1M_TXCLK Extension GMAC1 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M1M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_TXCLK is 2.5MHz Clock Input. Used to synchronize M1M_TXD[3:0] and M1M_TXEN. M1P_RXCLK Extension GMAC1 MII PHY Mode Receive Clock Output. In MII 100Mbps, M1P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_RXCLK is 2.5MHz Clock Output. Used to synchronize M1P_RXD[3:0] and M1P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXCLK/ M1P_TXCLK	50	I/O	-	M1M_RXCLK Extension GMAC1 MII MAC Mode Receive Clock Input. In MII 100Mbps, M1M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_RXCLK is 2.5MHz Clock Input. Used to synchronize M1M_RXD[3:0], M1M_RXDV, and M1M_CRS. M1P_TXCLK Extension GMAC1 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M1P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_TXCLK is 2.5MHz Clock Output. Used to synchronize M1P_TXD[3:0] and M1P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXDV/ M1P_TXEN	51	I	-	M1M_RXDV Extension GMAC1 MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M1M_RXCLK. M1P_TXEN Extension GMAC1 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M1P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXD0/ M1P_TXD0 M1M_RXD1/ M1P_TXD1 M1M_RXD2/ M1P_TXD2 M1M_RXD3/ M1P_TXD3	52 53 54 55	I	-	M1M_RXD[3:0] Extension GMAC1 MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M1M_RXCLK. M1P_TXD[3:0] Extension GMAC1 MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M1P_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

7.3. LED Pins

The RTL8363SB LED Pins can be configured to parallel mode LED or serial mode LED interface via Register configuration. LED0, LED1, and LED2 of Port n indicate information that can be defined via register or EEPROM.

In parallel LED mode, when the LED pin is pulled low, the LED output polarity will be high active. When the LED pin is pulled high, the LED output polarity will change from high active to low active. See section 9.19 LED Indicators, page 37 for more details.

Table 9. LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P2LED2/ DIS_8051	89	I/O_{PU}	-	Port 2 LED2 Output Signal. P2LED2 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 37 for more details.
P2LED1	92	I/O_{PU}	-	Port 2 LED1 Output Signal. P2LED1 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 37 for more details.
P2LED0/ DISAUTOLOAD	91	I/O_{PU}	-	Port 2 LED0 Output Signal. P2LED0 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 37 for more details.
P1LED2/ RESERVED	93	I/O_{PU}	-	Port 1 LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 37 for more details.
P1LED1	95	I/O_{PU}	-	Port 1 LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 37 for more details.
P1LED0/ RESERVED	94	I/O_{PU}	-	Port 1 LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 37 for more details.

7.4. Configuration Strapping Pins

Table 10. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
DIS_SPIS	87	I/O_{PU}	SPI Slave Management Interface Selection. Pull Up: Disable SPI Slave Management Interface Pull Down: Enable SPI Slave Management Interface *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
DIS_ROM	88	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.*
DIS_8051	89	I/O_{PU}	Disable Embedded 8051. Pull Up: Disable embedded 8051 Pull Down: Enable embedded 8051 *Note1: The strapping pin DISAUTOLOAD and DIS_8051 are for power on or reset initial stage configuration. Refer to Table 11 Configuration Strapping Pins (DISAUTOLOAD and DIS_8051), page 21 for details.* *Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
DISAUTOLOAD/ P2LED0	91	I/O_{PU}	Disable EEPROM Auto-load. Pull Up: Disable EEPROM auto-load Pull Down: Enable EEPROM/FLASH auto-load *Note1: The strapping pin DISAUTOLOAD and DIS_8051 are for power on or reset initial stage configuration. Refer to Table 11 Configuration Strapping Pins (DISAUTOLOAD and DIS_8051), page 21 for details.* *Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
RESERVED/ P1LED2	93	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 9.19 LED Indicator, page 37 for more details.*
RESERVED/ P1LED0	94	I/O_{PU}	Internal Use/Reserved. *Note: For normal operation, this pin must be pulled low via an external 4.7k ohm resistor upon power on or reset.* *When pulled low, the LED output polarity will be high active. See section 9.19 LED Indicator, page 37 for more details.*
SMI_SEL	96	I/O_{PU}	EEPROM SMI/MII Management Interface Selection. Pull Up: EEPROM SMI interface when DIS_SPIS = 1 Pull Down: MII Management interface when DIS_SPIS = 1 *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
RESERVED	20	I	Internal Use/Reserved. *Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset.*
RESERVED	21	I	Internal Use/Reserved. *Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset.*
RESERVED	35	I	Internal Use/Reserved. *Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset.*

7.5. Configuration Strapping Pins (DISAUTOLOAD and DIS_8051)

Table 11. Configuration Strapping Pins (DISAUTOLOAD and DIS_8051)

DISAUTOLOAD	DIS_8051	Initial Stage (Power On or Reset) Loading Data	
		From	To
0	0	EEPROM	Register
	1	EEPROM	Embedded 8051 Instruction Memory
1	Irrelevant	N/A	N/A

7.6. Management Interface Pins

Table 12. Management Interface Pins

Pin Name	Pin No.	Type	Description
SPIS_CSI	103	I	When DIS_SPIS is Pulled Low, the SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Chip Selection Input pin. When DIS_SPIS is Pulled Up, the SPI Slave Management Interface is Disabled.
SPIS_CK/SCK/ MMD_MDC	99	I/O_{PU}	When DIS_SPIS is Pulled Low, the SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Serial Clock Input pin. When DIS_SPIS is Pulled Up, the SPI Slave Management Interface is Disabled. This pin act as EEPROM SMI Interface Clock/MII Management Interface Clock (selected via the hardware strapping pin, SMI_SEL).
SPIS_DI/SDA/ MMD_MDIO	102	I/O_{PU}	When DIS_SPIS is Pulled Low, the SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Serial Data Input pin. When DIS_SPIS is Pulled Up, the SPI Slave Management Interface is Disabled. This pin act as EEPROM SMI Interface Data/MII Management Interface Data (selected via the hardware strapping pin, SMI_SEL).
SPIS_DO	101	O	When DIS_SPIS is Pulled Low, the SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Serial Data Output pin. When DIS_SPIS is Pulled Up, the SPI Slave Management Interface is Disabled.
INTERRUPT	18	O_{PU}	Interrupt Output for External CPU.

7.7. Miscellaneous Pins

Table 13. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
XTALO	97	AO	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output.
XTALI	98	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz +/-50ppm tolerance crystal reference or oscillator input.
MDIREF	10	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
RESERVED	31	AO	Reserved. Must be left floating in normal operation.
RESERVED	32	AO	Reserved. Must be left floating in normal operation.
nRESET	104	I_S	System Reset Input Pin. When low active will reset the RTL8363SB.

7.8. Test Pins

Table 14. Test Pins

Pin Name	Pin No.	Type	Description
RTT1	12	AO	Reserved for Internal Use. Must be left floating.
RTT2	14	AO	Reserved for Internal Use. Must be left floating.

7.9. Power and GND Pins

Table 15. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO_0	61, 85	P	Digital I/O High Voltage Power for Extension Port 0 General Purpose Interface, Management Interface, and nRESET.
DVDDIO_1	46, 60	P	Digital I/O High Voltage Power for Extension Port 1 General Purpose Interface.
DVDDIO	16	P	Digital I/O High Voltage Power for INTERRUPT, DIS_LPD/BUZZER.
DVDDL	19, 62, 86	P	Digital Low Voltage Power.
AVDDH	5, 8, 15, 28, 30, 106, 108, 122	AP	Analog High Voltage Power.
AVDDL	6, 11, 27, 29, 107, 113, 128	AP	Analog Low Voltage Power.
PLLVDDL0	119	AP	PLL0 Low Voltage Power.
GND	7, 13, 17, 23, 24, 25, 26, 33, 34, 49, 90, 100, 105, 114, 121, 127	G	GND.
AGND	9	AG	Analog GND.
PLLGND0	120	AG	PLL0 GND.

8. Physical Layer Functional Overview

8.1. MDI Interface

The RTL8363SB embeds Dual Gigabit Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

8.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

8.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

8.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

8.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal0), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

8.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

8.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

8.8. Auto-Negotiation for UTP

The RTL8363SB obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8363SB advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

8.9. Crossover Detection and Auto Correction

The RTL8363SB automatically determines whether or not it needs to crossover between pairs (see Table 16) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8363SB automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 16. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

8.10. Polarity Correction

The RTL8363SB automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

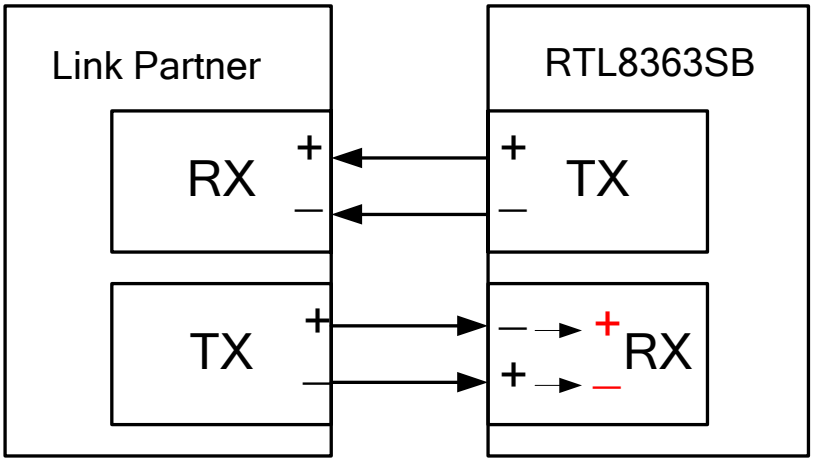


Figure 4. Conceptual Example of Polarity Correction

9. General Function Description

9.1. Reset

9.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8363SB will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Auto-load the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

9.1.2. Software Reset

The RTL8363SB supports two software resets; a chip reset and a soft reset.

9.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

9.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list
2. Restart the auto-negotiation process

9.2. IEEE 802.3x Full Duplex Flow Control

The RTL8363SB supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

9.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called 'Truncated Binary Exponential Backoff'. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL8363SB is 9.

The half duplex back-off algorithm in the RTL8363SB does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

9.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8363SB sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL8363SB supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

9.4. Search and Learning

Search

When a packet is received, the RTL8363SB uses the destination MAC address, Filtering Identifier (FID) and Enhanced FID (EFID) to search the 2K-entry look-up table. The 48-bit MAC address, 4-bit FID and 3-bit EFID use a hash algorithm, to calculate an 11-bit index value. The RTL8363SB uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8363SB uses the source MAC address, FID, and EFID of the incoming packet to hash into a 9-bit index. It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8363SB will update the entry with new information. If there is no match and the 2K entries are not all occupied by other MAC addresses, the RTL8363SB will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

The RTL8363SB supports a 64-entry Content Addressable Memory (CAM) to avoid look-up table hash collisions. When all 2K entries in the look-up table index are occupied, the source MAC address can be learned into the 64-entry CAM. If both the look-up table and the CAM are full, the source MAC address will not be learned in the RTL8363SB.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8363SB is between 200 and 400 seconds (typical is 300 seconds).

9.5. SVL and IVL/SVL

The RTL8363SB supports a 16-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

9.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8363SB. The maximum packet length may be set to 1522, 1536, 1552, or 16K bytes.

9.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8363SB supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 17 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 17. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
Provider Bridge Group Address	1-80-C2-00-00-08
Undefined 802.1 Address	01-80-C2-00-00-04 ~ 01-80-C2-00-00-07 & 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C & 01-80-C2-00-00-0F
Provider Bridge MVRP Address	01-80-C2-00-00-0D
IEEE Std 802.1AB Link Layer Discovery Protocol Address	01-80-C2-00-00-0E
All LANs Bridge Management Group Address	01-80-C2-00-00-10
Load Server Generic Address	01-80-C2-00-00-11
Loadable Device Generic Address	01-80-C2-00-00-12
Undefined 802.1 Address	01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F
Generic Address for All Manager Stations	01-80-C2-00-00-18
Generic Address for All Agent Stations	01-80-C2-00-00-1a
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F

9.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8363SB enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate, all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

9.9. Port Security Function

The RTL8363SB supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

9.10. MIB Counters

The RTL8363SB supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

9.11. Port Mirroring

The RTL8363SB supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored to multiple mirror ports.

9.12. VLAN Function

The RTL8363SB supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to 'Admit All' or 'Admit All Tagged'
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8363SB will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8363SB also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8363SB supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8363SB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

9.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached serial EEPROM or EEPROM SMI Slave interface. The 4K-entry VLAN Table designed into the RTL8363SB provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

9.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8363SB supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8363SB uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8363SB compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8363SB performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q

tag aware VLAN' is disabled, the RTL8363SB performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when '802.1Q tag aware VLAN' is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL8363SB. One is the 'VLAN tag admit' control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering', which will drop frames if the ingress port is not in the member set.

9.12.3. Protocol-Based VLAN

The RTL8363SB supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 5. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be 'Ethernet', and value to be '0x0800'. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

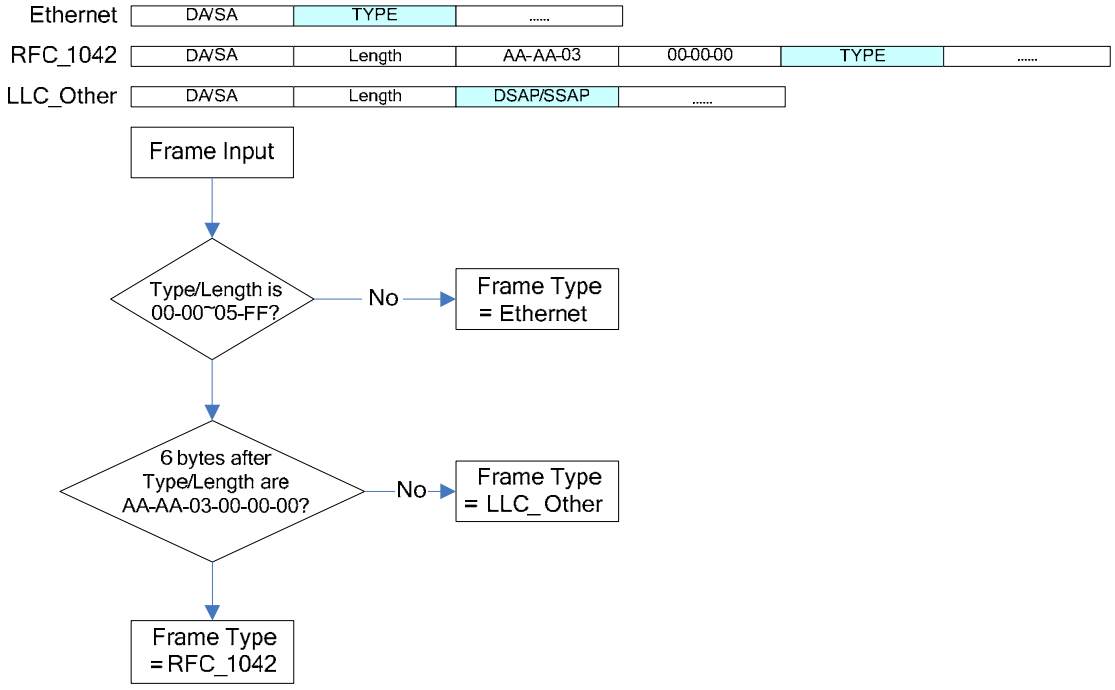


Figure 5. Protocol-Based VLAN Frame Format and Flow Chart

9.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8363SB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL8363SB will drop non-tagged packets and packets with an incorrect PVID.