



# REALTEK

## RTL8366/RTL8369

### 6/9-PORT 10/100/1000MBPS SWITCH CONTROLLER

## DATASHEET

Rev. 1.1

05 September 2005

Track ID: JATR-1076-21



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**USING THIS DOCUMENT**

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8366 and RTL8369 chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

**REVISION HISTORY**

| Revision | Release Date | Summary   |
|----------|--------------|---|
| 1.0      | 2005/08/17   | First release.  |
| 1.1      | 2005/09/05   | Change all model numbers RTL8365 to RTL8366.<br>Change Reference resistor value (see Table 7, page 15). |

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## 1. General Description

The RTL8366 and RTL8369 are 128-pin, ultra-low-power, high-performance 5/8-port Gigabit Ethernet switches, with one extra GMII/MII/RGMII port for specific applications. They integrate all the functions of a high speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single 0.15 $\mu$ m CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8366/8369 features superior memory management technology to efficiently utilize memory space. An integrated 4K-entry look-up table stores MAC addresses and associated information in a 12-bit direct mapping scheme. The table provides read/write access from the EEPROM Serial Management Interface (SMI), and each of the entries can be configured as a static entry. The entry aging time is between 200 and 400 seconds.

The RTL8369 implements a 4 channel Reduced Serial Gigabit Media Independent Interface (RSGMII) 2.5GHz serial differential interface that connects with 4 RTL8212's. Each channel carries 2Gbps of data to and from the RTL8212. The RSGMII interfaces help reduce PCB size and layout complexity.

The 6/9th port of the RTL8366/8369 implements a GMII/MII/RGMII interface for connecting with an external PHY or MAC in specific applications. This interface could be connected to an external CPU or RISC in 1 WAN + 4 LAN or 1 WAN + 8 LAN Router applications. In router applications, the RTL8366/8369 supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. When using this function, VID information carried in the VLAN tag will be changed to PVID.

The RTL8366/8369 supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including packet buffers and transmitting queues. If one of the forwarding ports are blocked, or system resources are unavailable, broadcast frames will be dropped according to the system configuration. The RTL8366/8369 supports two dropping methods:

- The input dropping method will not forward broadcast packets to any output ports and will drop these packets directly.
- The output dropping method will forward broadcast packets to non-blocked ports only.

To improve real-time and multimedia networking applications, the RTL8366/8369 supports three types of QoS (Quality of Service). These are based on (1) Port-based priority, (2) 802.1p/Q VLAN priority tag, (3) TOS field in the IPv4 header. Each output port supports a weighted ratio of high-priority and low-priority queues to fit bandwidth requirements in various applications.

The RTL8366/8369 provides a 4K-entry VLAN table for 802.1Q port-based and tag-based VLAN operation to separate logical connectivity from physical connectivity. Each port may be set to any topology via EEPROM upon reset, or EEPROM SMI after reset. The RTL8366/8369 also provides options to meet special application requirements. The first option is the ARP VLAN function, which is used to select to broadcast ARP frames to all VLANs, or only forward ARP frames to the originating VLAN. The second option is the Leaky VLAN function, which sends unicast frames to other VLANs, or only forwards unicast frames to the originating VLAN. The VLAN tags can be inserted or removed on a per-port basis.

## 2. Features

- 6/9-port gigabit non-blocking switch architecture
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- IEEE 802.3x flow control with asymmetric flow control ability
- 1Mbit SRAM for packet buffer
- 4K-entry SRAM MAC lookup table
- Supports 9Kbyte jumbo frame packet forwarding
- Integrates 4 pairs of 2.5GHz high-speed serial links
- Supports Spanning Tree port status behavior configuration
- Extra Interface (port 6/9) supports:
  - ◆ Media Independent Interface (MII) (supports 100Mbps only)
  - ◆ Gigabit Media Independent Interface (GMII) (supports 1000Mbps only)
  - ◆ Reduced Gigabit Media Independent Interface (RGMII) (supports 1000Mbps only)
- VLAN
  - ◆ 802.1Q VLAN support for 4096 entries
  - ◆ Supports port-based VLAN
  - ◆ Supports per-port egress VLAN tagging and un-tagging
- QoS
  - ◆ Two levels of queue priority
  - ◆ Priority determined by Port, 802.1Q VLAN tag, IP TOS/DS field
- Security Filtering
  - ◆ Disable learning for each port
  - ◆ Disable learning-table aging for each port
  - ◆ Drop unknown DA for each port
- Broadcast storm control protects system from attack by broadcast packets
- Supports Matrix LEDs and serial LEDs
- Port Mirroring
  - ◆ Mirror to any port
  - ◆ TX and RX separated
- Supports MIB counters with 3x32bits/per port
- Supports EEPROM SMI to access configuration register
- Supports 256 bytes EEPROM space for configuration
- 25MHz crystal or 1.8V OSC input
- Low power, 1.8/3.3V, 0.15 $\mu$ m CMOS process, 128-pin PQFP package

### **3. Applications**

- 5/8-port 1000Base-T switch
- 1 WAN + 4 LAN, or 1 WAN + 8 LAN 1000Base-T Router or MIMO-Gateway application

## 4. Block Diagram

### 4.1. Block Diagram of RTL8366

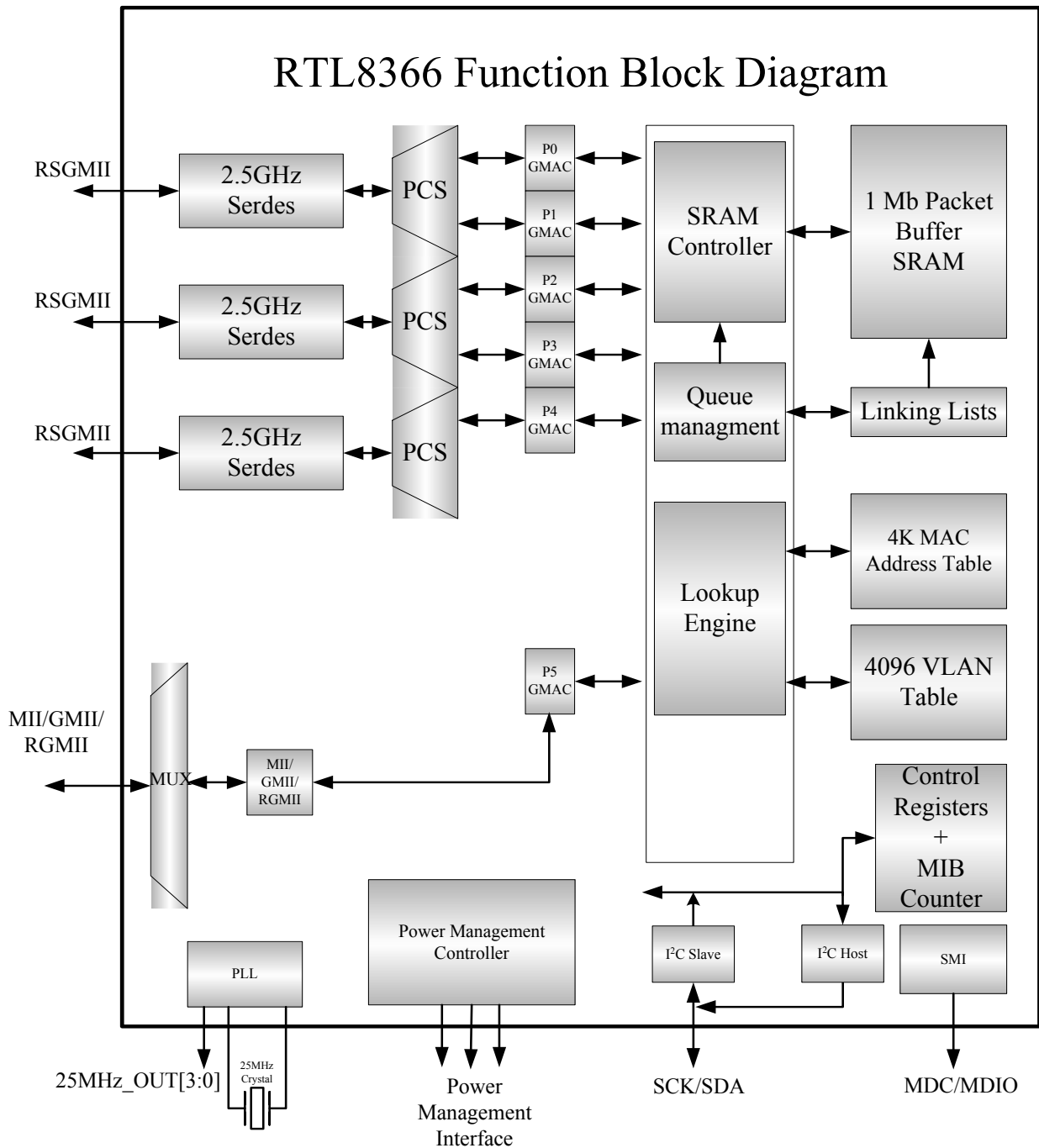


Figure 1. Block Diagram of RTL8366

## 4.2. Block Diagram of RTL8369

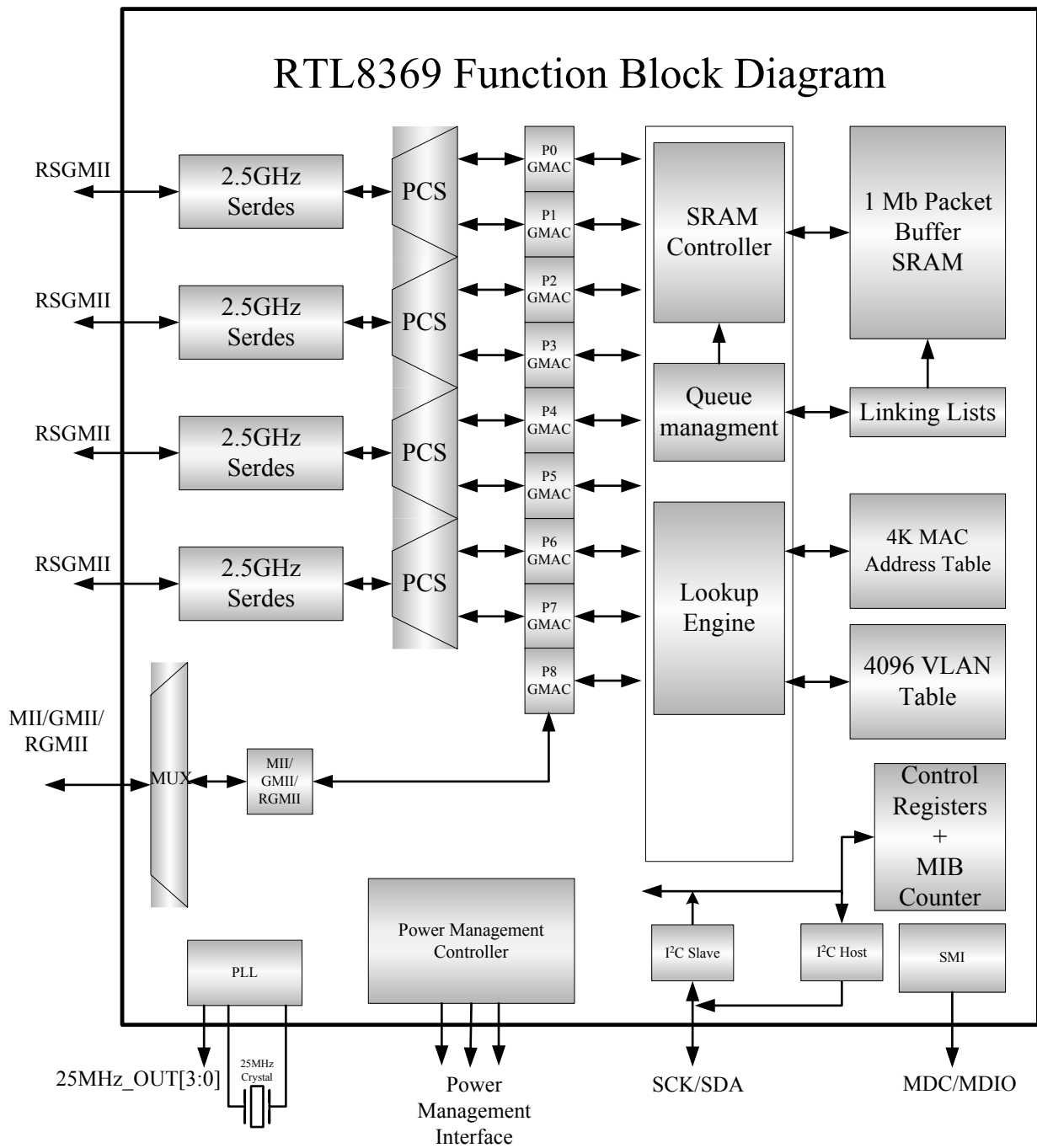


Figure 2. Block Diagram of RTL8369

## 5. Application Examples

### 5.1. 8-Port 1000Base-T Switch

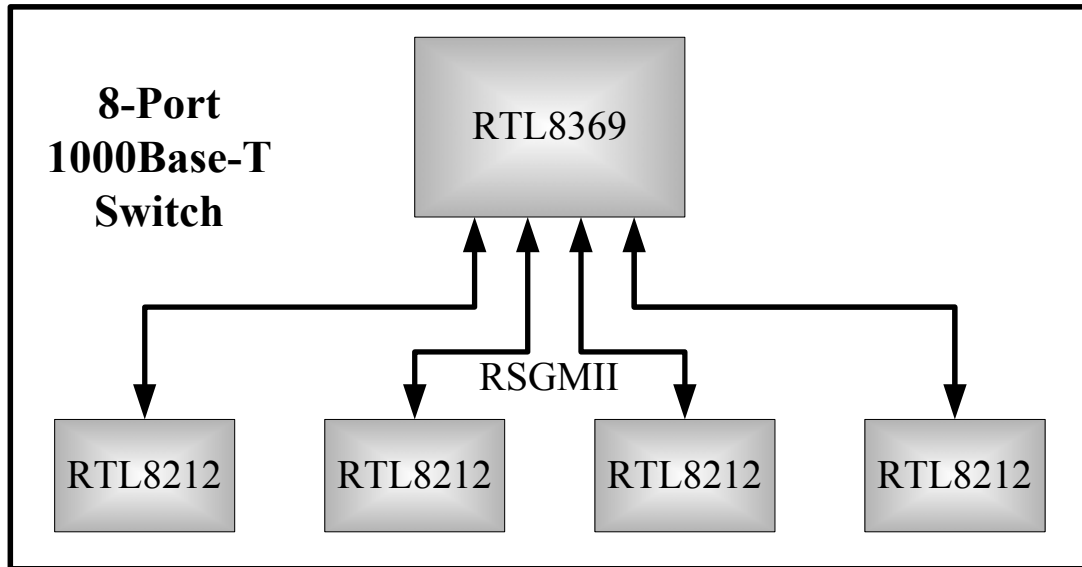


Figure 3. 8-Port 1000Base-T Switch

### 5.2. 5-Port 1000Base-T Switch

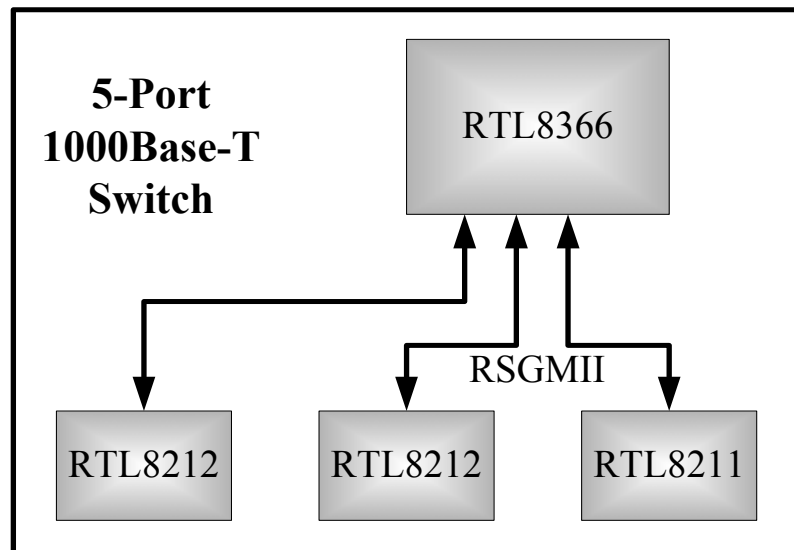


Figure 4. 5-Port 1000Base-T Switch



### 5.3. 9-Port (8 LAN+1 WAN) 1000Base-T Router

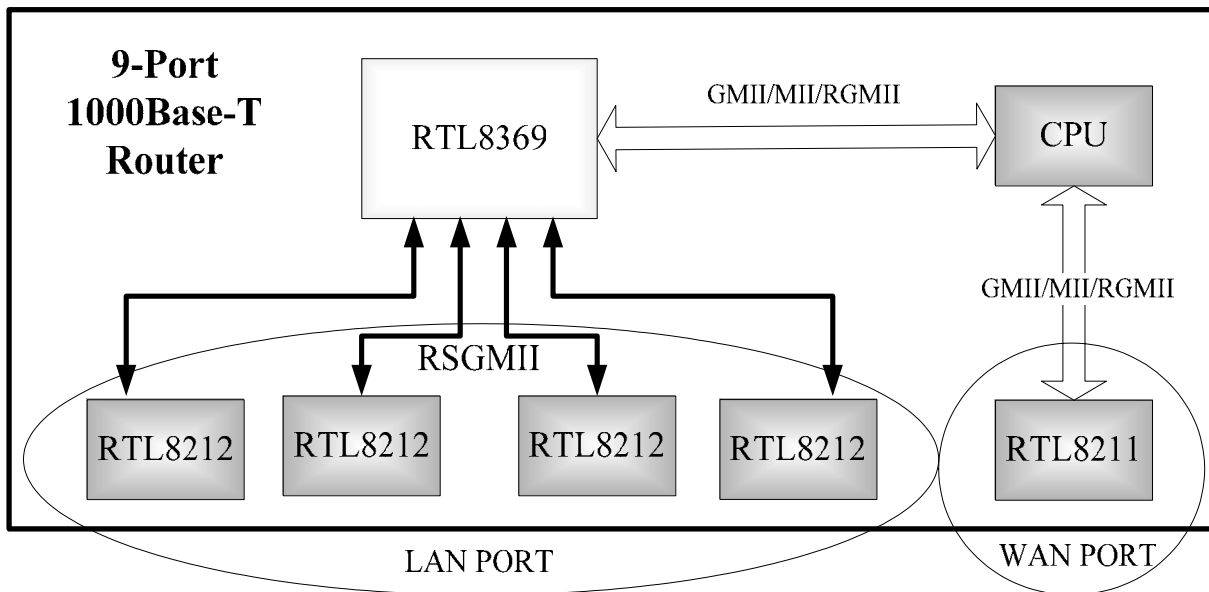


Figure 5. 9-Port (8 LAN+1 WAN) 1000Base-T Router

### 5.4. 5-Port (4 LAN+1 WAN) 1000Base-T Router

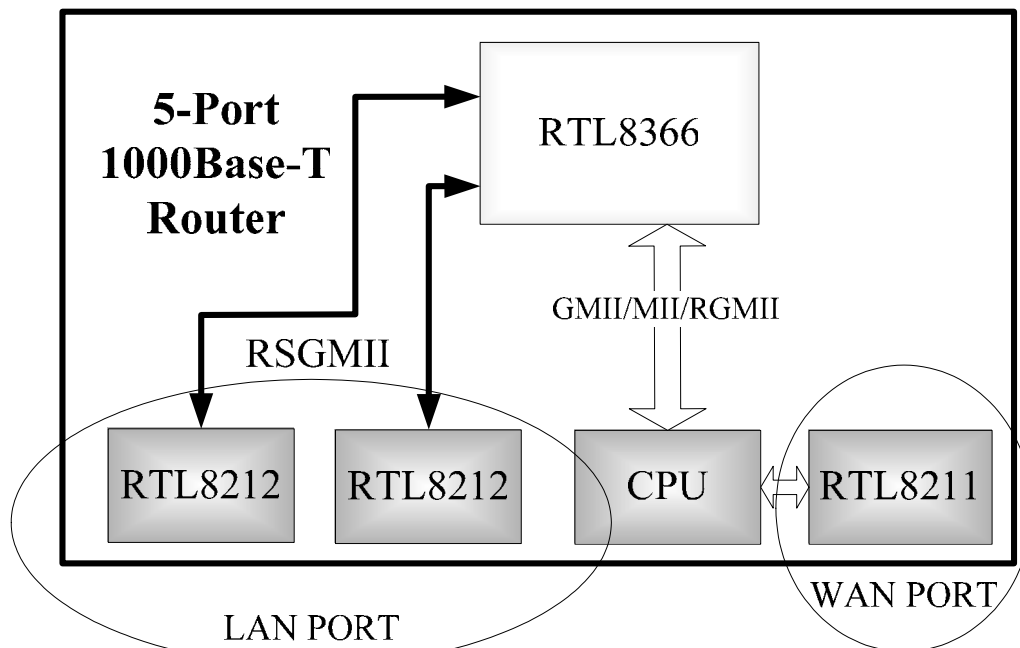


Figure 6. 5-Port (4 LAN+1 WAN) 1000Base-T Router



### 6.3. RTL8369 Pin Assignments

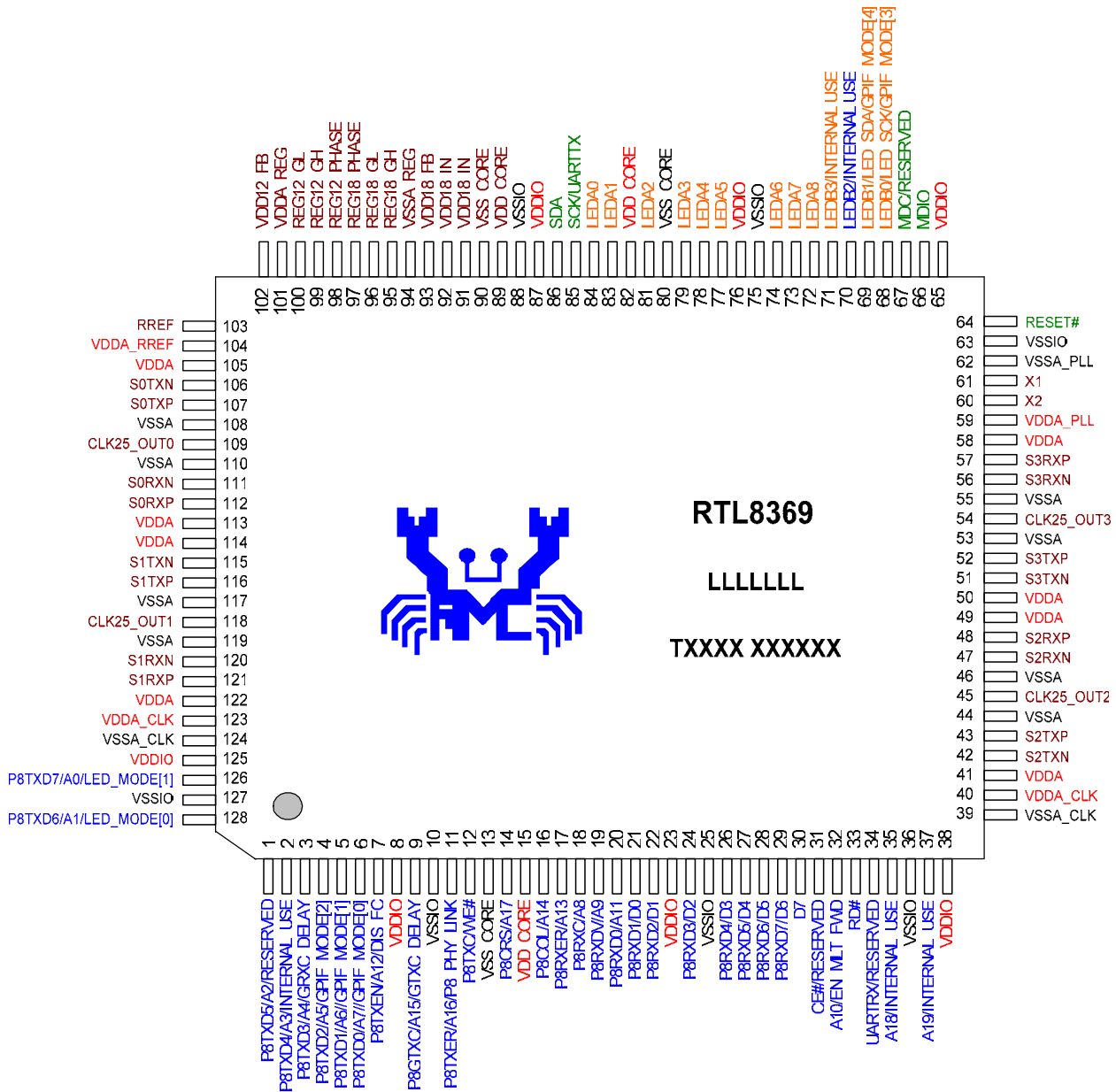


Figure 8. RTL8369 Pin Assignments

### 6.4. Package Identification

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 8.

## 7. Pin Descriptions

### 7.1. Pin Type Conventions

The signal type codes below are used in the following tables:

|           |                        |
|-----------|------------------------|
| I: Input  | D: Digital             |
| O: Output | PU: Internal pull-up   |
| A: Analog | PD: Internal pull-down |

### 7.2. RSGMII Pins

**Table 1. RSGMII Pins**

| Pin Name  | Pin No.                                     | Type | Description   |
|---|---|------|---|
| S0RXP, S0RXN,<br>S1RXP, S1RXN,<br>S2RXP, S2RXN,<br>S3RXP, S3RXN | 112, 111,<br>121, 120,<br>48, 47,<br>57, 56 | AI   | Differential Input: 2.5GHz serial interfaces to transfer data from an RTL8212 to the RTL8366/RTL8369.<br>For the RTL8369:<br>‘S0RXP, S0RXN’ conveys the traffic of port0 and port1<br>‘S1RXP, S1RXN’ conveys the traffic of port2 and port3<br>‘S2RXP, S2RXN’ conveys the traffic of port4 and port5<br>‘S3RXP, S3RXN’ conveys the traffic of port6 and port7<br>For RTL8366:<br>‘S0RXP, S0RXN’ conveys the traffic of port0 and port1<br>‘S1RXP, S1RXN’ conveys the traffic of port2 and port3<br>‘S2RXP, S2RXN’ conveys the traffic of port4<br>‘S3RXP, S3RXN’ are not available<br>These pins must be pulled low with a 1K Ohm resistor when not used. |
| S0TXP, S0TXN,<br>S1TXP, S1TXN,<br>S2TXP, S2TXN,<br>S3TXP, S3TXN | 107, 106,<br>116, 115,<br>43, 42,<br>52, 51 | AO   | Differential Output: 2.5GHz serial interfaces to transfer data from the RTL8366/RTL8369 to an RTL8212.<br>For the RTL8369:<br>‘S0TXP, S0TXN’ conveys the traffic of port0 and port1<br>‘S1TXP, S1TXN’ conveys the traffic of port2 and port3<br>‘S2TXP, S2TXN’ conveys the traffic of port4 and port5<br>‘S3TXP, S3TXN’ conveys the traffic of port6 and port7<br>For RTL8366:<br>‘S0TXP, S0TXN’ conveys the traffic of port0 and port1<br>‘S1TXP, S1TXN’ conveys the traffic of port2 and port3<br>‘S2TXP, S2TXN’ conveys the traffic of port4<br>‘S3TXP, S3TXN’ are not available   |

| Pin Name       | Pin No.             | Type | Description  |
|----------------|---------------------|------|--|
| CLK25_OUT[3:0] | 54, 45,<br>118, 109 | O    | For the RTL8369:<br>CLK25_OUT[3:0] are 25MHz reference clock outputs for the RSGMII interface. 1.8V DC signal.<br>For the RTL8366:<br>CLK25_OUT[2:0] are 25MHz reference clock outputs for the RSGMII interface. 1.8V DC signal.<br>CLK25_OUT[3] is not available. |

### 7.3. General Purpose Interfaces

General Purpose Interfaces include GMII MAC, MII MAC, RGMII, and MII PHY interfaces. The interfaces are selected by the pulling up or down of GPIF\_MODE[4:0] pins upon power on. Interface selection may also be configured by register access after power on.

#### 7.3.1. GMII Pins

When port8 is linked at 1000Mbps, the interface will be GMII. When port8 is linked at 100Mbps, the interface will be MII. 1000Mbps Half Duplex and 10Mbps mode are not supported in this configuration.

**Table 2. GMII Pins**

| Pin Name   | Pin No.                       | Type | Description  |
|------------|-------------------------------|------|--|
| P8TXD[7:0] | 126, 128, 1, 2,<br>3, 4, 5, 6 | O    | Transmit Data Output (GMII/MII mode).<br>Transmits data synchronously to the rising edge of P8GTXC.<br>In 100Mbps MII MAC mode, only P8TXD[3:0] are available.   |
| P8TXEN     | 7                             | O    | Transmit Data Enable (GMII/MII mode).<br>Transmit enable that is sent synchronously at the rising edge of P8GTXC in GMII mode.<br>Transmit enable that is sent synchronously at the rising edge of P8TXC in 100Mbps MII MAC mode.                                    |
| P8GTXC     | 9                             | O    | GMII Transmit Clock (GMII mode).<br>125MHz transmit clock output when GMII is operating at 1000Mbps. Used for P8TXD[7:0] and P8TXEN synchronization.   |
| P8TXER     | 11                            | O    | Transmit Data Error (GMII/MII mode).   |
| P8TXC      | 12                            | I    | MII Transmit Clock (MII mode).<br>25MHz clock driven by PHY when operating in 100Mbps MII MAC mode.<br>P8TXD[3:0], P8TXEN and P8TXER will be synchronized with P8TXC in this mode.<br>This pin must be pulled low with a 1K Ohm resistor in GMII mode configuration. |
| P8CRS      | 14                            | I    | Carrier Sense Input (MII mode).<br>P8CRS is only valid in 100Mbps MII MAC half duplex mode. It is asserted high when a valid carrier is detected on the media.<br>This pin must be pulled low with a 1K Ohm resistor when not used.                                  |

| Pin Name   | Pin No.                        | Type | Description   |
|------------|--------------------------------|------|---|
| P8COL      | 16                             | I    | Collision Detect Input (MII mode).<br>P8COL is only valid in 100Mbps MII MAC half duplex mode. It is asserted high when a collision is detected on the media.<br>This pin must be pulled low with a 1K Ohm resistor when not used.  |
| P8RXER     | 17                             | I    | Receive Data Error. (GMII/MII mode)<br>Indicates that the receiving Data is error. The switch filters the receiving packet once the P8RXER is asserted at the rising edge of P8RXC. Valid both in GMII mode and 100Mbps MII MAC mode.<br>This pin must be pulled low when not used.   |
| P8RXC      | 18                             | I    | GMII/MII Receive Clock Input (GMII/MII mode).<br>In GMII mode: 125MHz receive clock. Used to synchronize P8RXD[7:0], P8RXER, and P8RXDV.<br>In MII 100Mbps mode. P8RXC is 25MHz. Used to synchronize P8RXD[3:0], P8RXER, P8RXDV, P8CRS, and P8COL.<br>This pin must be pulled low with a 1K Ohm resistor when not used.<br>This pin must be pulled low with a 1K Ohm resistor in GMII and RGMII mode configuration. |
| P8RXDV     | 19                             | I    | Receive Data Valid Input (GMII/MII mode).<br>Receive data valid that is received synchronously at the rising edge of P8RXC in both GMII and 100Mbps MII MAC mode.<br>This pin must be pulled low with a 1K Ohm resistor when not used.  |
| P8RXD[7:0] | 29, 28, 27, 26, 24, 22, 21, 20 | I    | Receive Data Input (GMII/MII mode).<br>Receive data that is received synchronously at the rising edge of P8RXC.<br>In 100Mbps MII MAC mode, only P8RXD[3:0] are available.<br>These pins must be pulled low with a 1K Ohm resistor when not used.<br>P8RXD[7:4] pins must be pulled low with a 1K Ohm resistor in RGMII and MII mode configuration.   |

### 7.3.2. RGMII Pins

The RGMII interface only supports 1000Mbps Full Duplex mode. 10/100Mbps are not supported by this interface.

**Table 3. RGMII Pins**

| Pin Name   | Pin No.    | Type | Description   |
|------------|------------|------|---|
| P8TXD[3:0] | 3, 4, 5, 6 | O    | RGMII Transmit Data.<br>Transmits data bus synchronously to P8GTXC.   |
| P8TXCTRL   | 11         | O    | RGMII Transmit Control signal.<br>The P8TXCTRL indicates P8TXEN at the rising edge of P8TXC and P8TXER; at the falling edge of P8TXC. At P8GXTC falling edge, P8TXCTRL=P8TXEN (XOR) P8TXER. |
| P8TXC      | 9          | O    | RGMII Transmit Clock.<br>When port 8 is linked at 1000Mbps:<br>P8TXC is 125MHz. Used for P8TXD[3:0] and P8TXCTRL synchronization at P8TXC on both rising and falling edges.                 |

| Pin Name   | Pin No.        | Type | Description   |
|------------|----------------|------|---|
| P8RXC      | 18             | I    | <p>RGMI Receive Clock.</p> <p>When port 8 is linked at 1000Mbps:<br/>P8RXC is 125MHz. Used for P8RXD[3:0] and P8RXCTRL synchronization at both P8RXC rising and falling edge.</p> <p>This pin must be pulled low with a 1K Ohm resistor when not used.</p>              |
| P8RXCTRL   | 17             | I    | <p>RGMI Transmit Control signal.</p> <p>The P8RXCTRL indicates P8RXDV at the rising of P8RXC and P8RXER at the falling edge of P8RXC. At P8RXC falling edge, P8RXCTRL=P8RXDV (XOR) P8RXER.</p> <p>This pin must be pulled low with a 1K Ohm resistor when not used.</p> |
| P8RXD[3:0] | 24, 22, 21, 20 | I    | <p>RGMI Receive Data.</p> <p>Transmits data bus synchronously to P8RXC.</p> <p>These pins must be pulled low with a 1K Ohm resistor when not used.</p>  |

### 7.3.3. MII PHY Mode Interface Pins

**Table 4. MII PHY Mode Interface Pins**

| Pin Name    | Pin No.        | Type | Description  |
|-------------|----------------|------|--|
| P8PRXD[3:0] | 3, 4, 5, 6     | O    | <p>MII PHY Mode Receive Data.</p> <p>Output data bus to MAC, synchronous to the rising edge of P8PRXC.</p>   |
| P8PRXDV     | 7              | O    | <p>MII PHY Mode Receive Data Valid.</p> <p>Output data valid signal to MAC, synchronous to the rising edge of P8PRXC.</p>  |
| P8PRXC      | 9              | O    | <p>MII PHY Mode Receive Clock.</p> <p>In MII 100Mbps PHY mode, P8PRXC is 25MHz clock output.</p> <p>In MII 10Mbps PHY mode, P8PRXC is 2.5MHz clock output.</p> <p>Used to synchronize P8PRXD[3:0] and P8PRXDV.</p>   |
| P8PTXER     | 17             | I    | <p>MII PHY Mode Transmit Error.</p> <p>This pin must be pulled low with a 1K Ohm resistor when not used.</p>   |
| P8PTXC      | 18             | I    | <p>MII PHY Mode Transmit Clock.</p> <p>Transmit clock input from MII MAC is used for P8PTXD[3:0] and P8PTXEN synchronization.</p> <p>In MII 100Mbps PHY mode, P8PTXC is 25MHz clock input.</p> <p>In MII 10Mbps PHY mode, P8PTXC is 2.5MHz clock input.</p> <p>This pin must be pulled low with a 1K Ohm resistor when not used.</p> |
| P8PTXEN     | 19             | I    | <p>MII PHY Mode Transmit Data Enable.</p> <p>Transmit enable input from MII MAC is synchronous at the rising edge of P8PTXC.</p> <p>This pin must be pulled low with a 1K Ohm resistor when not used.</p>  |
| P8PTXD[3:0] | 24, 22, 21, 20 | I    | <p>MII PHY Mode Transmit Data.</p> <p>Transmit data input bus from MII MAC are synchronous to the rising edge of P8PTXC.</p> <p>These pins must be pulled low with a 1K Ohm resistor when not used.</p>  |

## 7.4. LED Pins

**Table 5. LED Pins**

| Pin Name  | Pin No.                            | Type   | Description   |
|-----------|------------------------------------|--|---|
| LEDA[8:0] | 72, 73, 74, 77, 78, 79, 81, 83, 84 | O <sub>PU</sub>  | When configuration register LED_MODE[1:0]=0b00 or 0b01, LEDA[8:0] is driven low to enable port status in matrix LED applications.<br>When configuration register LED_MODE[1:0]=0b10, LEDA[8:0] associates the LEDB0 for bi-color LED application.   |
| LEDB[3:0] | 71, 70, 69, 68                     | I/O <sub>PU</sub><br>I/O <sub>PD</sub><br>I/O <sub>PD</sub><br>I/O <sub>PD</sub> | When configuration register LED_MODE=0b00 or 0b01, the LEDB[3:0] indicates the status bit 0 of matrix LED application.<br>When configuration register LED_MODE=0b10, the LEDB0 is used for bi-color LED.<br>When configuration register LED_MODE=0b11, LEDB0 drives the clock for serial LED applications, and LEDB1 drives data for serial LED applications. |

## 7.5. Power Management Pins

**Table 6. Power Management Pins**

| Pin Name    | Pin No. | Type | Description  |
|-------------|---------|------|--|
| REG18_GH    | 95      | AO   | TBD (Floating when not used)                         |
| REG18_GL    | 96      | AO   | TBD (Floating when not used)                         |
| REG18_PHASE | 97      | AI   | TBD (Pull down with a 1K Ohm resistor when not used) |
| REG12_GH    | 99      | AO   | TBD (Floating when not used)                         |
| REG12_GL    | 100     | AO   | TBD (Floating when not used)                         |
| REG12_PHASE | 98      | AI   | TBD (Pull down with a 1K Ohm resistor when not used) |
| VDD18_FB    | 93      | AI   | TBD (Pull down with a 1K Ohm resistor when not used) |
| VDD12_FB    | 102     | AI   | TBD (Pull down with a 1K Ohm resistor when not used) |

## 7.6. Miscellaneous Pins

**Table 7. Miscellaneous Pins**

| Pin Name | Pin No. | Type              | Description  |
|----------|---------|-------------------|--|
| MDC      | 67      | I/O <sub>PD</sub> | MII management interface clock pin.  |
| MDIO     | 66      | I/O               | MII management interface data pin.   |
| SCK      | 85      | I/O <sub>PD</sub> | Clock of EEPROM SMI. EEPROM interface when GPIF_MODE[4:0] != 0b01000.                      |
| SDA      | 86      | I/O               | Data of EEPROM SMI. EEPROM interface when GPIF_MODE[4:0] != 0b01000.                       |
| X1, X2   | 61, 60  | A                 | 1.8V 25MHz crystal clock input and feedback pins.  |
| RREF     | 103     | A                 | Reference resistor.<br>A 2.49K Ohm (1%) resistor should be connected between RREF and GND. |
| RESET#   | 64      | DI                | System pin reset input. Low active use to reset RTL8366/RTL8369.                           |



## 7.7. Configuration Strapping Pins

**Table 8. Configuration Strapping Pins**

| Pin Name       | Pin No.            | Default | Description   |
|----------------|--------------------|---------|---|
| P8RXC_DELAY    | 3                  | 0b1     | 0b1: Adds a 1.5ns delay at P8RXC (RGMII Only)<br>Internal pull high with a 75K Ohm resistor.  |
| P8TXC_DELAY    | 9                  | 0b1     | 0b1: Adds a 1.5ns delay at P8RXC (RGMII Only)<br>Internal pull high with a 75K Ohm resistor.  |
| RESERVED       | 37, 35             | 0b00    | N/A<br>Internal pull down with a 75K Ohm resistor.  |
| GPIF_MODE[4:0] | 69, 68, 4,<br>5, 6 | 0b11000 | 0b11000: GMII/MII MAC Mode.<br>0b11001: RGMII.<br>0b11100: MII PHY Mode.<br>Others: Reserved<br><br>If the General Purpose Interface is in MII PHY Mode, then it is full duplex.<br>Flow control setting is from EEPROM.<br>GPIF_MODE[2:0] are internal pull down with a 75K Ohm resistor.<br>GPIF_MODE[4:3] are internal pull high with a 75K Ohm resistor.<br><i>Note 1: GMII/MII MAC mode does not support 10Mbps.</i><br><i>Note 2: MII PHY mode only supports 100Mbps Full duplex.</i> |
| RESERVED       | 31, 34,<br>67      | 0b000   | N/A<br>Internal pull down with a 75K Ohm resistor.  |
| INTERNAL USE   | 70                 | 0b0     | N/A<br>Internal pull down with a 75K Ohm resistor.  |
| INTERNAL USE   | 71                 | 0b0     | N/A<br>Internal pull down with a 75K Ohm resistor.  |
| DIS_FC         | 7                  | 0b0     | 0b0: Enable all ports 802.3x flow control ability.<br>0b1: Disable all ports 802.3x flow control ability.<br>Internal pull down with a 75K Ohm resistor.  |
| LED_MODE[1:0]  | 126, 128           | 0b00    | 0b00: Matrix Mode Type 1<br>LEDB[3:0]=100M, 1000M, LINK/ACT, DUPLEX/COL<br>0b01: matrix mode type 2<br>LEDB[3:0]=10M LINK/ACT, 100M LINK/ACT, 1000M LINK/ACT,<br>DUPLEX/COL<br>0b10: Bi-color matrix mode<br>LEDB[3:0]=N/A, N/A, N/A, (1000M+Link/Act, 100M/10M+Link/ACT)<br>0b11: serial LED mode<br>LEDB0 is LED_CLK and LEDB1 is LED_DATA.<br>Internal pull down with a 75K Ohm resistor.<br>For a detailed description, see section 8.11 LED, page 24.                                  |

| Pin Name    | Pin No. | Default | Description  |
|-------------|---------|---------|--|
| EN_MLT_FWD  | 32      | 0b1     | 0b0: Discard 802.1D reserve control frame (01-80-C2-00-00-04 ~ 01-80-C2-00-00-FF)<br>0b1: Forward 802.1D reserve control frame (01-80-C2-00-00-04 ~ 01-80-C2-00-00-FF)<br><br>01-80-C2-00-00-01 and 01-80-C2-00-00-02: Drop (default)<br>01-80-C2-00-00-00 and 01-80-C2-00-00-03: Forward (default)<br>Internal pull high with a 75K Ohm resistor. |
| P8_PHY_LINK | 11      | 0b0     | To configure Port 8 PHY mode link status when GPIF_MOD[4:0]=0b11100.<br>0b0: PHY Mode LINK down<br>0b1: PHY Mode LINK up<br>Internal pull down with a 75K Ohm resistor.  |
| RESERVED    | 2       | 0b0     | N/A<br>Internal pull down with a 75K Ohm resistor.   |

## 7.8. Power and GND Pins

**Table 9. Power and GND Pins**

| Pin Name  | Pin No.                            | Description  |
|-----------|------------------------------------|--|
| VDD_CORE  | 15, 82, 89                         | Power for digital circuit.<br>1.5V DC input when internal linear regulator is disabled.<br>When internal linear regulator is enabled, these pins must connect to Ground via bypass capacitors. |
| VSS_CORE  | 13, 80, 90                         | Ground for digital circuit.  |
| VDDIO     | 8, 23, 38, 65, 76, 87, 125         | Power for I/O pads. 3.3V DC input.   |
| VSSIO     | 10, 25, 36, 63, 75, 88, 127        | Ground for I/O pads.   |
| VDDA      | 41, 49, 50, 58, 105, 113, 114, 122 | Power for RSGMII. 1.8V DC input.   |
| VSSA      | 44, 46, 53, 55, 108, 110, 117, 119 | Ground for RSGMII.   |
| VDDA_CLK  | 40, 123                            | Power for RSGMII 25MHz output clock. 1.8V DC input.  |
| VSSA_CLK  | 39, 124                            | Ground for RSGMII 25MHz output clock.  |
| VDDA_REG  | 101                                | Power for power management. 3.3V DC input.<br>Connect to system ground when not use.   |
| VSSA_REG  | 94                                 | Ground for power management.   |
| VDDA_PLL  | 59                                 | Power for PLL. 1.8V DC input.  |
| VSSA_PLL  | 62                                 | Ground for PLL.  |
| VDDA_RREF | 104                                | Power for Reference resistor. 3.3V DC input.   |
| VDD18_IN  | 91, 92                             | Power for linear regulator circuit. DC 1.8V input.<br>If these pins are left floating, the internal 1.5V linear regulator is disabled.   |
| VDD18_FB  | 93                                 | TBD. Pull down with 1K Ohm resistor.   |
| VDD12_FB  | 102                                | TBD. Pull down with 1K Ohm resistor.   |

## 8. Function Description

### 8.1. Reset

#### 8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse will be generated and the RTL8366/RTL8369 will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the RESET# signal.
- Auto load the configuration from EEPROM if EEPROM is detected (approx. 8ms).
- Complete the embedded SRAM BIST process.
- Initialize the packet buffer descriptor allocation.
- Initialize the internal registers and prepare them to be accessed by the external CPU.
- Start MDC/MDIO configuration and polling.

*Note 1: To guarantee register access is valid and correct, the RTL8366/RTL8369 registers should not be accessed before the reset initialization process is finished.*

*Note 2: The connected PHY should have completed the reset process before the RTL8366/RTL8369 starts the MDC/MDIO configuration and polling process.*

#### 8.1.2. Software Reset

The RTL8366/RTL8369 supports two software resets; a chip reset and a soft reset.

##### CHIP\_RESET

When CHIP\_RESET in Register RCR (0x0100) is set to 0b1 (write and self clear), the chip will make the following steps:

1. Download configuration from strap pin and EEPROM.
2. Start embedded SRAM BIST (Built-In Self Test).
3. Clear all the Lookup and VLAN tables.
4. Reset all registers to default values.
5. Restart auto-negotiation process.

## SOFT\_RESET

When set SOFT\_RESET in Register RCR (0x0100) is set to 0b1 (write and self clear), the chip will complete the following steps:

1. Restart the auto-negotiation process.
2. Clear the FIFO and re-start packet buffer link list.

## 8.2. 802.3x Full Duplex Flow Control

The RTL8366/8369 supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, depends on the result of NWay.
- When Auto-Negotiation is disabled, depends on the register PAACR0-4 (0x0011~ 0x0015), PORT\_ABILITY<sub>n</sub>[7:6] (n: 0 - 8).

The RTL8366/8369 supports asymmetrical flow control in 1000Mbps mode. The Auto-Negotiation module checks the flow control ability of the PHY MII register 4, 9 and those of its link partner to resolve the flow control mode. The following shows the flow control resolution truth table.

**Table 10. Flow Control Resolution Truth Table**

| Local Device |            | Link Partner |            | Local Device Resolution                        | Local Partner Resolution                       |
|--------------|------------|--------------|------------|--|--|
| PAUSE        | ASM_DIR    | PAUSE        | ASM_DIR    |  |  |
| 0            | 0          | Irrelevant   | Irrelevant | Disable PAUSE<br>Transmit and Receive          | Disable PAUSE<br>Transmit and Receive          |
| 0            | 1          | 0            | Irrelevant | Disable PAUSE<br>Transmit and Receive          | Disable PAUSE<br>Transmit and Receive          |
| 0            | 1          | 1            | 0          | Disable PAUSE<br>Transmit and Receive          | Disable PAUSE<br>Transmit and Receive          |
| 0            | 1          | 1            | 1          | Enable PAUSE Transmit<br>Disable PAUSE Receive | Enable PAUSE Receive<br>Disable PAUSE Transmit |
| 1            | 0          | 0            | Irrelevant | Disable PAUSE<br>Transmit and Receive          | Disable PAUSE<br>Transmit and Receive          |
| 1            | Irrelevant | 1            | Irrelevant | Enable PAUSE<br>Transmit and Receive           | Enable PAUSE<br>Transmit and Receive           |
| 1            | 1          | 0            | 0          | Disable PAUSE<br>Transmit and Receive          | Disable PAUSE<br>Transmit and Receive          |
| 1            | 1          | 0            | 1          | Enable PAUSE Receive<br>Disable PAUSE Transmit | Enable PAUSE Transmit<br>Disable PAUSE Receive |

The results of flow control negotiation are shown in registers PSR0-4 (0x0159~ 0x015D), PORT\_STATUS<sub>n</sub>[5], and PORT\_STATUS<sub>n</sub>[4] (n: 0: 8).

### 8.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called “truncated binary exponential backoff”. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slotTime (512 bit times). The number of slot times to delay before the  $n^{\text{th}}$  retransmission attempt is chosen as a uniformly distributed random integer ‘r’ in the range:

$$0 \leq r < 2^k$$

where:

$k = \min(n, \text{backoffLimit})$ . The backoffLimit for the RTL8366/RTL8369 is 9.

The half duplex back-off algorithm in the RTL8366/RTL8369 does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

Two types of half duplex flow control are supported: BACK-PRESSURE and DEFER mode. Register SGCR (0x0000), bit 9 JAM\_MODE=0b0 is used Enables BACK-PRESSURE mode. Set JAM\_MODE=0b1 Enables DEFER mode (default).

#### 8.3.1. BACK-PRESSURE Mode (JAM\_MODE=0b0)

In BACK-PRESSURE mode, the RTL8366/8369 sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. Set Register SGCR (0x0000), bit 10, EN\_48PASS1=0b1 to receive one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

### **8.3.2. DEFER Mode (JAM\_MODE=0b1)**

DEFER is to assert the TXEN signal for 2K bytes in order to make the link partner back-off. The IPG between two asserted TXEN is 56 bits. When congestion control is activated on the ingress port, the RTL8366/RTL8369 will send a 4-byte jam pattern at the first incoming packet. The link partner will back-off and wait to re-try. The RTL8366/RTL8369 will start the DEFER signal 56 bits after the link partner starts to back-off.

## ***8.4. Search and Learning***

When a packet is received, the RTL8366/RTL8369 uses the least 12 bits of the destination MAC address to search the 4K-entry look-up table. This is the “Address Search”. If the destination MAC address is not found, the switch will broadcast the packet.

The RTL8366/RTL8369 then extracts the least 12 bits of the source MAC address to index the 4K-entry look-up table. If the entry is not already in the table it will record the source MAC address and add switching information. If this is an occupied entry, it will update the entry with new information. This is called “Learning”.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if it’s time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8366/RTL8369 is between 200 and 400 seconds (typical is 300 seconds).

The 4K-entry look-up table could be read/write via indirect register access by external CPU. The detailed look-up table access method is described in section 8.17 Look-up Table and VLAN Table Access, page 36.

## ***8.5. Illegal Frame Filtering***

Illegal frames such as CRC error packets, runt packets (length < 64 bytes) and oversize packets (length > maximum length) will be discarded by the RTL8366/RTL8369. The maximum packet length may be 1522, 1536, 1552, or 9216 bytes. This function is controlled by MAX\_LENGTH[1:0] in Register SGCR (0x0000).

## ***8.6. IEEE 802.1D Reserved Group Addresses Filtering Control***

The RTL8366/RTL8369 supports the ability to drop/forward 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-04 to 01-80-C2-00-00-0F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered. MAC address 01-80-C2-00-00-03 is always forwarded. This function is controlled by pin strapping of EN\_MLT\_FWD (pin 32) upon power on reset. After power on, the configuration may be changed via MLTID\_ST[15:0][1:0] in Register MCPCR0-1 (0x000F – 0x0010).

## ***8.7. Realtek Remote Control Protocol***

TBD

## ***8.8. Broadcast Storm Control***

The RTL8366/RTL8369 enables or disables broadcast storm control by setting EN\_BC\_STORM\_CTRL in Register SGCR (0x0000). The default is enabled. After 64 consecutive broadcast packets (DA=FF-FF-FF-FF-FF-FF) are received by a particular port, the following incoming broadcast packets will be discarded by this port for approximately 800ms. Any non-broadcast packet can reset the time window and broadcast counter such that the scheme restarts.

*Note: Trigger condition: consecutive DA=FF-FF-FF-FF-FF-FF packets. Release condition: receive non-broadcast packet on or after 800ms.*

## 8.9. MIB counter

The RTL8366/RTL8369 implement three 32-bit statistic counters for each port.

- MIB<sub>n</sub>\_SELA[1:0] in Register MCCR0-4 (0x0038~ 0x003C), n=0-8: Counter select for Port n in counter set A.
  - 0b00: TX byte count
  - 0b01: TX packet count (Default)
- MIB<sub>n</sub>\_SELB[1:0] in Register MCCR0-4 (0x0038~ 0x003C), n=0-8: Counter select for Port n in counter set B.
  - 0b00: RX byte count
  - 0b01: RX packet count (Default)
- MIB<sub>n</sub>\_SELC[1:0] in Register MCCR0-4 (0x0038~ 0x003C), n=0-8: Counter select for Port n in counter set C.
  - 0b00: RX error packet count (Default)
  - 0b01: RX drop packet count
  - 0b10: Collision count
- MIB<sub>n</sub>\_CNTA[31:0] in Register PnMIB\_CNTA, n=0-8: Counter set A.
- MIB<sub>n</sub>\_CNTB[31:0] in Register PnMIB\_CNTB, n=0-8: Counter set B.
- MIB<sub>n</sub>\_CNTC[31:0] in Register PnMIB\_CNTC, n=0-8: Counter set C.

The TX/RX packet/byte counter only counts forwarded packets. A read access of the MIB counter will *NOT* reset the counter to 0. The 32-bit counter is a continuous repeat counter that is set to zero only when powered-on, MIB\_RESET in Register RCR (0x0100) is asserted, an overflow occurs, or a change is made to MIB<sub>n</sub>\_SELA[1:0], MIB<sub>n</sub>\_SELB[1:0], MIB<sub>n</sub>\_SELC[1:0] registers.



## 8.10. Port Mirroring

The RTL8366/RTL8369 supports one set of port mirroring functions for all 6/9 ports. User could monitor both the TX and RX packets of the source port from a mirror port. The source port to be mirrored can be selected in SOURCE\_PORT[3:0] in Register PMCR (0x0007). The monitor port can be selected in MONITOR\_PORT[3:0] in Register PMCR (0x0007).

MIRROR\_TX and MIRROR\_RX in Register PMCR (0x0007) are used to select the TX or RX packets of the source port to be mirrored. If MIRROR\_ISO in Register PMCR (0x0007) is enabled, the monitor port only forwards the TX or RX packets of the source port. Any other packets destined for the monitor port will be dropped. When MIRROR\_SPC in Register PMCR (0x0007) is enabled, Pause packets received by the source port will be forwarded to the monitor port.

## 8.11. LEDs

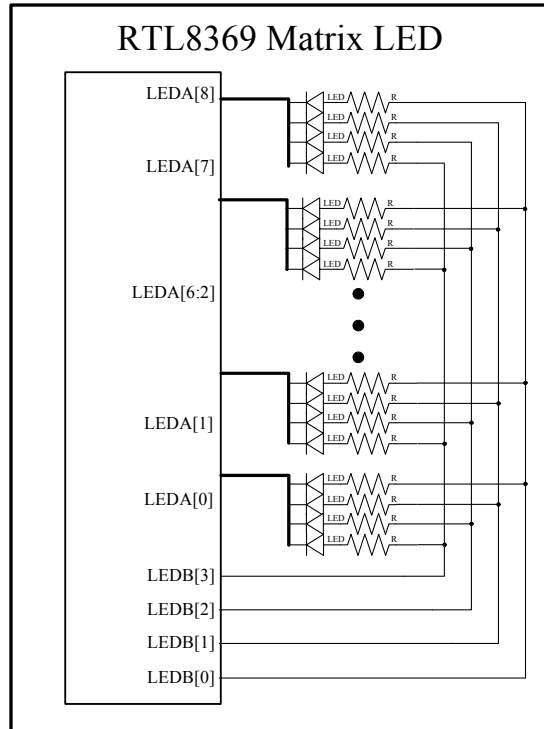
There are two types of LED mode supported in the RTL8366/RTL8369, matrix LED and serial LED. Configuration can be made by pins pulled high/low in LED\_MODE[1:0] upon power on strapping, or by setting LED\_MODE[1:0] in Register LCR0 (0x0036). Blinking enable is configured by setting LED\_RESET\_BLINK in Register LCR0 (0x0036). LED\_BLINK\_TIME in Register LCR0 (0x0036) controls the blink duration for LED on/off (43 ms or 120 ms).

### 8.11.1. Matrix LEDs

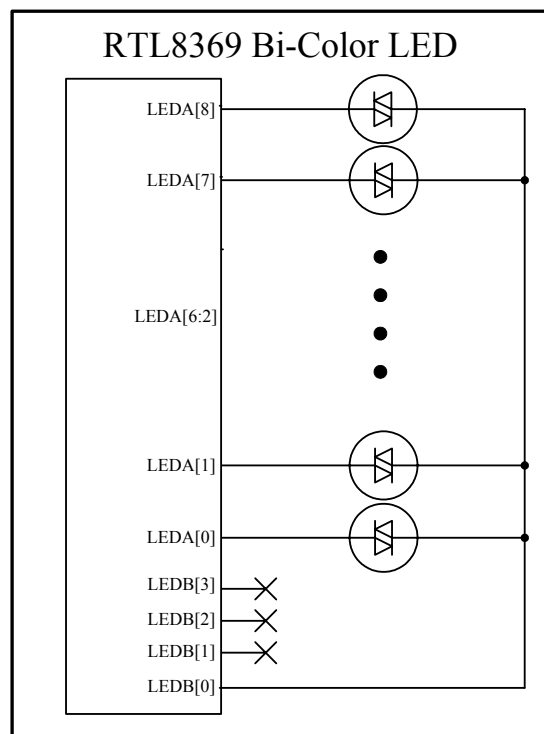
For Matrix LEDs, each port provides 4 LED indicators, LEDB[3:0]. The meaning of LEDB[3:0] is shown in Table 11.

**Table 11. LED Mode Configuration**

| LED_MODE[1:0] | Mode                    | Output LEDB[3:0] (LEDB[3], LEDB[2], LEDB[1], LEDB[0])   |
|---------------|-------------------------|---|
| 0b00          | 4-bit for matrix stream | 100M/10M, 1000M, LINK/ACT, DUPLEX/COL                   |
| 0b01          | 4-bit for matrix stream | 10M LINK/ACT, 100M LINK/ACT, 1000M LINK/ACT, DUPLEX/COL |
| 0b10          | Bi-color LED            | NC, NC, NC, (1000M+Link/Act, 100M/10M+Link/ACT)         |
| 0b11          | 4-bit for serial stream | Serial LED Mode   |



**Figure 9. Matrix LED Interconnections**



**Figure 10. Bi-Color LEDs**

## 8.11.2. Serial LED Mode

TBD

## 8.12. VLAN Function

### 8.12.1. VLAN Table, Configuration, and Mapping

The RTL8369 supports 802.1Q Port-Based and Tag-Based VLAN. It supports a total of 4096 VLAN tables for smart switch applications. 16 entries of the VLAN tables can be read/written directly via register access and EEPROM configuration upon power on strapping. All 4096 VLAN tables can be read/written indirectly via register access. VLAN table access is described in more detail in section 8.17 Look-up Table and VLAN Table Access, page 36.

Registers VTCR0 and VTCR1 (0x0005 and 0x0006) are used Enables VLAN function and optional ingress and egress filtering functions. Registers VIDCR0-15 and VMCR0-15 (0x0016 – 0x0035) are used to configure the VID and Member set of the first 16 VLAN entries. Registers PVICR0-2 (0x0058 – 0x005A) are used to configure the port VLAN index of ports 0-8. Register EVTCCR (0x010F) is used Enables all 4096 VLAN tables.

### 8.12.2. VLAN Configuration Mode 1 (Port-Based VLAN Application)

VLAN Configuration Mode 1 configures EN\_VLAN in Register VTCR0 (0x0005) as 0b1. The default VLAN membership configuration by internal register is port 7 overlapped with port 0-6, to form 8 individual VLANs. Using an attached serial EEPROM, or via EEPROM SMI, the default configuration may be modified to permit ports to join one of the 16 VLAN groups: VLAN 0-15.

**Table 12. PVID of Each Port's Default Configuration When EN\_VLAN=0b1**

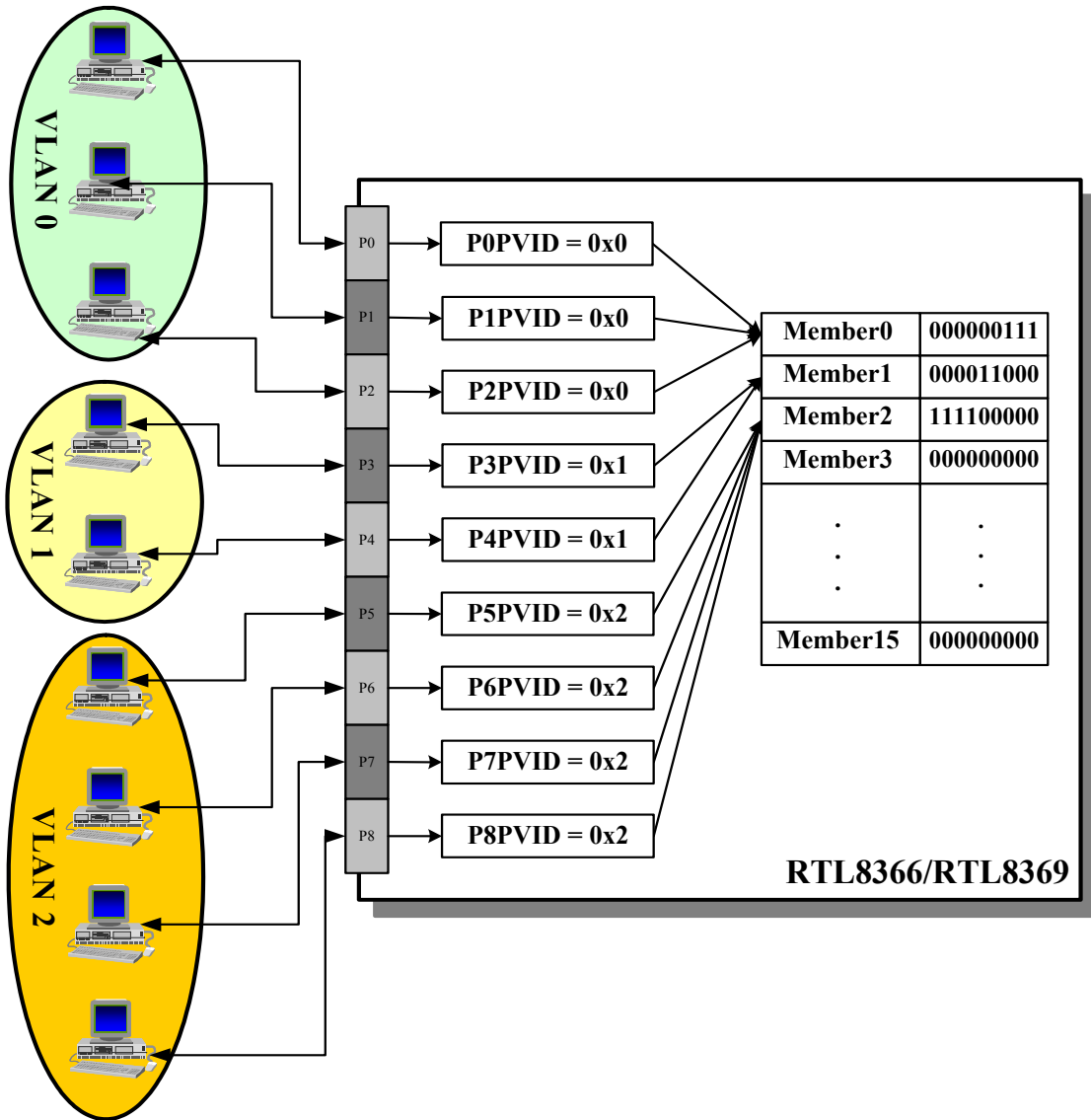
| Port Num | Register PVICR0-2 | Default Value | Notes                 |
|----------|-------------------|---------------|-----------------------|
| 0        | P0PVID[3:0]       | 0x0           | Index to VLAN group 0 |
| 1        | P1PVID[3:0]       | 0x1           | Index to VLAN group 1 |
| 2        | P2PVID[3:0]       | 0x2           | Index to VLAN group 2 |
| 3        | P3PVID[3:0]       | 0x3           | Index to VLAN group 3 |
| 4        | P4PVID[3:0]       | 0x4           | Index to VLAN group 4 |
| 5        | P5PVID[3:0]       | 0x5           | Index to VLAN group 5 |
| 6        | P6PVID[3:0]       | 0x6           | Index to VLAN group 6 |
| 7        | P7PVID[3:0]       | 0x7           | Index to VLAN group 7 |
| 8        | P8PVID[3:0]       | 0x8           | Index to VLAN group 8 |

**Table 13. Member Set of Each VLAN Group Default Configuration When EN\_VLAN=0b1**

| VLAN Group | Register VMCR0-15 | Default | Register VIDCR0-15 | Default | Notes                         |
|------------|-------------------|---------|--------------------|---------|-------------------------------|
| 0          | Member0[3:0]      | 0x81    | VID0[11:0]         | 0x100   | Member={Port 0, 7}, VID=0x100 |
| 1          | Member1[3:0]      | 0x82    | VID1[11:0]         | 0x101   | Member={Port 1, 7}, VID=0x100 |
| 2          | Member2[3:0]      | 0x84    | VID2[11:0]         | 0x102   | Member={Port 2, 7}, VID=0x100 |
| 3          | Member3[3:0]      | 0x88    | VID3[11:0]         | 0x103   | Member={Port 3, 7}, VID=0x100 |
| 4          | Member4[3:0]      | 0x90    | VID4[11:0]         | 0x104   | Member={Port 4, 7}, VID=0x100 |
| 5          | Member5[3:0]      | 0xA0    | VID5[11:0]         | 0x105   | Member={Port 5, 7}, VID=0x100 |
| 6          | Member6[3:0]      | 0xC0    | VID6[11:0]         | 0x106   | Member={Port 6, 7}, VID=0x100 |
| 7          | Member7[3:0]      | 0xFF    | VID7[11:0]         | 0x107   | Member={All Ports}, VID=0x100 |
| 8          | Member8[3:0]      | 0x00    | VID8[11:0]         | 0x000   | Member={None}, VID=0x000      |
| 9          | Member9[3:0]      | 0x00    | VID9[11:0]         | 0x000   | Member={None}, VID=0x000      |
| 10         | Member10[3:0]     | 0x00    | VID10[11:0]        | 0x000   | Member={None}, VID=0x000      |
| 11         | Member11[3:0]     | 0x00    | VID11[11:0]        | 0x000   | Member={None}, VID=0x000      |
| 12         | Member12[3:0]     | 0x00    | VID12[11:0]        | 0x000   | Member={None}, VID=0x000      |
| 13         | Member13[3:0]     | 0x00    | VID13[11:0]        | 0x000   | Member={None}, VID=0x000      |
| 14         | Member14[3:0]     | 0x00    | VID14[11:0]        | 0x000   | Member={None}, VID=0x000      |
| 15         | Member15[3:0]     | 0x00    | VID15[11:0]        | 0x000   | Member={None}, VID=0x000      |

Taking Figure 11 as an example, P0PVID~P2PVID are 0x0, P3PVID and P4PVID are 0x1, and P5PVID~P8PVID are 0x2. This means Port 0 to 2 belong to VLAN 0, Port 3 and Port 4 belong to VLAN 1, and Ports 5 to 8 belong to VLAN 2.

Member0=000000111 means Ports 0 to 2 are members of VLAN 0 and packet ingress from any of these ports could only be forwarded to these ports. Member1=000011000 means Port 3 and Port 4 are members of VLAN 1 and packet ingress from any of these ports can only be forwarded to these ports. Member2=111100000 means Ports 5 to 8 are members of VLAN 2 and packet ingress from any of these ports can only be forwarded to these ports. If packets ingress from Port 0 and the destination port is Port 3 (searched according to the DA of the packet), the switch will drop the packets.



**Figure 11. Port-Based VLAN Application Example**

### 8.12.3. VLAN Configuration Mode 2 (802.1Q 16 VLAN Entries Application)

802.1Q tagged-VID based VLAN mapping uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. Sixteen groups of VLAN membership registers,  $Member0[8:0] \sim Member15[8:0]$  (0x0017/0x0019/.../0x0035), consist of ports that are in the same VLAN corresponding to the registers defined in  $VID0[11:0] \sim VID15[11:0]$  (0x0016/0x0018/.../0x0034). If the VID of a VLAN-tagged frame does not hit  $VID0[11:0] \sim VID15[11:0]$ , then the frame will be dropped by the RTL8366/RTL8369. Otherwise, the RTL8366/RTL8369 compares the explicit identifier in the VLAN tag with the 16 VLAN registers to determine the VLAN association of this frame, then forwards it to the member set of this VLAN. Two VIDs are reserved for special purposes. One of them is all ones and is reserved and currently unused. The other is all zeros and indicates a priority tag, which is treated as an untagged frame. When `VLAN_TAG_AWARE` in Register `VTCR0` (0x0005) is enabled, the RTL8366/RTL8369 performs 802.1Q tag based VLAN mapping for tagged frames, but performs port-based VLAN mapping for untagged frames. If `VLAN_TAG_AWARE` is disabled, the RTL8366/RTL8369 performs only port-based VLAN mapping both for non-tagged and tagged frames. Figure 12 illustrates the processing flow when `VLAN_TAG_AWARE` is enabled.

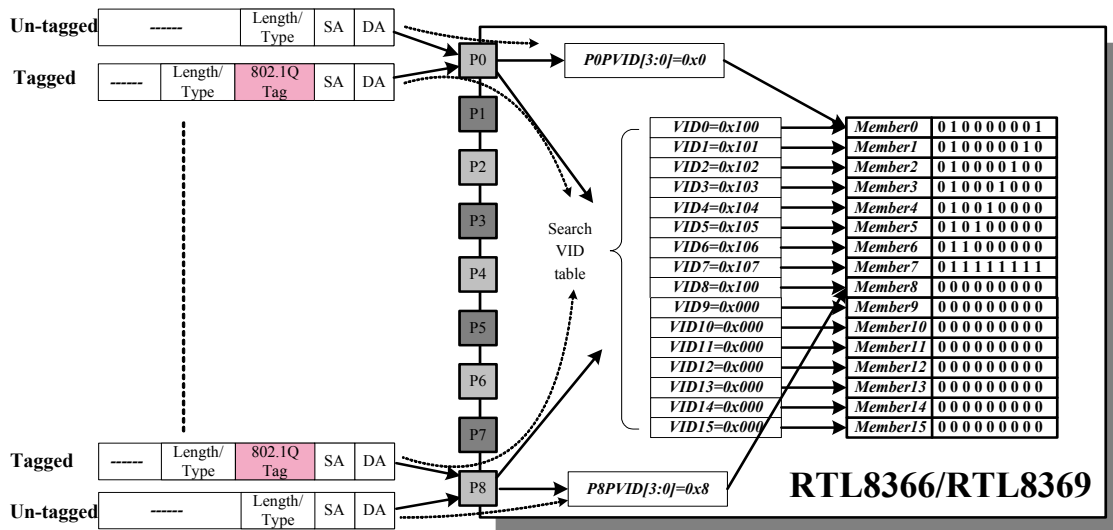


Figure 12. Tagged/Untagged Packet Forwarding When `VLAN_TAG_AWARE` is Enabled

### 8.12.4. VLAN Configuration Mode 3 (802.1Q 4096 VLAN Entries Application)

The RTL8366/RTL8369 supports 4096 VLAN entries by setting EN\_VLAN\_TBL in Register EVTCR (0x010F) as 0b1. VID[11:0] of each VLAN is the same as the index of each entry in the table. For example, the VID[11:0]=0x100 is the 256th entry in the VLAN table. The VLAN table format is shown in Figure 13.

| Entry | VID[11:0] | Member[8:0]     |
|-------|-----------|-----------------|
| 0     | 0x000     | Reserved        |
| 1     | 0x001     | 0 0 0 0 0 0 0 0 |
| 2     | 0x002     | 0 0 0 0 0 0 0 0 |
| ...   | ...       | ...             |
| ...   | ...       | ...             |
| ...   | ...       | ...             |
| ...   | ...       | ...             |
| 4093  | 0xFFD     | 0 0 0 0 0 0 0 0 |
| 4094  | 0xFFE     | 0 0 0 0 0 0 0 0 |
| 4095  | 0xFFF     | Reserved        |

4096  
VLAN  
Entry

**Figure 13. 4096 VLAN Table Format**

When 4096 VLAN tables are enabled, for Port-Based VLAN forwarding, VID<sub>n</sub>[11:0] of VLAN group *n* (n=0-8) are used to point to the entry of the 4096 VLAN tables.

P<sub>n</sub>PVID[3:0] are fixed as 0xn (n=0-8), and should not be changed when EN\_VLAN\_TBL=0b1. For example, P0PVID[3:0]=0x0 and VID0[11:0]=0x100 means the PVID of P0 is 0x100. The member set configuration depends on the setting at entry 256 in the VLAN table. The Member0[8:0] in Register VMCR0 (0x0017) is not used when EN\_VLAN\_TBL=0b1.

**Table 14. PVID of Each Port Configuration When EN\_VLAN=0b1 and EN\_VLAN\_TBL=0b1**

| Port Num | Register PVICR0-2 | Default Value | Note   |
|----------|-------------------|---------------|--|
| 0        | P0PVID[3:0]       | 0x0           | Index to the VID entry of VLAN group 0   |
| 1        | P1PVID[3:0]       | 0x1           | Index to the VID entry of VLAN group 1   |
| 2        | P2PVID[3:0]       | 0x2           | Index to the VID entry of VLAN group 2   |
| 3        | P3PVID[3:0]       | 0x3           | Index to the VID entry of VLAN group 3   |
| 4        | P4PVID[3:0]       | 0x4           | Index to the VID entry of VLAN group 4   |
| 5        | P5PVID[3:0]       | 0x5           | Index to the VID entry of VLAN group 5<br><i>Not supported in the RTL8366.</i> |
| 6        | P6PVID[3:0]       | 0x6           | Index to the VID entry of VLAN group 6<br><i>Not supported in the RTL8366.</i> |

| Port Num | Register PVICR0-2 | Default Value | Note   |
|----------|-------------------|---------------|--|
| 7        | P7PVID[3:0]       | 0x7           | Index to the VID entry of VLAN group 7<br><i>Not supported in the RTL8366.</i> |
| 8        | P8PVID[3:0]       | 0x8           | Index to the VID entry of VLAN group 8   |

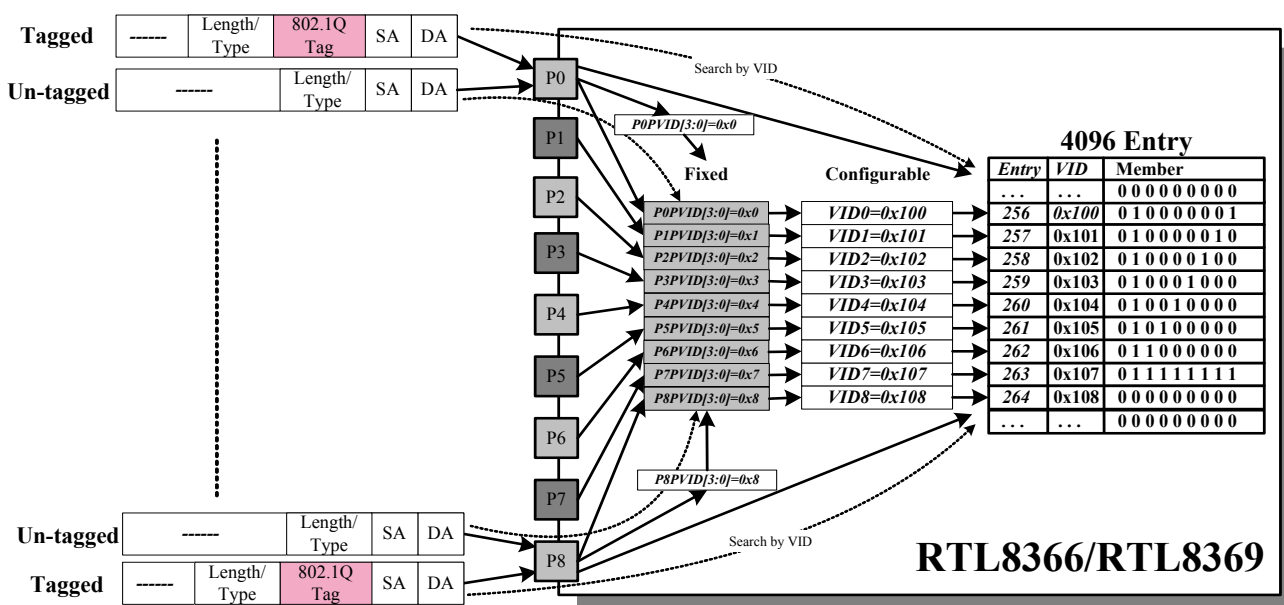
When 4096 VLAN tables are enabled, for 802.1Q Tag-Based VLAN forwarding, the RTL8366/RTL8369 use the VID in the tagged packet to search the VID<sub>n</sub>[11:0] of each VLAN table.

### No Match

If the VID of the tagged packet does not match any VID<sub>n</sub>[11:0] of all the valid VLAN tables, the packet is dropped by the switch.

### Match

If the VID of the tagged packet matches the VID<sub>n</sub>[11:0] of a valid VLAN entry, the packet is forwarded according to the DA Search result and member set of the VLAN entry.



**Figure 14. Tagged/Untagged Packet Forwarding When VLAN\_TAG\_AWARE and EN\_VLAN\_TBL are Enabled**



### 8.12.5. VLAN Ingress and Egress Rules

The RTL8366/RTL8369 support three VLAN ingress-filtering controls. These filtering functions can be enabled or disabled by register access or EEPROM configuration. All of these functions are disabled by default.

- **VLAN\_TAG\_ADMIT** (VLAN Tag Admit Control): enables receiving only VLAN-tagged frames. Untagged frames or priority tagged frames (VID=0) will be dropped by the RTL8366/RTL8369.
- **EN\_INGRESS\_RULE** (Ingress Member Set Filtering Control): enables dropping of frames if the receiving port is not in the member set for the frame's VLAN classification VID.
- **EN\_TAG\_DROP** (VLAN Tag Drop Control): drops all VLAN-tagged frames and receives all other untagged frames or priority tagged frames (VID=0).

The RTL8366/RTL8369 supports 3 VLAN egress VLAN leaky controls. These leaky rules have higher priority than VLAN egress rules (the destination port need not be a member of the VLAN table).

- **EN\_UC\_LEAKY** (Unicast VLAN Leaky Control): Enables inter-VLAN unicast packet forwarding.
- **EN\_ARP\_LEAKY** (ARP Packet VLAN Leaky Control): Enables RP packets (DA=FF-FF-FF-FF-FF-FF and Ether-Type=0x0806) to forward to all the other ports ignoring the egress rule. *EN\_ARP should be enabled (Register SGCR, 0x0000, bit 7) before enabling the EN\_ARP\_LEAKY function.*
- **EN\_IPMC\_LEAKY** (IP Multicast Packet VLAN Leaky Control): Enables IP Multicast packets to forward to all the other ports ignoring the egress rule. *EN\_IGMP should be enabled (Register SGCR, 0x0000, bit 6) before enabling the EN\_IPMC\_LEAKY function.*

### 8.12.6. VLAN Tagging/Un-Tagging

Per-Port Output tag/untag control: Four types of output VLAN tagging control are supported, controlled by Register VTCR0-1 (0x0005 and 0x0006),  $P_n\_TAG\_CONTROL[1:0]$ ,  $n=0: 8$ .

- 0b00: Keeps all packets unchanged.
- 0b01: Inserts a VLAN tag according to the PVID of the ingress port.
- 0b10: Removes VLAN-tags from frames.
- 0b11: Inserts a priority tag according to the priority of the packet.

If the VLAN tag removed frame is less than 64 bytes, the RTL8369 will add '0x20' as load padding before the CRC field.

## **8.13. QOS**

There are two priority queues supported in the RTL8366/RTL8369, and 3 types of priority classification. The queue service rate is based on the Weighted Round Robin algorithm, the packet-based service weight ratio of the high-priority queue and low-priority queue can be set to 4:1, 8:1, 16:1, or 'Always high priority first'. The ratio can be selected by QWEIGHT[1:0] in Register QCR0 (0x0009). The 3 types of priority classification are Port-based, Differentiated Service-based, and 802.1Q VLAN tag-based.

### **8.13.1. Port-Based Priority**

Port-based priority is enabled via EN\_PORT\_PRI in Register QCR0 (0x0009). Configuring PORT\_PRI[8:0] as 0b1 in Register QCR1 (0x000A) forces incoming packets at the ingress port to be high priority. When port-based priority is applied, any packet received from a high priority port will be treated as a high priority packet.

### **8.13.2. IEEE 802.1p/Q-Based Priority**

IEEE 802.1p/Q-based priority is enabled via EN\_1Q\_PRI in Register QCR0 (0x0009). When 802.1p tag priority is applied, the RTL8366/RTL8369 recognizes 802.1Q VLAN tagged packets and extracts the 3-bit User Priority information from the VLAN tag. The RTL8366/RTL8369 sets the User Priority threshold to 3. VLAN tagged packets with User Priority values 4~7 are treated as high priority packets, and other User Priority values (0~3) as low priority packets (follows the IEEE 802.1p standard).

### 8.13.3. Differentiated Service Based Priority

Differentiated Service-based priority function is enabled by EN\_DS\_PRI in Register QCR0 (0x0009). When TCP/IP's TOS/DiffServ (DS) based priority is applied, the RTL8366/RTL8369 recognizes TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined in RFC2474. The DS field byte for IPv4 is the Type-of-Service (TOS) octet. Recommended DiffServ Codepoints are defined in RFC2597 for classifying traffic into different service classes. The RTL8366/RTL8369 extracts the codepoint value of the DS field from IPv4 packets and identifies the priority of the incoming IP packet following the definitions by TOS[63:0] in Register QCR2-5 (0x000B – 0x000E). For example, if TOS[5] = 0b1 means TOS[5:0] = 0b000101

**Table 15. IPv4 Frame Format**

| 6 bytes | 6 bytes | 4 bytes               | 2 bytes | 4 bits             | 4 bits | 6 bits             | 2 bits |      | 4 bytes |
|---------|---------|-----------------------|---------|--------------------|--------|--------------------|--------|------|---------|
| DA      | SA      | 802.1Q Tag (Optional) | 08-00   | Version IPv4: 0100 | IHL    | TOS[0:5]: DS-field | ----   | Data | CRC     |

**Table 16. IPv6 Frame Format**

| 6 bytes | 6 bytes | 4 bytes               | 2 bytes | 4 bits             | 6 bits             | 2 bits |      | 4 bytes |
|---------|---------|-----------------------|---------|--------------------|--------------------|--------|------|---------|
| DA      | SA      | 802.1Q Tag (Optional) | 08-DD   | Version Ipv6: 0110 | TOS[0:5]: DS-field | ----   | Data | CRC     |

## 8.14. Port Property Configuration

The RTL8366/RTL8369 can configure the NWay ability of the RTL8212 via EEPROM upon power on strapping. In Register PAACR0-4 (0x0011~ 0x0015), PORT\_ABILITY $n$ [7:0] are used to configure the NWay ability in the RTL8212 MII register when Auto-Negotiation is enabled. When Auto-Negotiation is disabled, the 'Forced parameter' forces the port to a particular defined status. The port ability is written to PHY register 4 and 9 upon power on reset. The register mapping of PORT\_ABILITY $n$ [7:0],  $n=0: 8$ , is shown in Table 17.

**Table 17. Port Ability Register**

| Name                 | Asymmetric Flow Control | Flow Control | 1000 Full | 100 Full | 100 Half | 10 Full  | 10 Half  | Auto-Negotiation |
|----------------------|-------------------------|--------------|-----------|----------|----------|----------|----------|------------------|
| Bit                  | 7                       | 6            | 5         | 4        | 3        | 2        | 1        | 0                |
| RTL8212 MII Register | Reg.4[11]               | Reg.4[10]    | Reg.9[9]  | Reg.4[8] | Reg.4[7] | Reg.4[6] | Reg.4[5] | Reg.0[12]        |

## 8.15. Spanning Tree Status Register

The RTL8366 and RTL8369 support a Spanning Tree status register PnSTS[1:0]. When the system supports the spanning tree function, a CPU or RISC must be present. All ports behave according to PnSTS[1:0]. The CPU determines the state of the ports according to BPDU, then updates the SPS to control the port behavior. The CPU port should carry the ingress port number of the receiving BPDU. The port state behavior is shown in Table 18.

**Table 18. Spanning Tree Status: Port State Behavior**

| PnSTS[1:0]        | Receive BPDU | Transmit BPDU | Learn Address | Forward Data Frames |
|-------------------|--------------|---------------|---------------|---------------------|
| Blocking (0b00)   | V            | X             | X             | X                   |
| Listening (0b01)  | V            | V             | X             | X                   |
| Learning (0b10)   | V            | V             | V             | X                   |
| Forwarding (0b11) | V            | V             | V             | V                   |

## 8.16. PHY MII Register Access

The RTL8366 and RTL8369 provide an external CPU with an indirect access interface to change the PHY MII register configuration. In Register PHYACR0-4 (0x0118 – 0x011C), the PHY address, Register address, Input data, and Read/Write commands can be configured.

### 8.16.1. PHY MII Register Read Access

1. Configure PHY\_ADDR[4:0] in Register PHYACR1 (0x0119).
2. Configure PHY\_REG[4:0] in Register PHYACR2 (0x011A).
3. Configure PHY\_EXEC=0b1 and PHY\_RW=0b0 in Register PHYACR0 (0x0118).
4. When PHY\_EXEC=0b0 in Register PHYACR0, read the data from PHY\_DATA\_IN[15:0] in Register PHYACR3 (0x011B).

### 8.16.2. PHY MII Register Write Access

1. Configure PHY\_ADDR[4:0] in Register PHYACR1 (0x0119).
2. Configure PHY\_REG[4:0] in Register PHYACR2 (0x011A).
3. Configure PHY\_DATA\_OUT[15:0] in Register PHYACR4 (0x011C).
4. Configure PHY\_EXEC=0b1 and PHY\_RW=0b1 in Register PHYACR0 (0x0118).
5. When PHY\_EXEC=0b0 in Register PHYACR0, the switch is finished write access to the PHY MII register.

## 8.17. Look-up Table and VLAN Table Access

The RTL8366/RTL8369 support indirect access to the 4K-entry lookup tables and 4K VLAN tables by external CPU or RISC. TABLE\_EXEC in Register LVTACR (0x0180) is used to start the access command, and TABLE\_CMD[2:0] is used to select the access method. WD[69:0] in Register LVTDIR0-4 (0x0182 – 0x0186) is the data input buffer, which is used to input specific Lookup table or VLAN table entry information. RD[47:0] in Register LVTDOR0-2 (0x0188 – 0x018A) is the data output buffer, which is the output information after access has completed.

**Table 19. Data Input/Output Buffer Format and Register Mapping**

|               |               |               |
|---------------|---------------|---------------|
| LVTDOR2[15:0] | LVTDOR1[15:0] | LVTDOR0[15:0] |
| RD[47:32]     | RD[31:16]     | RD[15:0]      |

|              |               |               |               |               |
|--------------|---------------|---------------|---------------|---------------|
| LVTDIR4[5:0] | LVTDIR3[15:0] | LVTDIR2[15:0] | LVTDIR1[15:0] | LVTDIR0[15:0] |
| WD[69:48]    | WD[63:48]     | WD[47:32]     | WD[31:16]     | WD[15:0]      |



**Table 21. Summary Format for Lookup and VLAN Table Access Output Data buffer (RD[47:0])**

|                |               |               |               |             |               |           |               |               |               |               |               |             |    |    |    |    |
|----------------|---------------|---------------|---------------|-------------|---------------|-----------|---------------|---------------|---------------|---------------|---------------|-------------|----|----|----|----|
| RD[47:32]      | 47            | 46            | 45            | 44          | 43            | 42        | 41            | 40            | 39            | 38            | 37            | 36          | 35 | 34 | 33 | 32 |
| Uni-cast Read  | Reserved      |               |               | Fail        | Fixed         | Multicast | Aging[1:0]    |               | SPA[3:0]      |               |               | MAC_B3[7:4] |    |    |    |    |
| Multicast Read | Reserved      |               |               | Fail        | Fixed         | Multicast | P8_Aging[1:0] | P7_Aging[1:0] | P6_Aging[1:0] | P5_Aging[1:0] | P4_Aging[1:0] |             |    |    |    |    |
| VLAN Read      | Reserved      |               |               |             |               |           |               |               |               |               |               |             |    |    |    |    |
| RD[31:16]      | 31            | 30            | 29            | 28          | 27            | 26        | 25            | 24            | 23            | 22            | 21            | 20          | 19 | 18 | 17 | 16 |
| Uni-cast Read  | MAC_B3[3:0]   |               |               | MAC_B4[7:0] |               |           |               |               |               |               | MAC_B5[7:4]   |             |    |    |    |    |
| Multicast Read | P3_Aging[1:0] | P2_Aging[1:0] | P1_Aging[1:0] |             | P0_Aging[1:0] |           | Reserved      |               |               |               |               |             |    |    |    |    |
| VLAN Read      | Reserved      |               |               |             |               |           |               |               |               |               |               |             |    |    |    |    |
| RD[15:0]       | 15            | 14            | 13            | 12          | 11            | 10        | 9             | 8             | 7             | 6             | 5             | 4           | 3  | 2  | 1  | 0  |
| Uni-cast Read  | MAC_B5[3:0]   |               |               | MAC_B2[7:0] |               |           |               |               |               |               | MAC_B1[7:4]   |             |    |    |    |    |
| Multicast Read | Reserved      |               |               | MAC_B2[7:0] |               |           |               |               |               |               | MAC_B1[7:4]   |             |    |    |    |    |
| VLAN Read      | Reserved      |               |               |             |               |           |               | Member[8:0]   |               |               |               |             |    |    |    |    |

### 8.17.1. Look-Up Table Read Access Method (Unicast)

The standard MAC address format is shown in Table 22. For example, the DA of a Pause packet is 01-80-C2-00-00-01. That means Byte5=0x01, Byte4=0x80, Byte3=0xC2, Byte2=0x00, Byte1=0x00, and Byte0=0x01.

**Table 22. MAC Address Format**

|        | MAC Address |   |   |   |   |   |   | Pause DA |    |
|--------|-------------|---|---|---|---|---|---|----------|----|
| Byte 5 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0        | 01 |
| Byte 4 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0        | 80 |
| Byte 3 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0        | C2 |
| Byte 2 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0        | 00 |
| Byte 1 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0        | 00 |
| Byte 0 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0        | 01 |

For Lookup Table read access, we need to input the entry number of a specific table. The WD[63:0] (LVTDIR0-3) format is shown in Table 23. After inputting the lookup table read access command (TABLE\_CMD[2:0]=0b000 and TABLE\_EXEC=0b1), the returned data will be shown in RD[47:0] (LVTDIR0-2) (see Table 24). Other reserved and un-defined bits in WD[63:0] (LVTDIR0-3) must=0b0.

**Table 23. Data Input Buffer (WD[63:0]) Format for Lookup Table Read Access**

|        | MAC Address     | Write Data[47:0] | Example |
|--------|-----------------|------------------|---------|
| Byte 5 | 7 6 5 4 3 2 1 0 |                  |         |
| Byte 4 | 7 6 5 4 3 2 1 0 |                  |         |
| Byte 3 | 7 6 5 4 3 2 1 0 |                  |         |
| Byte 2 | 7 6 5 4 3 2 1 0 |                  |         |
| Byte 1 | 7 6 5 4 3 2 1 0 | WD[35:32]        | 0xA     |
| Byte 0 | 7 6 5 4 3 2 1 0 | WD[47:40]        | 0xBC    |

**Table 24. Data Output Buffer (RD[47:0]) Format for Lookup Table Unicast Entry Read Access**

|        | MAC Address     | Read Data[47:0] | Example |
|--------|-----------------|-----------------|---------|
| Byte 5 | 7 6 5 4 3 2 1 0 | RD[19:12]       | 0x12    |
| Byte 4 | 7 6 5 4 3 2 1 0 | RD[27:20]       | 0x34    |
| Byte 3 | 7 6 5 4 3 2 1 0 | RD[35:28]       | 0x56    |
| Byte 2 | 7 6 5 4 3 2 1 0 | RD[11:4]        | 0x78    |
| Byte 1 | 7 6 5 4 3 2 1 0 | RD[3:0]         | 0x9     |
| Byte 0 | 7 6 5 4 3 2 1 0 |                 |         |

| Item     | Reserved  | Fail   | Fixed  | Multicast | Aging     | SPA       |
|----------|-----------|--------|--------|-----------|-----------|-----------|
| RD[47:0] | RD[47:45] | RD[44] | RD[43] | RD[42]    | RD[41:40] | RD[39:36] |
| Example  | 0b000     | 0b0    | 0b1    | 0b0       | 0b11      | 0x5       |

For example, if we want to read the lookup table entry 2748 (0xABC), then we have to configure:

- WD[35:32] (LVTDIR2[3:0])=0xA
- WD[47:40] (LVTDIR2[15:8])=0xBC
- Others=0



The MAC address read from this entry will be XX-XX-XX-XX-XA-BC. The returned data will be shown in LVTDOR0-2 in the following format:

If a fixed entry in the lookup table is 12-34-56-78-9A-BC, SPA (Source Port Address) is port 5, the return data is in RD[19:12]=0x12, RD[27:20]=0x34, RD[35:28]=0x56, RD[11:4]=0x78, and RD[3:0]=0x9. SPA is in RD[39:36]=0x5, Aging is in RD[41:40]=0b11, Multicast is in RD[42]=0, Fixed is in RD[43]=1, and Fail is in RD[44]=0.

### **8.17.2. Look-up Table Write Access Method (Unicast)**

For Lookup Table write access, we need to input the MAC address, Multicast flag, Fixed flag, SPA (Source Port Address), and Aging timer. The WD[63:0] format is shown in Table 25. After inputting the lookup table write access command (TABLE\_CMD[2:0]=0b001 and TABLE\_EXEC=0b1), the lookup table write access is finished.

For example, to configure a fixed entry with SPA as port 5 and MAC Address=12-34-56-78-9A-BC:

- Configure WD[7:0]=0x12, WD[15:8]=0x34, WD[23:16]=0x56, WD[31:24]=0x78, WD[39:32]=0x9A, and WD[47:40]=0xBC
- WD[48]=0b0 for Unicast entry
- WD[49]=0b1 for fixed entry, WD[51:50]=0b00
- WD[55:52]=0x5 for port 5
- WD[57:56]=0b11 for aging timer.
- Other reserved and un-defined bits in WD[63:0] must=0b0

**Table 25. Data Output Buffer (RD[47:0]) Format for Lookup Table Unicast Entry Read Access**

|        | MAC Address |   |   |   |   |   |   |   | Write Data[47:0] | Example |
|--------|-------------|---|---|---|---|---|---|---|------------------|---------|
| Byte 5 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | WD[7:0]          | 0x12    |
| Byte 4 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | WD[15:8]         | 0x34    |
| Byte 3 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | WD[23:16]        | 0x56    |
| Byte 2 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | WD[31:24]        | 0x78    |
| Byte 1 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | WD[39:32]        | 0x9A    |
| Byte 0 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | WD[47:40]        | 0xBC    |

| Item     | Aging     | SPA       | Reserved  | Fixed  | Multicast |
|----------|-----------|-----------|-----------|--------|-----------|
| WD[63:0] | WD[57:56] | WD[55:52] | WD[51:50] | WD[49] | WD[48]    |
| Example  | 0b11      | 0x5       | 0b00      | 0b1    | 0b0       |

When the entry is configured as fixed and enabled, aging must be configured as 0b01: 0b11 for normal searching and forwarding. If the aging of a fixed entry is configured as 0b00, then all packets with the DA=MAC Address will be broadcast to all active ports. Other port's ingress packets with the SA=MAC Address will not be learned into the lookup table.

For example, if the entry 2748 (0xABC) is configured as fixed and aging=0b00, with MAC Address=12-34-56-78-9A-BC, any packets with DA=MAC Address will be broadcast to all active ports, and ingress packets with SA=MAC Address will not be learned into the lookup table.

### 8.17.3. Look-up Table Read Access Method (Multicast)

The standard Multicast MAC address format is shown in Table 26. The DA MAC address of a Multicast packet ranges from 01-00-5E-00-00-00 to 01-00-5E-7F-FF-FF. The MAC address table consists of 25 fixed bits, and 23 configurable bits.

**Table 26. Multicast MAC Address Range and Format**

|        | MAC Address |   |   |   |   |   |   |   | DA        |
|--------|-------------|---|---|---|---|---|---|---|-----------|
| Byte 5 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x01      |
| Byte 4 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00      |
| Byte 3 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x5E      |
| Byte 2 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00-0x7F |
| Byte 1 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00-0xFF |
| Byte 0 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00-0xFF |

For Lookup Table Multicast entry read access, we need to input the entry number of a specific table. The WD[63:0] format is shown in Table 27. After inputting the lookup table read access command (TABLE\_CMD[2:0]=0b000 and TABLE\_EXEC=0b1), the returned data will be RD[47:0] as shown in Table 28. Other reserved and un-defined bits in WD[63:0] must=0b0.

**Table 27. Data Input Buffer (WD[63:0]) Format for Lookup Table Multicast Entry Read Access**

|        | MAC Address |   |   |   |   |   |   |   | Write Data[47:0] |  |           |  | Example |     |
|--------|-------------|---|---|---|---|---|---|---|------------------|--|-----------|--|---------|-----|
| Byte 5 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                  |  |           |  |         |     |
| Byte 4 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                  |  |           |  |         |     |
| Byte 3 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                  |  |           |  |         |     |
| Byte 2 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                  |  |           |  |         |     |
| Byte 1 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                  |  | WD[35:32] |  |         | 0xA |
| Byte 0 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | WD[47:40]        |  |           |  | 0xBC    |     |

**Table 28. Data Output Buffer (RD[47:0]) Format for Lookup Table Multicast Entry Read Access**

|        | MAC Address |   |   |   |   |   |   |   | Read Data[47:0] |  | Example |  |
|--------|-------------|---|---|---|---|---|---|---|-----------------|--|---------|--|
| Byte 5 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                 |  |         |  |
| Byte 4 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                 |  |         |  |
| Byte 3 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                 |  |         |  |
| Byte 2 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RD[11:4]        |  | 0x78    |  |
| Byte 1 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RD[3:0]         |  | 0x9     |  |
| Byte 0 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                 |  |         |  |

| Item     | Reserved  | Fail   | Fixed  | Multicast | P8 Aging  | ... | P1 Aging  | P0 Aging  |
|----------|-----------|--------|--------|-----------|-----------|-----|-----------|-----------|
| RD[47:0] | RD[47:45] | RD[44] | RD[43] | RD[42]    | RD[41:40] | ... | RD[27:26] | RD[25:24] |
| Example  | 0b000     | 0b0    | 0b1    | 0b1       | 0b11      | ... | 0b00      | 0b11      |

For example, if we want to read the lookup table multicast entry 2748 (0xABC), then we have to configure:

- WD[35:32] (LVTDIR2[3:0])=0xA
- WD[47:40] (LVTDIR2[15:8])=0xBC
- Others=0

When a fixed multicast entry in the lookup table is 01-00-5E-78-9A-BC, member ports={8, 5, 3, 1, 0}. The return data in RD[11:4]=0x78, RD[3:0]=0x9, RD[41:24]=Portn\_Aging[1:0] (n=0-8)={0b11 0b00 0b00 0b11 0b00 0b11 0b00 0b11}, Multicast is in RD[42] = 1, Fixed is in RD[43] = 1, and Fail is in RD[44]=0.

### 8.17.4. Look-up Table Write Access Method (Multicast)

For Lookup Table Multicast entry write access, we need to input the Multicast MAC address, Multicast flag, Fixed flag, and Aging timer of all 9 ports. The WD[69:0] format is shown in Table 29. After inputting the lookup table write access command (TABLE\_CMD[2:0]=0b001 and TABLE\_EXEC=0b1), the lookup table write access is finished.

For example, to configure a fixed entry with member ports to be Ports {8, 5, 3, 1, 0} and the MAC Address=01-00-5E-78-9A-BC:

- Configure WD[7:0]=0x01, WD[15:8]=0x00, WD[23:16]=0x5E, WD[31:24]=0x78, WD[39:32]=0x9A, and WD[47:40]=0xBC
- WD[48]=0b1 for Multicast entry
- WD[49]=0b1 for fixed entry
- WD[69:52]={0b11 0b00 0b00 0b11 0b00 0b11 0b00 0b11 0b11} for Ports {8, 5, 3, 1, 0} aging timer
- Other reserved and un-defined bits in WD[63:0] must=0b0.

**Table 29. Data Input Buffer (WD[69:0]) Format for Lookup Table Multicast Entry Write Access**

|        | MAC Address     | Write Data[47:0] | Example |
|--------|-----------------|------------------|---------|
| Byte 5 | 7 6 5 4 3 2 1 0 | WD[7:0]          | 0x01    |
| Byte 4 | 7 6 5 4 3 2 1 0 | WD[15:8]         | 0x00    |
| Byte 3 | 7 6 5 4 3 2 1 0 | WD[23:16]        | 0x5E    |
| Byte 2 | 7 6 5 4 3 2 1 0 | WD[31:24]        | 0x78    |
| Byte 1 | 7 6 5 4 3 2 1 0 | WD[39:32]        | 0x9A    |
| Byte 0 | 7 6 5 4 3 2 1 0 | WD[47:40]        | 0xBC    |

| Item     | P8 Aging  | ... | P1 Aging  | P0 Aging  | Reserved  | Fixed  | Multicast |
|----------|-----------|-----|-----------|-----------|-----------|--------|-----------|
| WD[69:0] | WD[69:68] | ... | WD[55:54] | WD[53:52] | WD[51:50] | WD[49] | WD[48]    |
| Example  | 0b11      | ... | 0b00      | 0b11      | 0b00      | 0b1    | 0b1       |

### 8.17.5. VLAN Table Read Access Method

For VLAN table read access, we need to input the VLAN entry number into Entry[11:0] (WD[11:0]). After inputting the VLAN table read access command (TABLE\_CMD[1:0]=0b10 and TABLE\_EXEC=0b1), the returned data will be shown in Member[8:0] (Register RD[8:0]) as shown in Table 30.

**Table 30. Data Output Buffer (RD[8:0]) Format for VLAN Table Read Access**

| Entry[11:0] | VID[11:0] | Member[8:0] |
|-------------|-----------|-------------|
| WD[11:0]    |           | RD[8:0]     |
| 0           | 0x000     | Reserved    |
| 1           | 0x001     | 0b010000001 |
| 2           | 0x002     | 0b010000010 |
| ...         | ...       | ...         |
| 4094        | 0xFFE     | 0b000000000 |
| 4095        | 0xFFF     | Reserved    |

For example, when input data are Entry[11:0]=0x002 (WD[11:0]) in Register LVTDIR0, TABLE\_CMD[1:0]=0b10, and TABLE\_EXEC=0b1, then the member set of VLAN entry 2 (VID[11:0]=0x002) will return Member[8:0]=0b010000010 (RD[8:0]) in Register LVTDOR0.

### 8.17.6. VLAN Table Write Access Method

For VLAN table write access, we need to input the VLAN entry number into Entry[11:0] (WD[11:0]) and member set into Member[8:0] (WD[24:16]). After inputting the VLAN table read access command (TABLE\_CMD[1:0]=0b11 and TABLE\_EXEC=0b1), the VLAN table write access is finished (see Table 31).

**Table 31. Data Output Buffer (WD[24:0]) Format for VLAN Table Write Access**

| Entry[11:0] | VID[11:0] | Member[8:0] |
|-------------|-----------|-------------|
| WD[11:0]    |           | WD[24:16]   |
| 0           | 0x000     | Reserved    |
| 1           | 0x001     | 0b010000001 |
| 2           | 0x002     | 0b010000010 |
| ...         | ...       | ...         |
| 4094        | 0xFFE     | 0b000000000 |
| 4095        | 0xFFF     | Reserved    |

For example, when input Entry[11:0]=0x001 (WD[11:0]) in Register LVTDIR0, Member[8:0]=0b010000001 in Register LVTDIR1, and TABLE\_CMD[1:0]=0b11, TABLE\_EXEC=0b1, the VLAN entry, VID[11:0]=0x001, is configured as Member={ Port 0 and Port 7}.

## 9. Interface Descriptions

### 9.1. EEPROM SMI Host to EEPROM

The EEPROM interface of the RTL8366 and RTL8369 uses the serial bus EEPROM Serial Management Interface (SMI). The 2K-bit 24C02 EEPROM is read via the EEPROM SMI protocol. When the RTL8366/RTL8369 is powered up, the RTL8366/RTL8369 drives SCK and SDA to read the registers from the EEPROM.

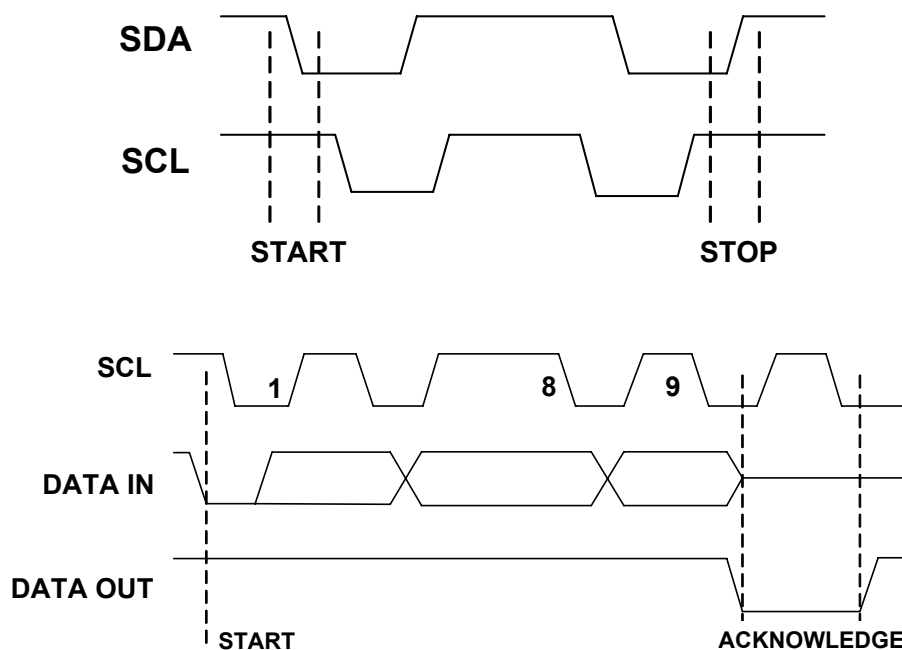


Figure 15. EEPROM SMI Host to EEPROM

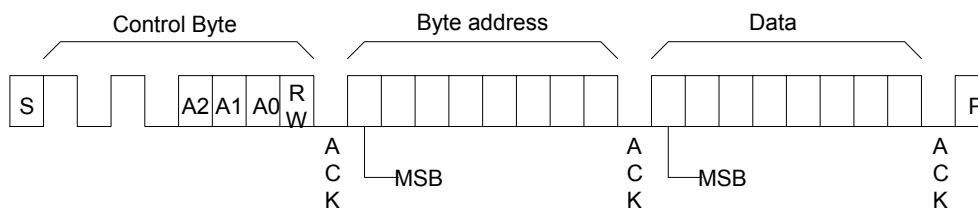


Figure 16. Host Mode EEPROM SMI Frame



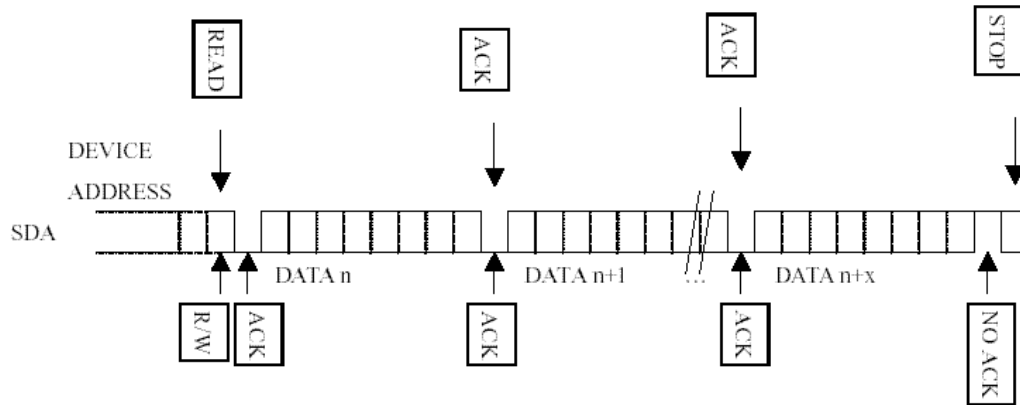


Figure 17. EEPROM SMI Sequential Read

## 9.2. EEPROM SMI Slave for External CPU

When EEPROM auto-load is complete, the RTL8366/RTL8369 registers can be accessed via SCK and SDA via an external CPU. The device address of the RTL8366/RTL8369 is 0x4. Read/write timing is shown in Figure 18 and Figure 19. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

### Register write through EEPROM SMI Slave interface

Address: 16'h0318

Data: 16'h1918

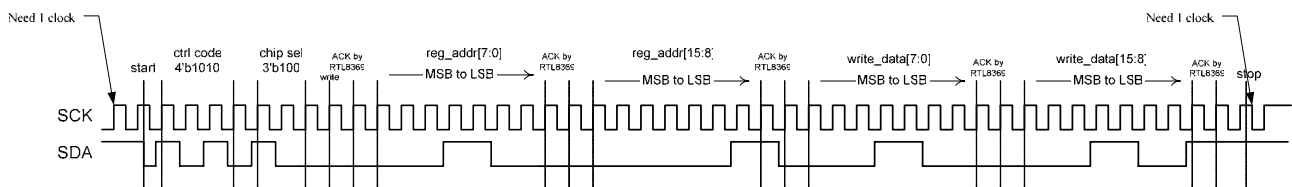


Figure 18. EEPROM SMI Write Command for Slave Mode

### Register read through EEPROM SMI Slave interface

Address: 16'h0318

Data: 16'h1918

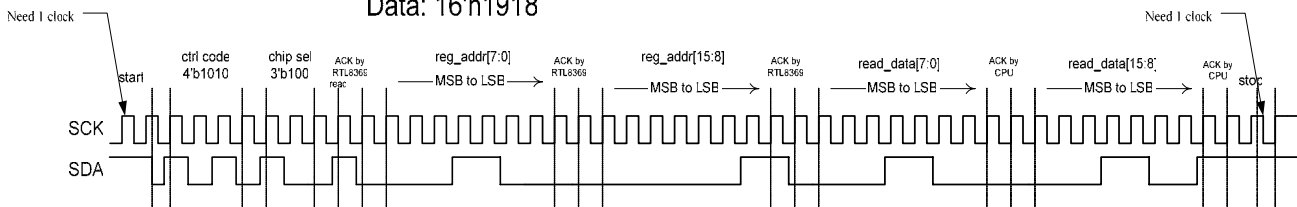


Figure 19. EEPROM SMI Read Command for Slave Mode

### 9.3. *SMI (MDC/MDIO) Interface*

The RLT8366/RTL8369 use Simple Management Interface (SMI) via MDC and MDIO signals to poll the MII register of the RTL8212. The polled PHY addresses are in SMI frame format.

**Table 32. SMI Frame Format**

|              | <b>Preamble<br/>(32 bits)</b> | <b>Start<br/>(2 bits)</b> | <b>OP<br/>Code<br/>(2 bits)</b> | <b>PHYAD<br/>(5 bits)</b>  | <b>REGAD<br/>(5 bits)</b>  | <b>Turn<br/>Around<br/>(2 bits)</b> | <b>Data<br/>(16 bits)</b>           | <b>Idle</b> |
|--------------|-------------------------------|---------------------------|---------------------------------|--|--|-------------------------------------|-------------------------------------|-------------|
| <b>Read</b>  | 1.....1                       | 01                        | 10                              | A <sub>4</sub> A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub> | R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub> | Z0                                  | D <sub>15</sub> .....D <sub>0</sub> | Z*          |
| <b>Write</b> | 1.....1                       | 01                        | 01                              | A <sub>4</sub> A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub> | R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub> | 10                                  | D <sub>15</sub> .....D <sub>0</sub> | Z*          |

### 9.4. *MAC to PHY Interface: RSGMII (Reduced Serial Gigabit Media Independent Interface)*

To reduce PCB complexity and IC pin count, the RTL8366/RTL8369 provides 3/4 innovative 2.5Gbps RSGMII (Reduced Serial Gigabit Media Independent Interface). Each of these serial interfaces can carry data originating from two Gigabit MAC ports simultaneously, and recover clock from the data rather than use a dedicated clock. These interfaces reduces the interconnection between the MAC and PHY to only 5 pins for each dual MAC RTL8212. Figure 20 shows the RSGMII interconnection diagram.



## 9.5. General Purpose Interface

The General Purpose Interface (GPIF) can be operated in 3 modes, strapped by GPIF\_MODE[4:0] pins upon reset.

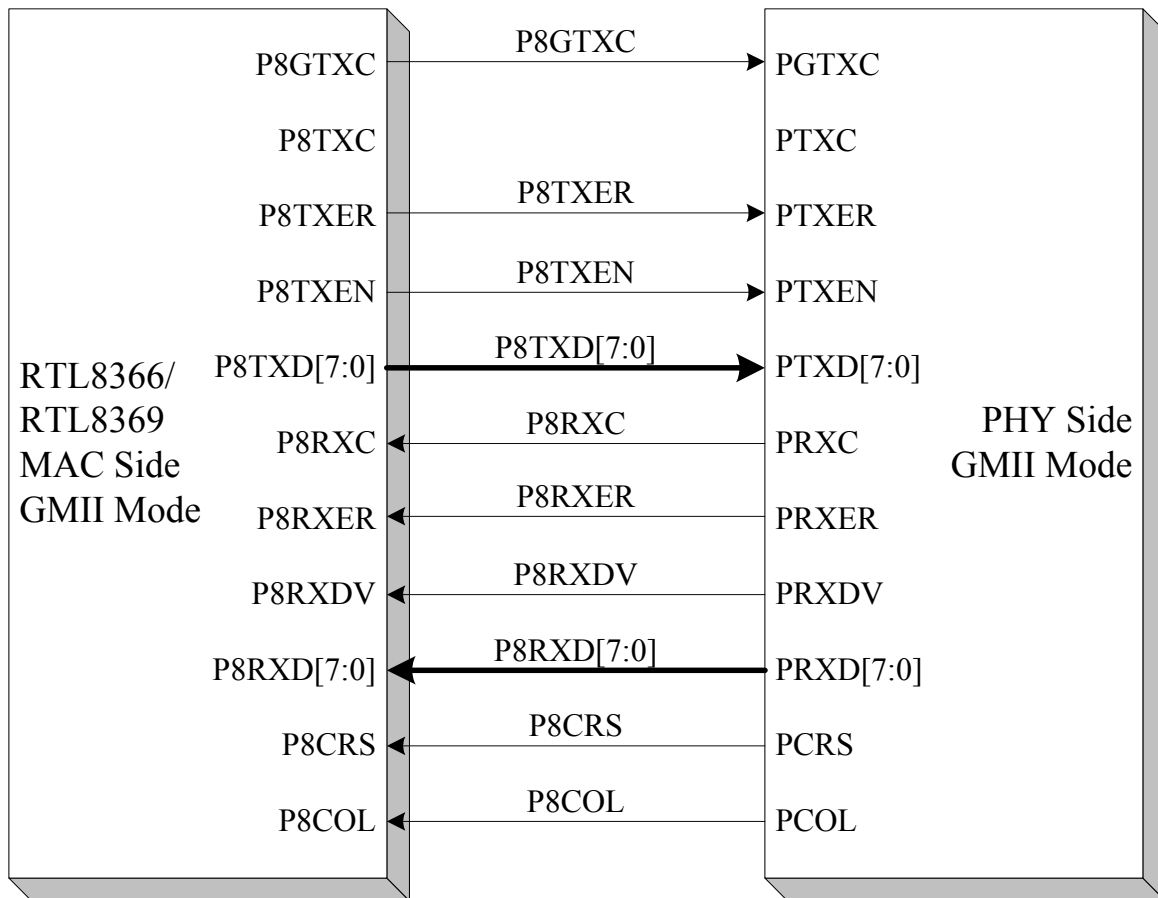
- 0b11000: GMII/MII MAC: The interface is run in GMII mode when the port is linked at 1000Mbps. As the speed changes to 100Mbps mode, the interface turns to run in MII MAC mode. *10Mbps is not supported in this configuration.*
- 0b11001: RGMII: The interface is run in RGMII mode. *Only supports 1000Mbps Full Duplex mode.*
- 0b11100: MII PHY mode: The interface is run in MII PHY mode at 100Mbps Full duplex. *100Mbps Half duplex and 10Mbps Full/Half duplex are not supported in this configuration.*

When NWay is off in GMII/RGMII mode, the speed is determined by PORT\_ABILITY<sub>n</sub>[7:0] (Reg. 0x11-15) configuration. In MII PHY mode, the link/flow control ability is determined by strapped pin P8\_PHY\_LINK (pin 11) and DIS\_FC (pin 7). The P8\_PHY\_LINK and DIS\_FC have their reflected registers, which are configurable by the CPU interface.

**Table 33. GMII/RGMII/MII PHY Mode Pins**

| Pin No.        | GMII/MII   | RGMII      | MII PHY     |
|----------------|------------|------------|-------------|
| 126, 128, 1, 2 | P8TXD[7:4] | N/A        | N/A         |
| 3, 4, 5, 6     | P8TXD[3:0] | P8TXD[3:0] | P8PRXD[3:0] |
| 7              | P8TXEN     | N/A        | P8PRXDV     |
| 9              | P8GTXC     | P8TXC      | P8PRXC      |
| 11             | P8TXER     | P8TXCTRL   | N/A         |
| 12             | P8TXC      | N/A        | N/A         |
| 14             | P8CRS      | N/A        | N/A         |
| 16             | P8COL      | N/A        | N/A         |
| 17             | P8RXER     | P8RXCTRL   | P8PTXER     |
| 18             | P8RXC      | P8RXC      | P8PTXC      |
| 19             | P8RXDV     | N/A        | P8PTXEN     |
| 29, 28, 27, 26 | P8RXD[7:4] | N/A        | N/A         |
| 24, 22, 21, 20 | P8RXD[3:0] | P8RXD[3:0] | P8PTXD[3:0] |

### 9.5.1. GMII/MII MAC Mode (Only for 100Mbps and 1000Mbps)



**Figure 21. Signal Diagram of GMII Mode Interface (1000Mbps)**

### 9.5.2. MII MAC Mode Interface (100Mbps)

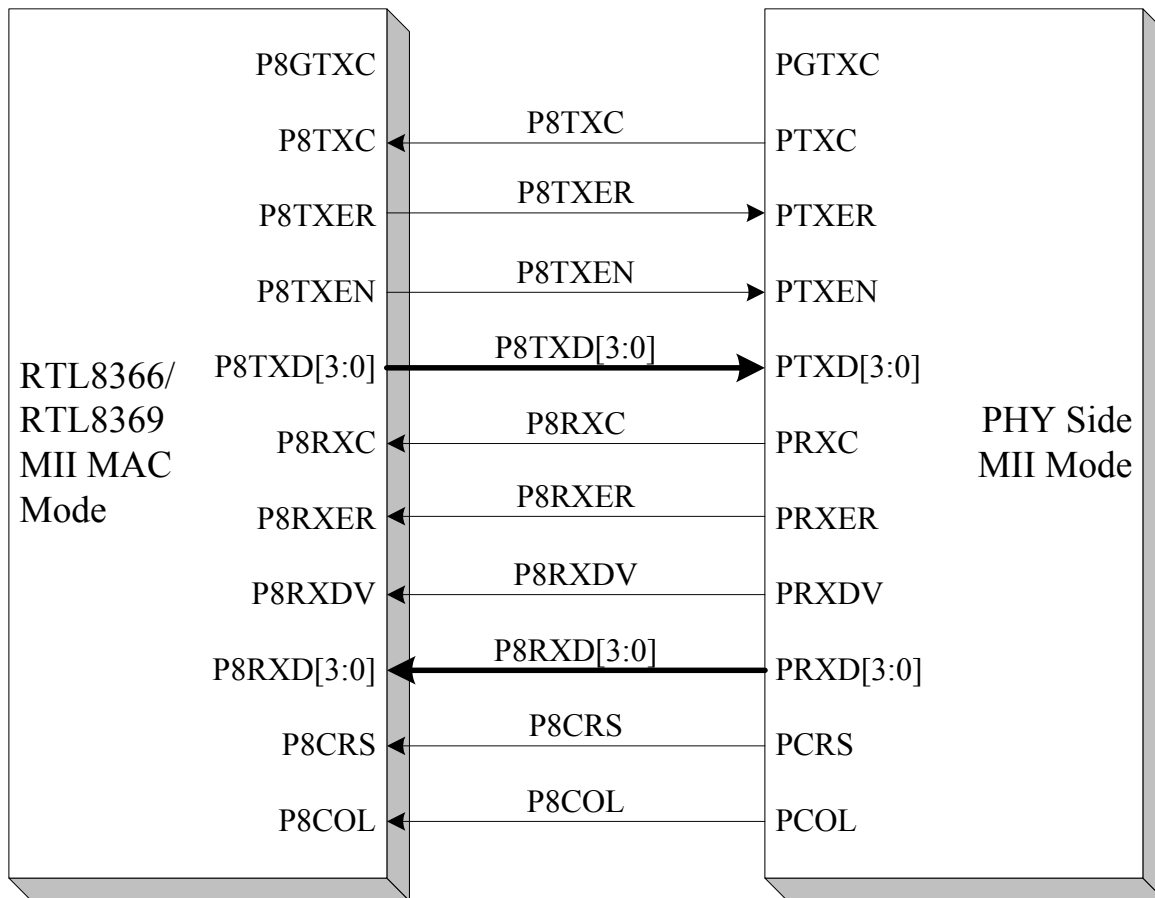
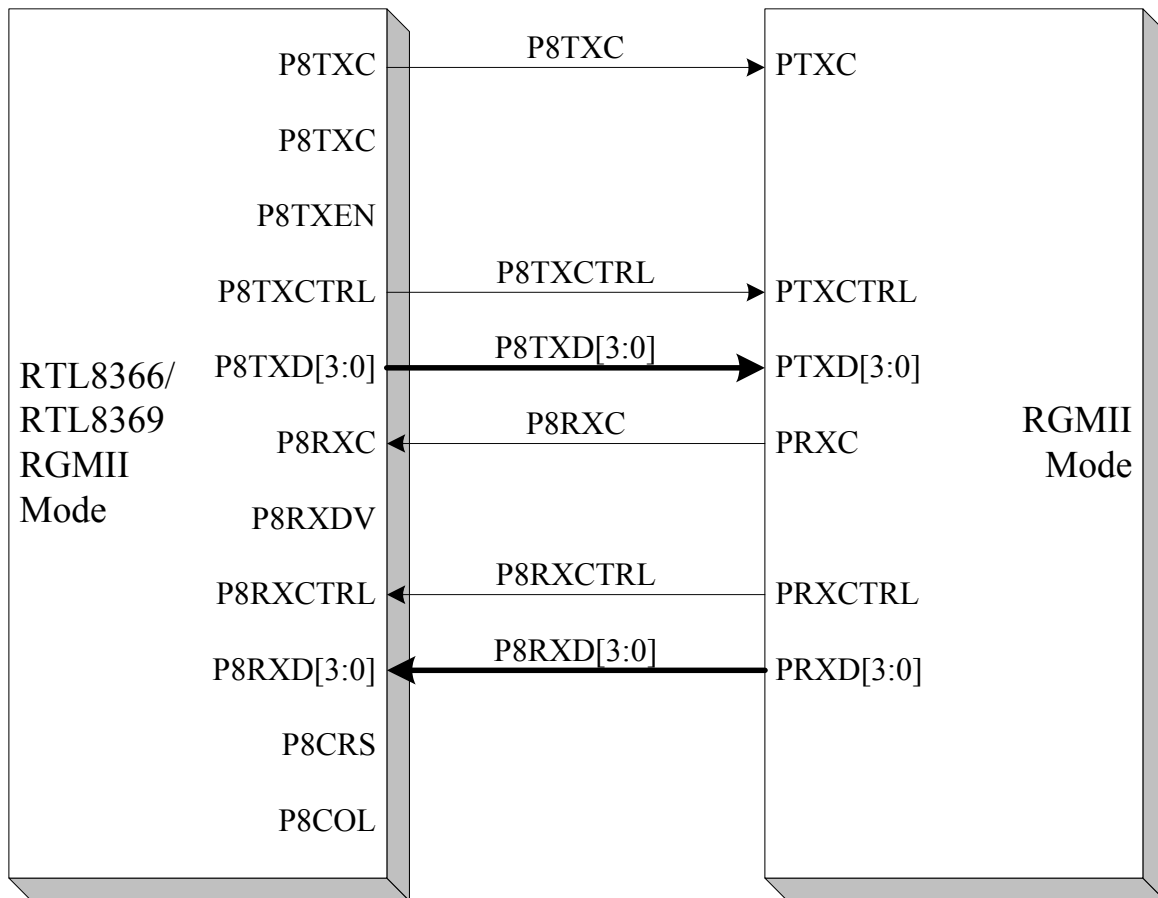


Figure 22. Signal Diagram of MII MAC Mode Interface (100Mbps)

### 9.5.3. RGMII Mode (Only for 1000Mbps Full Duplex)



**Figure 23. Signal Diagram of RGMII Mode Interface**

### 9.5.4. MII PHY Mode (Only for 100Mbps Full Duplex)

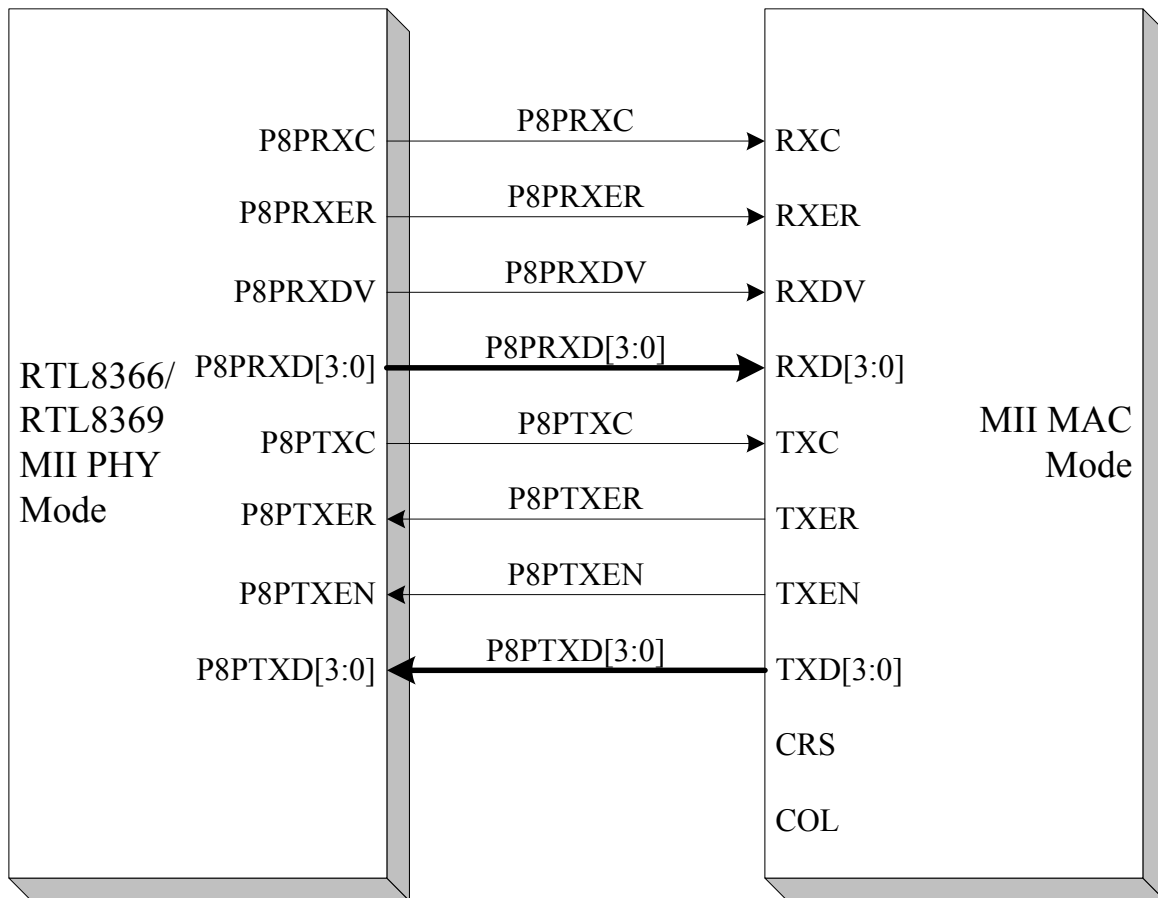


Figure 24. Signal Diagram of MII PHY Mode Interface (100Mbps Full)

## 9.6. Power Management Interface

TBD



## 10. Register and EEPROM Descriptions

RTL8366/RTL8369 registers can be divided into two parts. One is from 0x0000 to 0x007F and the other is 0x0100 to 0xFFFF

The first part can be configured by EEPROM via auto-load after power on or pin reset. Both parts can be accessed by external CPU via the EEPROM SMI after power on.

Per-port configuration registers for ports 5~7 are not supported in the RTL8366. For example, DISABLE\_PORT[7:5] is not supported in the RTL8366.

### 10.1. Registers List Part I

All register values can be configured by EEPROM via auto-load after power on, or pin reset. Two bytes of EEPROM configure 1 register of the RTL8366/RTL8369. For example, data 0x01 and 0x00 configure the register 0x0000. 0x01 is MSB and 0x00 is LSB. If configuration of register 0x0000 is 0x2E04, EEPROM data of 0x01 is 0x2E and 0x00 is 0x04.

#### 10.1.1. EEPROM Mapped Registers

**Table 34. EEPROM Mapped Registers**

| EEPROM       | Address | Description                                | Register Name     | Bits   | Default | Default |
|--------------|---------|--|-------------------|--------|---------|---------|
| 0x00<br>0x01 | 0x0000  | Switch Global Control Register (SGCR)      | EN_BC_STORM_CTRL  | [0]    | 0b0     | 0x2E04  |
|              |         |  | Internal Use      | [1]    | 0b0     |         |
|              |         |  | Internal Use      | [2]    | 0b1     |         |
|              |         |  | Reserved          | [3]    | 0b0     |         |
|              |         |  | MAX_LENGTH[1:0]   | [5:4]  | 0b0     |         |
|              |         |  | EN_IGMP           | [6]    | 0b0     |         |
|              |         |  | EN_ARP            | [7]    | 0b0     |         |
|              |         |  | DIS_BP            | [8]    | 0b0     |         |
|              |         |  | JAM_MODE          | [9]    | 0b1     |         |
|              |         |  | EN_48PASS1        | [10]   | 0b1     |         |
|              |         |  | MAX_PAUSE_CNT     | [11]   | 0b1     |         |
|              |         |  | EN_MLT_BRD        | [12]   | 0b0     |         |
|              |         |  | Internal Use      | [13]   | 0b1     |         |
|              |         |  | Internal Use      | [14]   | 0b0     |         |
| Internal Use | [15]    | 0b0  |                   |        |         |         |
| 0x02<br>0x03 | 0x0001  | Port Enable Control Register (PECR)        | DISABLE_PORT[8:0] | [8:0]  | 0x000   | 0x0000  |
|              |         |  | Reserved          | [15:9] | 0x00    |         |
| 0x04<br>0x05 | 0x0002  | Switch Security Control Register 0 (SSCR0) | DIS_LEARN[8:0]    | [8:0]  | 0x000   | 0x0000  |
|              |         |  | Reserved          | [15:9] | 0x00    |         |
| 0x06         | 0x0003  | Switch Security Control                    | DIS_AGE[8:0]      | [8:0]  | 0x0     | 0x0000  |

| EEPROM       | Address | Description                                   | Register Name       | Bits    | Default | Default |
|--------------|---------|---|---------------------|---------|---------|---------|
| 0x07         |         | Register 1 (SSCR1)                            | Reserved            | [15:9]  | 0x00    |         |
| 0x08<br>0x09 | 0x0004  | Switch Security Control<br>Register 2 (SSCR2) | DROP_UNKNOWN_DA     | [0]     | 0b0     | 0x0020  |
|              |         |   | Internal Use        | [1]     | 0b0     |         |
|              |         |   | Internal Use        | [2]     | 0b0     |         |
|              |         |   | Reserved            | [3]     | 0b0     |         |
|              |         |   | Internal Use        | [4]     | 0b0     |         |
|              |         |   | Internal Use        | [5]     | 0b1     |         |
|              |         |   | Internal Use        | [6]     | 0b0     |         |
|              |         |   | Internal Use        | [7]     | 0b0     |         |
|              |         |   | Reserved            | [9:8]   | 0b00    |         |
|              |         |   | Internal Use        | [10]    | 0b0     |         |
|              |         |   | Reserved            | [15:11] | 0x00    |         |
| 0x0A<br>0x0B | 0x0005  | VLAN/Trunk Control Register 0<br>(VTCR0)      | EN_VLAN             | [0]     | 0b0     | 0x200A  |
|              |         |   | VLAN_TAG_AWARE      | [1]     | 0b1     |         |
|              |         |   | VLAN_TAG_ADMIT      | [2]     | 0b0     |         |
|              |         |   | EN_INGRESS_RULE     | [3]     | 0b1     |         |
|              |         |   | EN_UC_LEAKY         | [4]     | 0b0     |         |
|              |         |   | EN_ARP_LEAKY        | [5]     | 0b0     |         |
|              |         |   | EN_IPMC_LEAKY       | [6]     | 0b0     |         |
|              |         |   | Internal Use        | [7]     | 0b0     |         |
|              |         |   | Internal Use        | [11:8]  | 0b0     |         |
|              |         |   | EN_TAG_DROP         | [12]    | 0b0     |         |
|              |         |   | Internal Use        | [13]    | 0b1     |         |
|              |         |   | P8_TAG_CONTROL[1:0] | [15:14] | 0b0     |         |
| 0x0C<br>0x0D | 0x0006  | VLAN/Trunk Control Register 1<br>(VTCR1)      | P0_TAG_CONTROL[1:0] | [1:0]   | 0b00    | 0x0000  |
|              |         |   | P1_TAG_CONTROL[1:0] | [3:2]   | 0b00    |         |
|              |         |   | P2_TAG_CONTROL[1:0] | [5:4]   | 0b00    |         |
|              |         |   | P3_TAG_CONTROL[1:0] | [7:6]   | 0b00    |         |
|              |         |   | P4_TAG_CONTROL[1:0] | [9:8]   | 0b00    |         |
|              |         |   | P5_TAG_CONTROL[1:0] | [11:10] | 0b00    |         |
|              |         |   | P6_TAG_CONTROL[1:0] | [13:12] | 0b00    |         |
|              |         |   | P7_TAG_CONTROL[1:0] | [15:14] | 0b00    |         |
| 0x0F         | 0x0007  | Port Mirror Control Register<br>(PMCR)        | SOURCE_PORT[3:0]    | [3:0]   | 0x0     | 0x0000  |
|              |         |   | MINITOR_PORT[3:0]   | [7:4]   | 0x0     |         |
|              |         |   | MIRROR_RX           | [8]     | 0b0     |         |
|              |         |   | MIRROR_TX           | [9]     | 0b0     |         |
|              |         |   | MIRROR_SPC          | [10]    | 0b0     |         |
|              |         |   | MIRROR_ISO          | [11]    | 0b0     |         |
|              |         |   | Reserved            | [14:12] | 0b00    |         |
|              |         |   | Internal Use        | [15]    | 0b0     |         |
| 0x10<br>0x11 | 0x0008  | Internal Use                                  | N/A                 | [15:0]  | 0x0800  | 0x0800  |
| 0x12<br>0x13 | 0x0009  | QoS Control Register 0 (QCR0)                 | EN_QOS              | [0]     | 0b0     | 0xF000  |
|              |         |   | Internal Use        | [1]     | 0b0     |         |

| EEPROM       | Address | Description  | Register Name      | Bits    | Default           | Default |
|--------------|---------|--|--------------------|---------|-------------------|---------|
|              |         |  | EN_PORT_PRI        | [2]     | 0b0               |         |
|              |         |  | EN_DS_PRI          | [3]     | 0b0               |         |
|              |         |  | EN_1Q_PRI          | [4]     | 0b0               |         |
|              |         |  | QWEIGHT[1:0]       | [7:6]   | 0b00              |         |
|              |         |  | VLAN_PRI_TAB[7:0]  | [15:8]  | 0xF0              |         |
| 0x14<br>0x15 | 0x000A  | QoS Control Register 1 (QCR1)                        | PORT_PRI[8:0]      | [8:0]   | 0x000             | 0x0000  |
|              |         |  | Reserved           | [15:9]  | 0x00              |         |
| 0x16<br>0x17 | 0x000B  | QoS Control Register 2 (QCR2)                        | TOS[15:0]          | [15:0]  | 0x0000            | 0x0000  |
| 0x18<br>0x19 | 0x000C  | QoS Control Register 3 (QCR3)                        | TOS[31:16]         | [15:0]  | 0x0000            | 0x0000  |
| 0x1A<br>0x1B | 0x000D  | QoS Control Register 4 (QCR4)                        | TOS[47:32]         | [15:0]  | 0x0000            | 0x0000  |
| 0x1C<br>0x1D | 0x000E  | QoS Control Register 5 (QCR5)                        | TOS[63:48]         | [15:0]  | 0x0000            | 0x0000  |
| 0x1E<br>0x1F | 0x000F  | MAC Control Packet Control Register 0 (MCPCR0)       | MLTIDST[15:0]      | [15:0]  | 0x5541<br>(Strap) | 0x5541  |
| 0x20<br>0x21 | 0x0010  | MAC Control Packet Control Register 1 (MCPCR1)       | MLTIDST[31:16]     | [15:0]  | 0x5555<br>(Strap) | 0x5555  |
| 0x22<br>0x23 | 0x0011  | Port Advertising Ability Control Register 0 (PAACR0) | PORT_ABILITY0[7:0] | [7:0]   | 0xFF              | 0xFFFF  |
|              |         |  | PORT_ABILITY1[7:0] | [15:8]  | 0xFF              |         |
| 0x24<br>0x25 | 0x0012  | Port Advertising Ability Control Register 1 (PAACR1) | PORT_ABILITY2[7:0] | [7:0]   | 0xFF              | 0xFFFF  |
|              |         |  | PORT_ABILITY3[7:0] | [15:8]  | 0xFF              |         |
| 0x26<br>0x27 | 0x0013  | Port Advertising Ability Control Register 2 (PAACR2) | PORT_ABILITY4[7:0] | [7:0]   | 0xFF              | 0xFFFF  |
|              |         |  | PORT_ABILITY5[7:0] | [15:8]  | 0xFF              |         |
| 0x28<br>0x29 | 0x0014  | Port Advertising Ability Control Register 3 (PAACR3) | PORT_ABILITY6[7:0] | [7:0]   | 0xFF              | 0xFFFF  |
|              |         |  | PORT_ABILITY7[7:0] | [15:8]  | 0xFF              |         |
| 0x2A<br>0x2B | 0x0015  | Port Advertising Ability Control Register 4 (PAACR4) | PORT_ABILITY8[7:0] | [7:0]   | 0xFF              | 0x00FF  |
|              |         |  | Reserved           | [15:8]  | 0x00              |         |
| 0x2C<br>0x2D | 0x0016  | VLAN ID Configuration Register 0 (VIDCR0)            | VID0[11:0]         | [11:0]  | 0x100             | 0x0100  |
|              |         |  | Reserved           | [15:12] | 0x0               |         |
| 0x2E<br>0x2F | 0x0017  | VLAN Member Configuration Register 0 (VMCR0)         | MEMBER0[8:0]       | [8:0]   | 0x081             | 0x0081  |
|              |         |  | Reserved           | [15:9]  | 0x00              |         |
| 0x30<br>0x31 | 0x0018  | VLAN ID Configuration Register 1 (VIDCR1)            | VID1[11:0]         | [11:0]  | 0x101             | 0x0101  |
|              |         |  | Reserved           | [15:12] | 0x0               |         |
| 0x32<br>0x33 | 0x0019  | VLAN Member Configuration Register 1 (VMCR1)         | MEMBER1[8:0]       | [8:0]   | 0x082             | 0x0082  |
|              |         |  | Reserved           | [15:9]  | 0x00              |         |
| 0x34<br>0x35 | 0x001A  | VLAN ID Configuration Register 2 (VIDCR2)            | VID2[11:0]         | [11:0]  | 0x102             | 0x0102  |
|              |         |  | Reserved           | [15:12] | 0x0               |         |
| 0x36<br>0x37 | 0x001B  | VLAN Member Configuration Register 2 (VMCR2)         | MEMBER2[8:0]       | [8:0]   | 0x084             | 0x0084  |
|              |         |  | Reserved           | [15:9]  | 0x00              |         |
| 0x38<br>0x39 | 0x001C  | VLAN ID Configuration Register 3 (VIDCR3)            | VID3[11:0]         | [11:0]  | 0x103             | 0x0103  |
|              |         |  | Reserved           | [15:12] | 0x0               |         |
| 0x3A         | 0x001D  | VLAN Member Configuration                            | MEMBER3[8:0]       | [8:0]   | 0x088             | 0x0088  |

| EEPROM | Address | Description               | Register Name | Bits    | Default | Default |
|--------|---------|---------------------------|---------------|---------|---------|---------|
| 0x3B   |         | Register 3 (VMCR3)        | Reserved      | [15:9]  | 0x00    |         |
| 0x3C   | 0x001E  | VLAN ID Configuration     | VID4[11:0]    | [11:0]  | 0x104   | 0x0104  |
| 0x3D   |         | Register 4 (VIDCR4)       | Reserved      | [15:12] | 0x0     |         |
| 0x3E   | 0x001F  | VLAN Member Configuration | MEMBER4[8:0]  | [8:0]   | 0x090   | 0x0090  |
| 0x3F   |         | Register 4 (VMCR4)        | Reserved      | [15:9]  | 0x00    |         |
| 0x40   | 0x0020  | VLAN ID Configuration     | VID5[11:0]    | [11:0]  | 0x105   | 0x0105  |
| 0x41   |         | Register 5 (VIDCR5)       | Reserved      | [15:12] | 0x0     |         |
| 0x42   | 0x0021  | VLAN Member Configuration | MEMBER5[8:0]  | [8:0]   | 0x0A0   | 0x00A0  |
| 0x43   |         | Register 5 (VMCR5)        | Reserved      | [15:9]  | 0x00    |         |
| 0x44   | 0x0022  | VLAN ID Configuration     | VID6[11:0]    | [11:0]  | 0x106   | 0x0106  |
| 0x45   |         | Register 6 (VIDCR6)       | Reserved      | [15:12] | 0x0     |         |
| 0x46   | 0x0023  | VLAN Member Configuration | MEMBER6[8:0]  | [8:0]   | 0xC0    | 0x00C0  |
| 0x47   |         | Register 6 (VMCR6)        | Reserved      | [15:9]  | 0x00    |         |
| 0x48   | 0x0024  | VLAN ID Configuration     | VID7[11:0]    | [11:0]  | 0x107   | 0x0107  |
| 0x49   |         | Register 7 (VIDCR7)       | Reserved      | [15:12] | 0x0     |         |
| 0x4A   | 0x0025  | VLAN Member Configuration | MEMBER7[8:0]  | [8:0]   | 0xFF    | 0x00FF  |
| 0x4B   |         | Register 7 (VMCR7)        | Reserved      | [15:9]  | 0x00    |         |
| 0x4C   | 0x0026  | VLAN ID Configuration     | VID8[11:0]    | [11:0]  | 0x000   | 0x0000  |
| 0x4D   |         | Register 8 (VIDCR8)       | Reserved      | [15:12] | 0x0     |         |
| 0x4E   | 0x0027  | VLAN Member Configuration | MEMBER8[8:0]  | [8:0]   | 0x000   | 0x0000  |
| 0x4F   |         | Register 8 (VMCR8)        | Reserved      | [15:9]  | 0x00    |         |
| 0x50   | 0x0028  | VLAN ID Configuration     | VID9[11:0]    | [11:0]  | 0x000   | 0x0000  |
| 0x51   |         | Register 9 (VIDCR9)       | Reserved      | [15:12] | 0x0     |         |
| 0x52   | 0x0029  | VLAN Member Configuration | MEMBER9[8:0]  | [8:0]   | 0x000   | 0x0000  |
| 0x53   |         | Register 9 (VMCR9)        | Reserved      | [15:9]  | 0x00    |         |
| 0x54   | 0x002A  | VLAN ID Configuration     | VID10[11:0]   | [11:0]  | 0x000   | 0x0000  |
| 0x55   |         | Register 10 (VIDCR10)     | Reserved      | [15:12] | 0x0     |         |
| 0x56   | 0x002B  | VLAN Member Configuration | MEMBER10[8:0] | [8:0]   | 0x000   | 0x0000  |
| 0x57   |         | Register 10 (VMCR10)      | Reserved      | [15:9]  | 0x00    |         |
| 0x58   | 0x002C  | VLAN ID Configuration     | VID11[11:0]   | [11:0]  | 0x000   | 0x0000  |
| 0x59   |         | Register 11 (VIDCR11)     | Reserved      | [15:12] | 0x0     |         |
| 0x5A   | 0x002D  | VLAN Member Configuration | MEMBER11[8:0] | [8:0]   | 0x000   | 0x0000  |
| 0x5B   |         | Register 11 (VMCR11)      | Reserved      | [15:9]  | 0x00    |         |
| 0x5C   | 0x002E  | VLAN ID Configuration     | VID12[11:0]   | [11:0]  | 0x000   | 0x0000  |
| 0x5D   |         | Register 12 (VIDCR12)     | Reserved      | [15:12] | 0x0     |         |
| 0x5E   | 0x002F  | VLAN Member Configuration | MEMBER12[8:0] | [8:0]   | 0x000   | 0x0000  |
| 0x5F   |         | Register 12 (VMCR12)      | Reserved      | [15:9]  | 0x00    |         |
| 0x60   | 0x0030  | VLAN ID Configuration     | VID13[11:0]   | [11:0]  | 0x000   | 0x0000  |
| 0x61   |         | Register 13 (VIDCR13)     | Reserved      | [15:12] | 0x0     |         |
| 0x62   | 0x0031  | VLAN Member Configuration | MEMBER13[8:0] | [8:0]   | 0x000   | 0x0000  |
| 0x63   |         | Register 13 (VMCR13)      | Reserved      | [15:9]  | 0x00    |         |
| 0x64   | 0x0032  | VLAN ID Configuration     | VID14[11:0]   | [11:0]  | 0x000   | 0x0000  |
| 0x65   |         | Register 14 (VIDCR14)     | Reserved      | [15:12] | 0x0     |         |

| EEPROM       | Address | Description                                    | Register Name   | Bits    | Default | Default |
|--------------|---------|--|-----------------|---------|---------|---------|
| 0x66<br>0x67 | 0x0033  | VLAN Member Configuration Register 14 (VMCR14) | MEMBER14[8:0]   | [8:0]   | 0x000   | 0x0000  |
|              |         |  | Reserved        | [15:9]  | 0x00    |         |
| 0x68<br>0x69 | 0x0034  | VLAN ID Configuration Register 15 (VIDCR15)    | VID15[11:0]     | [11:0]  | 0x000   | 0x0000  |
|              |         |  | Reserved        | [15:12] | 0x0     |         |
| 0x6A<br>0x6B | 0x0035  | VLAN Member Configuration Register 15 (VMCR15) | MEMBER15[8:0]   | [8:0]   | 0x000   | 0x0000  |
|              |         |  | Reserved        | [15:9]  | 0x00    |         |
| 0x6C<br>0x6D | 0x0036  | LED Control Register 0 (LCR0)                  | LED_MODE[1:0]   | [1:0]   | 0b00    | 0x0000  |
|              |         |  | LED_BLINK_TIME  | [2]     | 0b0     |         |
|              |         |  | LED_RESET_BLINK | [3]     | 0b0     |         |
|              |         |  | Internal Use    | [5:4]   | 0b00    |         |
|              |         |  | Internal Use    | [7:6]   | 0b00    |         |
|              |         |  | Internal Use    | [9:8]   | 0b00    |         |
|              |         |  | Internal Use    | [11:10] | 0b00    |         |
|              |         |  | Internal Use    | [12]    | 0b0     |         |
|              |         |  | Reserved        | [15:13] | 0b0000  |         |
| 0x6E<br>0x6F | 0x0037  | Internal Use                                   | N/A             | [15:0]  | 0x4305  | 0x4305  |
| 0x70<br>0x71 | 0x0038  | MIB Counter Control Register 0 (MCCR0)         | MIB0_SELA[1:0]  | [1:0]   | 0b01    | 0x0505  |
|              |         |  | MIB0_SELB[1:0]  | [3:2]   | 0b01    |         |
|              |         |  | MIB0_SELC[1:0]  | [5:4]   | 0b00    |         |
|              |         |  | Reserved        | [7:6]   | 0b00    |         |
|              |         |  | MIB1_SELA[1:0]  | [9:8]   | 0b01    |         |
|              |         |  | MIB1_SELB[1:0]  | [11:10] | 0b01    |         |
|              |         |  | MIB1_SELC[1:0]  | [13:12] | 0b00    |         |
|              |         |  | Reserved        | [15:14] | 0b00    |         |
| 0x72<br>0x73 | 0x0039  | MIB Counter Control Register 1 (MCCR1)         | MIB2_SELA[1:0]  | [1:0]   | 0b01    | 0x0505  |
|              |         |  | MIB2_SELB[1:0]  | [3:2]   | 0b01    |         |
|              |         |  | MIB2_SELC[1:0]  | [5:4]   | 0b00    |         |
|              |         |  | Reserved        | [7:6]   | 0b00    |         |
|              |         |  | MIB3_SELA[1:0]  | [9:8]   | 0b01    |         |
|              |         |  | MIB3_SELB[1:0]  | [11:10] | 0b01    |         |
|              |         |  | MIB3_SELC[1:0]  | [13:12] | 0b00    |         |
|              |         |  | Reserved        | [15:14] | 0b00    |         |
| 0x74<br>0x75 | 0x003A  | MIB Counter Control Register 2 (MCCR2)         | MIB4_SELA[1:0]  | [1:0]   | 0b01    | 0x0505  |
|              |         |  | MIB4_SELB[1:0]  | [3:2]   | 0b01    |         |
|              |         |  | MIB4_SELC[1:0]  | [5:4]   | 0b00    |         |
|              |         |  | Reserved        | [7:6]   | 0b00    |         |
|              |         |  | MIB5_SELA[1:0]  | [9:8]   | 0b01    |         |
|              |         |  | MIB5_SELB[1:0]  | [11:10] | 0b01    |         |
|              |         |  | MIB5_SELC[1:0]  | [13:12] | 0b00    |         |
|              |         |  | Reserved        | [15:14] | 0b00    |         |
| 0x76<br>0x77 | 0x003B  | MIB Counter Control Register 3 (MCCR3)         | MIB6_SELA[1:0]  | [1:0]   | 0b01    | 0x0505  |
|              |         |  | MIB6_SELB[1:0]  | [3:2]   | 0b01    |         |
|              |         |  | MIB6_SELC[1:0]  | [5:4]   | 0b00    |         |

| EEPROM       | Address | Description                                    | Register Name     | Bits    | Default | Default |
|--------------|---------|--|-------------------|---------|---------|---------|
|              |         |  | Reserved          | [7:6]   | 0b00    |         |
|              |         |  | MIB7_SELA[1:0]    | [9:8]   | 0b01    |         |
|              |         |  | MIB7_SELB[1:0]    | [11:10] | 0b01    |         |
|              |         |  | MIB7_SELC[1:0]    | [13:12] | 0b00    |         |
|              |         |  | Reserved          | [15:14] | 0b00    |         |
| 0x78<br>0x79 | 0x003C  | MIB Counter Control Register 4 (MCCR4)         | MIB8_SELA[1:0]    | [1:0]   | 0b01    | 0x0005  |
|              |         | MIB8_SELB[1:0]                                 | [3:2]             | 0b01    |         |         |
|              |         | MIB8_SELC[1:0]                                 | [5:4]             | 0b00    |         |         |
|              |         | Reserved                                       | [15:6]            | 0b00    |         |         |
| 0x7A<br>0x7B | 0x003D  | RX Spanning Tree Statistic Register 0 (RSTSR0) | P0RXSTS[1:0]      | [1:0]   | 0b11    | 0xFFFF  |
|              |         |  | P1RXSTS[1:0]      | [3:2]   | 0b11    |         |
|              |         |  | P2RXSTS[1:0]      | [5:4]   | 0b11    |         |
|              |         |  | P3RXSTS[1:0]      | [7:6]   | 0b11    |         |
|              |         |  | P4RXSTS[1:0]      | [9:8]   | 0b11    |         |
|              |         |  | P5RXSTS[1:0]      | [11:10] | 0b11    |         |
|              |         |  | P6RXSTS[1:0]      | [13:12] | 0b11    |         |
|              |         |  | P7RXSTS[1:0]      | [15:14] | 0b11    |         |
| 0x7C<br>0x7D | 0x003E  | RX Spanning Tree Statistic Register 1 (RSTSR1) | P8RXSTS[1:0]      | [1:0]   | 0b11    | 0x0003  |
|              |         |  | Reserved          | [15:3]  | 0x0000  |         |
| 0x7E<br>0x7F | 0x003F  | TX Spanning Tree Statistic Register (TSTSR)    | TXSTS[8:0]        | [8:0]   | 0x1FF   | 0x01FF  |
|              |         |  | Reserved          | [15:9]  | 0x00    |         |
| 0x80<br>0x81 | 0x0040  | Internal Use                                   | N/A               | [15:0]  | 0x0C18  | 0x0C18  |
| 0x82<br>0x83 | 0x0041  | Internal Use                                   | N/A               | [15:0]  | 0x1120  | 0x1120  |
| 0x84<br>0x85 | 0x0042  | Internal Use                                   | N/A               | [15:0]  | 0x000D  | 0x000D  |
| 0x86<br>0x87 | 0x0043  | Internal Use                                   | N/A               | [15:0]  | 0x000D  | 0x000D  |
| 0x88<br>0x89 | 0x0044  | Reserved                                       | N/A               | [15:0]  | 0x0000  | 0x0000  |
| 0x8A<br>0x8B | 0x0045  | Internal Use                                   | N/A               | [15:0]  | 0x0000  | 0x0000  |
| 0x8C<br>0x8D | 0x0046  | Switch MAC Address Register 0 (SMAR0)          | SWITCH_MAC[15:0]  | [15:0]  | 0x0000  | 0x0000  |
| 0x8E<br>0x8F | 0x0047  | Switch MAC Address Register 1 (SMAR1)          | SWITCH_MAC[31:16] | [15:0]  | 0x0000  | 0x0000  |
| 0x90<br>0x91 | 0x0048  | Switch MAC Address Register 2 (SMAR2)          | SWITCH_MAC[47:32] | [15:0]  | 0x0000  | 0x0000  |
| 0x92<br>0x93 | 0x0049  | Internal Use                                   | Internal Use      | [15:0]  | 0x8899  | 0x8899  |
| 0x94<br>0x95 | 0x004A  | Internal Use                                   | N/A               | [1:0]   | 0b00    | 0x0000  |
|              |         |  | Reserved          | [15:2]  | 0x0000  |         |
| 0x96<br>0x97 | 0x004B  | Internal Use                                   | N/A               | [7:0]   | 0xFF    | 0x01FF  |
|              |         |  | Reserved          | [15:8]  | 0x01    |         |

| EEPROM       | Address | Description                                 | Register Name    | Bits    | Default | Default |
|--------------|---------|---|------------------|---------|---------|---------|
| 0x98<br>0x99 | 0x004C  | Internal Use                                | N/A              | [15:0]  | 0x8369  | 0x8369  |
| 0x9A<br>0x9B | 0x004D  | Switch IP Address Register 0 (SIAR0)        | SW_IP[15:0]      | [15:0]  | 0x0101  | 0x0101  |
| 0x9C<br>0x9D | 0x004E  | Switch IP Address Register 1 (SIAR1)        | SW_IP[31:16]     | [15:0]  | 0xC0A8  | 0xC0A8  |
| 0x9E<br>0x9F | 0x004F  | Internal Use                                | N/A              | [7:0]   | 0x00    | 0x0000  |
|              |         |   | Reserved         | [15:8]  | 0x00    |         |
| 0xA0<br>0xA1 | 0x0050  | P8 GMII Control Register (P8GCR)            | GIPIF_MODE[2:0]  | [2:0]   | 0b000   | 0xF300  |
|              |         |   | Internal Use     | [3]     | 0b0     |         |
|              |         |   | Internal Use     | [4]     | 0b0     |         |
|              |         |   | Internal Use     | [5]     | 0b0     |         |
|              |         |   | Internal Use     | [6]     | 0b0     |         |
|              |         |   | P8_PHY_LINK      | [7]     | 0b0     |         |
|              |         |   | P8_PHY_XFC[1:0]  | [9:8]   | 0b11    |         |
|              |         |   | P8_PHY_SPD       | [10]    | 0b0     |         |
|              |         |   | Internal Use     | [11]    | 0b0     |         |
|              |         |   | P8RXC_DELAY      | [12]    | 0b1     |         |
|              |         |   | P8TXC_DELAY      | [13]    | 0b1     |         |
|              |         |   | GIPIF_MODE[4:3]  | [15:14] | 0b11    |         |
| 0xA2<br>0xA3 | 0x0051  | System Vendor ID Register 0 (SVIDR0)        | VENDOR_ID[15:0]  | [15:0]  | 0x0000  | 0x0000  |
| 0xA4<br>0xA5 | 0x0052  | System Vendor ID Register 1 (SVIDR1)        | VENDOR_ID[31:16] | [15:0]  | 0x0000  | 0x0000  |
| 0xA6<br>0xA7 | 0x0053  | Internal Use                                | N/A              | [15:0]  | 0x7D1B  | 0x7D1B  |
| 0xA8<br>0xA9 | 0x0054  | Internal Use                                | N/A              | [15:0]  | 0x0000  | 0x0000  |
| 0xAA<br>0xAB | 0x0055  | Internal Use                                | N/A              | [15:0]  | 0x0000  | 0x0000  |
| 0xAC<br>0xAD | 0x0056  | Internal Use                                | N/A              | [15:0]  | 0x0000  | 0x0000  |
| 0xAE<br>0xAF | 0x0057  | Internal Use                                | N/A              | [15:0]  | 0x0000  | 0x0000  |
| 0xB0<br>0xB1 | 0x0058  | Port VLAN Index Control Register 0 (PVICR0) | P0PVID[3:0]      | [3:0]   | 0x0     | 0x3210  |
|              |         |   | P1PVID[3:0]      | [7:4]   | 0x1     |         |
|              |         |   | P2PVID[3:0]      | [11:8]  | 0x2     |         |
|              |         |   | P3PVID[3:0]      | [15:12] | 0x3     |         |
| 0xB2<br>0xB3 | 0x0059  | Port VLAN Index Control Register 2 (PVICR1) | P4PVID[3:0]      | [3:0]   | 0x4     | 0x7654  |
|              |         |   | P5PVID[3:0]      | [7:4]   | 0x5     |         |
|              |         |   | P6PVID[3:0]      | [11:8]  | 0x6     |         |
|              |         |   | P7PVID[3:0]      | [15:12] | 0x7     |         |
| 0xB4<br>0xB5 | 0x005A  | Port VLAN Index Control Register 2 (PVICR2) | P8PVID[3:0]      | [3:0]   | 0x8     | 0x0008  |
|              |         |   | Reserved         | [15:4]  | 0x000   |         |
| 0xB6         | 0x005B  | Internal Use                                | N/A              | [8:0]   | 0x000   | 0x0000  |

| EEPROM        | Address           | Description  | Register Name | Bits   | Default | Default |
|---------------|-------------------|--------------|---------------|--------|---------|---------|
| 0xB7          |                   |              | Reserved      | [15:9] | 0x00    |         |
| 0xB8~<br>0xCF | 0x005C~<br>0x0067 | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000  |
| 0xD0~<br>0xFD | 0x0068~<br>0x007E | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000  |
| 0xFE<br>0xFF  | 0x007F            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000  |

## 10.2. Registers List Part II

**Table 35. Registers List Part II**

| Address           | Description                                | Register Name | Bits    | Default | Default |
|-------------------|--|---------------|---------|---------|---------|
| 0x0100            | Reset Control Register (RCR)               | CHIP_RESET    | [0]     | 0b0     | 0x0000  |
|                   |  | SOFT_RESET    | [1]     | 0b0     |         |
|                   |  | MIB_RESET     | [2]     | 0b0     |         |
|                   |  | Reserved      | [15:3]  | 0x0000  |         |
| 0x0101            | Internal Use                               | N/A           | [8:0]   | 0x000   | 0x0000  |
|                   |  | Reserved      | [15:9]  | 0x00    |         |
| 0x0102            | Internal Use                               | N/A           |         | 0x0008  | 0x0008  |
| 0x0103            | Internal Use                               | N/A           | [8:0]   | 0x000   | 0x3000  |
|                   |  | Reserved      | [11:9]  | 0b000   |         |
|                   |  | N/A           | [12]    | 0b1     |         |
|                   |  | N/A           | [13]    | 0b1     |         |
|                   |  | Reserved      | [15:14] | 0b00    |         |
| 0x0104            | Chip Version Control Register (CVCR)       | CHIP_VER[3:0] | [3:0]   | 0x1     | 0x0001  |
|                   |  | Reserved      | [15:4]  | 0x000   |         |
| 0x0105            | Internal Use                               | N/A           | [15:0]  | 0x8369  | 0x8369  |
| 0x0106~<br>0x010B | Reserved                                   | N/A           | [15:0]  | 0x0000  | 0x0000  |
| 0x010C            | Internal Use                               | N/A           | [15:0]  | N/A     | N/A     |
| 0x010D            | Internal Use                               | N/A           | [15:0]  | N/A     | N/A     |
| 0x010E            | Internal Use                               | N/A           | [15:0]  | N/A     | N/A     |
| 0x010F            | Enable VLAN Table Control Register (EVTCT) | EN_VLAN_TBL   | [0]     | 0b0     | 0x0000  |
|                   |  | Reserved      | [15:1]  | 0x0000  |         |
| 0x0110            | Internal Use                               | N/A           | [15:0]  | 0x0000  | 0x0000  |
| 0x0111            | Internal Use                               | N/A           | [15:0]  | 0x0000  | 0x0000  |
| 0x0112            | Internal Use                               | N/A           | [15:0]  | 0x0000  | 0x0000  |
| 0x0113            | Internal Use                               | N/A           | [15:0]  | 0x0000  | 0x0000  |
| 0x0118            | PHY Access Control Register 0 (PHYACR0)    | PHY_EXEC      | [0]     | 0b0     | 0x0000  |
|                   |  | PHY_RW        | [1]     | 0b0     |         |
|                   |  | Reserved      | [15:2]  | 0x0000  |         |
| 0x0119            | PHY Access Control Register 1 (PHYACR1)    | PHY_ADD[4:0]  | [4:0]   | 0x00    | 0x0000  |
|                   |  | Reserved      | [15:5]  | 0x000   |         |



| Address           | Description                             | Register Name      | Bits   | Default | Default |
|-------------------|---|--------------------|--------|---------|---------|
| 0x011A            | PHY Access Control Register 2 (PHYACR2) | PHY_REG[4:0]       | [4:0]  | 0x00    | 0x0000  |
|                   |   | Reserved           | [15:5] | 0x000   |         |
| 0x011B            | PHY Access Control Register 3 (PHYACR3) | PHY_DATA_IN[15:0]  | [15:0] | 0x0000  | 0x0000  |
| 0x011C            | PHY Access Control Register 4 (PHYACR4) | PHY_DATA_OUT[15:0] | [15:0] | 0x0000  | 0x0000  |
| 0x011D~<br>0x011F | Reserved                                | N/A                | [15:0] | 0x0000  | 0x0000  |
| 0x0120            | Port 0 MIB Counter A 0 (P0MIB_CNTA0)    | MIB0_CNTA[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0121            | Port 0 MIB Counter A 1 (P0MIB_CNTA1)    | MIB0_CNTA[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0122            | Port 0 MIB Counter B 0 (P0MIB_CNTA0)    | MIB0_CNTB[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0123            | Port 0 MIB Counter B 1 (P0MIB_CNTA1)    | MIB0_CNTB[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0124            | Port 0 MIB Counter C 0 (P0MIB_CNTA0)    | MIB0_CNTC[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0125            | Port 0 MIB Counter C 1 (P0MIB_CNTA1)    | MIB0_CNTC[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0126            | Port 1 MIB Counter A 0 (P1MIB_CNTA0)    | MIB1_CNTA[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0127            | Port 1 MIB Counter A 1 (P1MIB_CNTA1)    | MIB1_CNTA[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0128            | Port 1 MIB Counter B 0 (P1MIB_CNTA0)    | MIB1_CNTB[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0129            | Port 1 MIB Counter B 1 (P1MIB_CNTA1)    | MIB1_CNTB[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x012A            | Port 1 MIB Counter C 0 (P1MIB_CNTA0)    | MIB1_CNTC[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x012B            | Port 1 MIB Counter C 1 (P1MIB_CNTA1)    | MIB1_CNTC[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x012C            | Port 2 MIB Counter A 0 (P2MIB_CNTA0)    | MIB2_CNTA[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x012D            | Port 2 MIB Counter A 1 (P2MIB_CNTA1)    | MIB2_CNTA[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x012E            | Port 2 MIB Counter B 0 (P2MIB_CNTA0)    | MIB2_CNTB[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x012F            | Port 2 MIB Counter B 1 (P2MIB_CNTA1)    | MIB2_CNTB[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0130            | Port 2 MIB Counter C 0 (P2MIB_CNTA0)    | MIB2_CNTC[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0131            | Port 2 MIB Counter C 1 (P2MIB_CNTA1)    | MIB2_CNTC[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0132            | Port 3 MIB Counter A 0 (P3MIB_CNTA0)    | MIB3_CNTA[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0133            | Port 3 MIB Counter A 1 (P3MIB_CNTA1)    | MIB3_CNTA[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0134            | Port 3 MIB Counter B 0 (P3MIB_CNTA0)    | MIB3_CNTB[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0135            | Port 3 MIB Counter B 1 (P3MIB_CNTA1)    | MIB3_CNTB[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0136            | Port 3 MIB Counter C 0 (P3MIB_CNTA0)    | MIB3_CNTC[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0137            | Port 3 MIB Counter C 1 (P3MIB_CNTA1)    | MIB3_CNTC[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0138            | Port 4 MIB Counter A 0 (P4MIB_CNTA0)    | MIB4_CNTA[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0139            | Port 4 MIB Counter A 1 (P4MIB_CNTA1)    | MIB4_CNTA[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x013A            | Port 4 MIB Counter B 0 (P4MIB_CNTA0)    | MIB4_CNTB[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x013B            | Port 4 MIB Counter B 1 (P4MIB_CNTA1)    | MIB4_CNTB[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x013C            | Port 4 MIB Counter C 0 (P4MIB_CNTA0)    | MIB4_CNTC[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x013D            | Port 4 MIB Counter C 1 (P4MIB_CNTA1)    | MIB4_CNTC[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x013E            | Port 5 MIB Counter A 0 (P5MIB_CNTA0)    | MIB5_CNTA[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x013F            | Port 5 MIB Counter A 1 (P5MIB_CNTA1)    | MIB5_CNTA[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0140            | Port 5 MIB Counter B 0 (P5MIB_CNTA0)    | MIB5_CNTB[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0141            | Port 5 MIB Counter B 1 (P5MIB_CNTA1)    | MIB5_CNTB[31:16]   | [15:0] | 0x0000  | 0x0000  |
| 0x0142            | Port 5 MIB Counter C 0 (P5MIB_CNTA0)    | MIB5_CNTC[15:0]    | [15:0] | 0x0000  | 0x0000  |
| 0x0143            | Port 5 MIB Counter C 1 (P5MIB_CNTA1)    | MIB5_CNTC[31:16]   | [15:0] | 0x0000  | 0x0000  |

| Address | Description                          | Register Name     | Bits   | Default | Default |
|---------|--------------------------------------|-------------------|--------|---------|---------|
| 0x0144  | Port 6 MIB Counter A 0 (P6MIB_CNTA0) | MIB6_CNTA[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x0145  | Port 6 MIB Counter A 1 (P6MIB_CNTA1) | MIB6_CNTA[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x0146  | Port 6 MIB Counter B 0 (P6MIB_CNTB0) | MIB6_CNTB[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x0147  | Port 6 MIB Counter B 1 (P6MIB_CNTB1) | MIB6_CNTB[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x0148  | Port 6 MIB Counter C 0 (P6MIB_CNTC0) | MIB6_CNTC[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x0149  | Port 6 MIB Counter C 1 (P6MIB_CNTC1) | MIB6_CNTC[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x014A  | Port 7 MIB Counter A 0 (P7MIB_CNTA0) | MIB7_CNTA[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x014B  | Port 7 MIB Counter A 1 (P7MIB_CNTA1) | MIB7_CNTA[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x014C  | Port 7 MIB Counter B 0 (P7MIB_CNTB0) | MIB7_CNTB[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x014D  | Port 7 MIB Counter B 1 (P7MIB_CNTB1) | MIB7_CNTB[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x014E  | Port 7 MIB Counter C 0 (P7MIB_CNTC0) | MIB7_CNTC[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x014F  | Port 7 MIB Counter C 1 (P7MIB_CNTC1) | MIB7_CNTC[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x0150  | Port 8 MIB Counter A 0 (P8MIB_CNTA0) | MIB8_CNTA[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x0151  | Port 8 MIB Counter A 1 (P8MIB_CNTA1) | MIB8_CNTA[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x0152  | Port 8 MIB Counter B 0 (P8MIB_CNTB0) | MIB8_CNTB[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x0153  | Port 8 MIB Counter B 1 (P8MIB_CNTB1) | MIB8_CNTB[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x0154  | Port 8 MIB Counter C 0 (P8MIB_CNTC0) | MIB8_CNTC[15:0]   | [15:0] | 0x0000  | 0x0000  |
| 0x0155  | Port 8 MIB Counter C 1 (P8MIB_CNTC1) | MIB8_CNTC[31:16]  | [15:0] | 0x0000  | 0x0000  |
| 0x0156  | Internal Use                         | N/A               | [15:0] | 0x0000  | 0x0000  |
| 0x0157  | Internal Use                         | N/A               | [15:0] | 0x0000  | 0x0000  |
| 0x0158  | Flow Control Status Register (FCSR)  | FLOWCTRL[8:0]     | [8:0]  | 0x000   | 0x0000  |
|         |                                      | Reserved          | [15:9] | 0x00    |         |
| 0x0159  | Port Status Register 0 (PSR0)        | PORT_STATUS0[7:0] | [7:0]  | 0xE0    | 0xE0E0  |
|         |                                      | PORT_STATUS1[7:0] | [15:8] | 0xE0    |         |
| 0x015A  | Port Status Register 1 (PSR1)        | PORT_STATUS2[7:0] | [7:0]  | 0xE0    | 0xE0E0  |
|         |                                      | PORT_STATUS3[7:0] | [15:8] | 0xE0    |         |
| 0x015B  | Port Status Register 2 (PSR2)        | PORT_STATUS4[7:0] | [7:0]  | 0xE0    | 0xE0E0  |
|         |                                      | PORT_STATUS5[7:0] | [15:8] | 0xE0    |         |
| 0x015C  | Port Status Register 3 (PSR3)        | PORT_STATUS6[7:0] | [7:0]  | 0xE0    | 0xE0E0  |
|         |                                      | PORT_STATUS7[7:0] | [15:8] | 0xE0    |         |
| 0x015D  | Port Status Register 4 (PSR4)        | PORT_STATUS8[7:0] | [7:0]  | 0xEE    | 0x00EE  |
|         |                                      | Reserved          | [15:8] | 0x00    |         |
| 0x015E  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x015F  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0160  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0161  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0162  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0163  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0164  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0165  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0166  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0167  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |
| 0x0168  | Internal Use                         | N/A               | [15:0] | N/A     | N/A     |

| Address            | Description  | Register Name    | Bits    | Default     | Default |
|--------------------|--|------------------|---------|-------------|---------|
| 0x0169             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x016A             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x016B             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x016C             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x016D             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x016E             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x016F             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0170             | EEPROM Status Register (EEPSR)                       | EEPROM_EXISTENCE | [0]     | 0b0         | 0x0004  |
|                    |  | Internal Use     | [1]     | 0b0         |         |
|                    |  | EERPOM_RDY       | [2]     | 0b1         |         |
|                    |  | Reserved         | [15:3]  | 0x0000      |         |
| 0x0171             | Internal Use   | N/A              | [3:0]   | 0x0         | 0x0000  |
|                    |  | Reserved         | [15:4]  | 0x000       |         |
| 0x0172             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0173             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0174             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0175             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0176             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0177             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0178             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0179             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x017A             | Internal Use   | N/A              | [15:0]  | N/A         | N/A     |
| 0x0180             | Lookup & VLAN Table Access Control Register (LVTACR) | TABLE_EXEC       | [0]     | 0b0         | 0x0000  |
|                    |  | Reserved         | [7:1]   | 0x00        |         |
|                    |  | TABLE_CMD[2:0]   | [10:8]  | 0b000       |         |
|                    |  | Reserved         | [15:11] | 0x00        |         |
| 0x0182             | Lookup & VLAN Table Data Input Register 0 (LVTDIR0)  | WD[15:0]         | [15:0]  | 0x0000      | 0x0000  |
| 0x0183             | Lookup & VLAN Table Data Input Register 1 (LVTDIR1)  | WD[31:16]        | [15:0]  | 0x0000      | 0x0000  |
| 0x0184             | Lookup & VLAN Table Data Input Register 2 (LVTDIR2)  | WD[47:32]        | [15:0]  | 0x0000      | 0x0000  |
| 0x0185             | Lookup & VLAN Table Data Input Register 3 (LVTDIR3)  | WD[63:48]        | [15:0]  | 0x0000      | 0x0000  |
| 0x0186             | Lookup & VLAN Table Data Input Register 4 (LVTDIR4)  | WD[69:64]        | [5:0]   | 0x00        | 0x00    |
|                    |  | Reserved         | [15:6]  | 0x000       | 0x000   |
| 0x0188             | Lookup & VLAN Table Data Output Register 0 (LVTDOR0) | RD[15:0]         | [15:0]  | 0x0000      | 0x0000  |
| 0x0189             | Lookup & VLAN Table Data Output Register 1 (LVTDOR1) | RD[31:16]        | [15:0]  | 0x0000      | 0x0000  |
| 0x018A             | Lookup & VLAN Table Data Output Register 2 (LVTDOR2) | RD[47:32]        | [15:0]  | 0x0000      | 0x0000  |
| 0x018B –<br>0x018F | Reserved   | N/A              | [15:0]  | 0x0000<br>0 | 0x0000  |
| 0x0190             | Internal Use   | N/A              | [15:0]  | 0x0000      | 0x0000  |

| Address           | Description  | Register Name | Bits   | Default | Default                      |
|-------------------|--------------|---------------|--------|---------|------------------------------|
| 0x0191            | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0192            | Internal Use | N/A           | [15:0] | N/A     | N/A                          |
| 0x0193            | Internal Use | N/A           | [15:0] | N/A     | N/A                          |
| 0x0194            | Internal Use | N/A           | [15:0] | 0x01FF  | 0x01FF                       |
| 0x0195            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0196            | Internal Use | N/A           | [15:0] | 0x0001  | 0x0001                       |
| 0x0197            | Internal Use | N/A           | [15:0] | 0x0001  | 0x0001                       |
| 0x0198            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0199            | Internal Use | N/A           | [15:0] | 0x0040  | 0x0040                       |
| 0x019A            | Internal Use | N/A           | [15:0] | 0xFFFF  | 0xFFFF                       |
| 0x019B            | Internal Use | N/A           | [15:0] | 0xFFFF  | 0xFFFF                       |
| 0x019C            | Internal Use | N/A           | [15:0] | 0xFFFF  | 0xFFFF                       |
| 0x019D            | Internal Use | N/A           | [15:0] | 0x0009  | 0x0009                       |
| 0x019E            | Internal Use | N/A           | [15:0] | 0x4C00  | 0x4C00                       |
| 0x019F            | Internal Use | N/A           | [15:0] | 0x5452  | 0x5452                       |
| 0x01A0~<br>0x01DF | Internal Use | N/A           | [15:0] | N/A     | N/A                          |
| 0x01E0~<br>0x01FF | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0200            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0201            | Internal Use | N/A           | [15:0] | 0x0003  | 0x0003                       |
| 0x0202            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0203            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0204            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0205            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0206            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0207            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0208            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0209            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x020A            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x020B~<br>0x020F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0210~<br>0x021A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x021B~<br>0x021F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0220~<br>0x022A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x022B~<br>0x022F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |

| Address           | Description  | Register Name | Bits   | Default | Default                      |
|-------------------|--------------|---------------|--------|---------|------------------------------|
| 0x0230~<br>0x023A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x023B~<br>0x023F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0240~<br>0x024A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x024B~<br>0x024F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0250~<br>0x025A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x025B~<br>0x025F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0260~<br>0x026A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x026B~<br>0x026F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0270~<br>0x027A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x027B~<br>0x027F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0280~<br>0x028A | Internal Use | N/A           | [15:0] |         | Same as<br>0x0200:<br>0x021A |
| 0x028B~<br>0x028F | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0290            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0291            | Internal Use | N/A           | [15:0] | 0xFFFF  | 0xFFFF                       |
| 0x0292            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0293            | Internal Use | N/A           | [15:0] | 0x0000  | 0x0000                       |
| 0x0294~<br>0xFFFF | Reserved     | N/A           | [15:0] | 0x0000  | 0x0000                       |

### 10.3. Registers Description Part I

#### 10.3.1. 0x0000: Switch Global Control Register (SGCR)

**Table 36. 0x0000: Switch Global Control Register (SGCR)**

| Reg.  | Bits | Name             | Description   | R/W | Default |
|-------|------|------------------|---|-----|---------|
| 0x000 | 0    | EN_BC_STORM_CTRL | Enable Broadcast Storm Filtering Control.<br>Set Enables the broadcast storm filtering control function.<br>0b1: Enable Broadcast storm filtering control<br>0b0: Disable Broadcast storm filtering control | R/W | 0b0     |
|       | 1    | Internal Use     | N/A   | R/W | 0b0     |
|       | 2    | Internal Use     | N/A   | R/W | 0b1     |
|       | 3    | Reserved         |   |     | 0b0     |
|       | 5:4  | MAX_LENGTH[1:0]  | Configures the maximum length of valid packets.<br>0b00: 1522 bytes<br>0b01: 1536 bytes<br>0b10: 1552 bytes<br>0b11: 9216 bytes   | R/W | 0b00    |
|       | 6    | EN_IGMP          | Enables IGMP (DA=01-00-5E-00-00-00 to 01-00-5E-7F-FF-FF) snooping.<br>0b0: Disabled<br>0b1: Enabled   | R/W | 0b0     |
|       | 7    | EN_ARP           | Enables the awareness of ARP packet (EtherType=0x0806).<br>0b0: Disable awareness of ARP packets<br>0b1: Enable awareness of ARP packets  | R/W | 0b0     |
|       | 8    | DIS_BP           | Disables half duplex flow control features.<br>0b0: Enable half duplex flow control features<br>0b1: Disable half duplex flow control features  | R/W | 0b0     |
|       | 9    | JAM_MODE         | There are two half duplex flow control modes. One is BACK-PRESSURE mode, the other is defer mode.<br>0b0: BACK-PRESSURE mode<br>0b1: DEFER mode   | R/W | 0b1     |
|       | 10   | EN_48PASS1       | Enables receiving a packet after 48 consecutive BACK-PRESSURE packets.<br>0b0: No 48 pass 1<br>0b1: Enabled.  | R/W | 0b1     |
|       | 11   | MAX_PAUSE_CNT    | Limits the maximum consecutive pause frame number when congestion occurs.<br>0b0: Limit to maximum of 128 consecutive pause frames.<br>0b1: Un-limit the max consecutive pause frame number.                | R/W | 0b1     |

| Reg.   | Bits     | Name           | Description   | R/W  | Default |
|--------|----------|----------------|---|------|---------|
|        | 12       | EN_MLT_BRD     | Configures the multicast and broadcast packet Egress drop policy. When any of the destination ports of the packet is in a congestion state, this bit controls whether the packet should be dropped at ingress or egress.<br>0b0: Drops the packet at ingress<br>0b1: Drops the packet at egress | R/W  | 0b0     |
|        | 13       | Internal Use   | N/A   | R/W  | 0b1     |
|        | 14       | Internal Use   | N/A   | R/W  | 0b0     |
|        | 15       | Internal Use   | N/A   | R/W  | 0b0     |
| 0x0002 | 8:0      | DIS_LEARN[8:0] | 0b0: Enables learning of packets received from the port<br>0b1: Disables learning of packets received from the port   | R/W  | 0x000   |
|        | 15:9     | Reserved       |   |      | 0x00    |
| 0x0003 | 8:0      | DIS_AGE[8:0]   | 0b0: Enables auto aging of packets received from the port<br>0b1: Disables auto aging of packets received from the port   | R/W  | 0x000   |
|        | 15:9     | Reserved       |   |      | 0x00    |
| 0x0004 | 0        | DROP_UNKNOW_DA | 0b0: Do not drop packets whose DA has not been learned<br>0b1: Drop packets whose DA has not been learned<br><i>Note: Even if the learning function is enabled, the switch will not learn the SA of dropped packets.</i>  | R/W  | 0b0     |
|        | 1        | Internal Use   | N/A   | R/W  | 0b0     |
|        | 2        | Internal Use   | N/A   | R/W  | 0b0     |
|        | 3        | Reserved       |   |      | 0b0     |
|        | 4        | Internal Use   | N/A   | R/W  | 0b0     |
|        | 5        | Internal Use   | N/A   | R/W  | 0b1     |
|        | 6        | Internal Use   | N/A   | R/W  | 0b0     |
|        | 7        | Internal Use   | N/A   | R/W  | 0b0     |
|        | 9:8      | Reserved       |   |      | 0b00    |
|        | 10       | Internal Use   | N/A   | R/W  | 0b0     |
| 15:11  | Reserved |                |   | 0x00 |         |

### 10.3.2. 0x0005 ~ 0x0006: VLAN/Trunk Control Register 0-1 (VTCR0-1)

**Table 37. 0x0005 ~ 0x0006: VLAN/Trunk Control Register 0-1 (VTCR0-1)**

| Reg.   | Bits | Name            | Description   | R/W | Default |
|--------|------|-----------------|---|-----|---------|
| 0x0005 | 0    | EN_VLAN         | Enable VLAN function.<br>When the VLAN function is enabled, the power-on default VLAN topology is 8 Home VLANs for non-EEPROM environments.<br>0b0: Disables the VLAN function<br>0b1: Enables the VLAN function  | R/W | 0b0     |
|        | 1    | VLAN_TAG_AWARE  | IEEE 802.1Q VLAN tag aware.<br>If 802.1Q VLAN aware is enabled, the switch will identify the VLAN by the VID of the VLAN tag for tagged frames, and by the PVID of each ingress port for un-tagged frames. If 802.1Q VLAN aware is disabled, the switch will identify the VLAN by the PVID of each ingress port for all frames.<br>0b0: Disable 802.1Q VLAN aware<br>0b1: Enable 802.1Q VLAN aware  | R/W | 0b1     |
|        | 2    | VLAN_TAG_ADMIT  | Ingress rule for acceptable frame types control.<br>If this parameter is set to 'Admit only VLAN-Tagged Frames', any frames received on that port that carry no VID (i.e., Untagged Frames or Priority-Tagged Frames) are discarded.<br>If this parameter is set to 'Admit all Frames', all incoming Priority-Tagged and Untagged Frames are associated with a VLAN by the ingress rule on the receiving port.<br>0b0: Admit all Frames<br>0b1: Admit only VLAN-Tagged Frames | R/W | 0b0     |
|        | 3    | EN_INGRESS_RULE | Ingress rule for ingress member filtering control.<br>If the EN_INGRESS_RULE is set, then all frames received on a port whose VLAN classification does not include that port in its member set shall be discarded.<br>0b0: Disable ingress member set filtering<br>0b1: Enable ingress member set filtering   | R/W | 0b1     |
|        | 4    | EN_UC_LEAKY     | Unicast Packet Inter-VLAN Leaky Control.<br>Enables inter-VLAN communication for unicast forwarding packets.<br>Normally, inter-VLAN packet switching is not valid. The RTL8369 supports a control bit that enables inter-VLAN communication in the switch without an external router.<br>0b0: Disable<br>0b1: Enable   | R/W | 0b0     |



| Reg.   | Bits  | Name                | Description   | R/W | Default |
|--------|-------|---------------------|---|-----|---------|
|        | 5     | EN_ARP_LEAKY        | ARP broadcast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for ARP broadcast packets (DA=FF-FF-FF-FF-FF-FF and EtherType=0x0806) forwarding.<br>0b0: Disable<br>0b1: Enable<br><i>Note: Before enabling this function, EN_ARP in the SGCR register (0x0000) must be enabled.</i> | R/W | 0b0     |
|        | 6     | EN_IPMC_LEAKY       | IP Multicast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for IP Multicast packet (DA=01-00-5E-00-00-00 to 01-00-5E-7F-FF-FF) forwarding.<br>0b0: Disable<br>0b1: Enable<br><i>Note: Before enabling this function, EN_IGMP in the SGCR register (0x0000) must be enabled.</i>   | R/W | 0b0     |
|        | 7     | Internal Use        | N/A   | R/W | 0b0     |
|        | 11:8  | Internal Use        | N/A   | R/W | 0x0     |
|        | 12    | EN_TG_DROP          | Enables dropping of VLAN tagged packets.<br>0b0: Normal operation<br>0b1: Drop VLAN tagged packets  | R/W | 0b0     |
|        | 13    | Internal Use        | N/A   | R/W | 0b1     |
|        | 15:14 | P8_TAG_CONTROL[1:0] | VLAN tagging un-tagging control.<br>0b00: Keep all packets unchanged<br>0b01: Insert VLAN tag according to the PVID of the Ingress port<br>0b10: Remove VLAN-tagged for tagged frame<br>0b11: Insert priority tag according to the priority of the packet   | R/W | 0b00    |
| 0x0006 | 1:0   | P0_TAG_CONTROL[1:0] | VLAN tagging/un-tagging control.<br>0b00: Keep all packets unchanged<br>0b01: Insert VLAN tag according to the PVID of the Ingress port<br>0b10: Remove VLAN-tagged for tagged frame<br>0b11: Insert priority tag according to the priority of the packet   | R/W | 0b00    |
|        | 3:2   | P1_TAG_CONTROL[1:0] | Same as P0_TAG_CONTROL[1:0]   | R/W | 0b00    |
|        | 5:4   | P2_TAG_CONTROL[1:0] | Same as P0_TAG_CONTROL[1:0]   | R/W | 0b00    |
|        | 7:6   | P3_TAG_CONTROL[1:0] | Same as P0_TAG_CONTROL[1:0]   | R/W | 0b00    |
|        | 9:8   | P4_TAG_CONTROL[1:0] | Same as P0_TAG_CONTROL[1:0]   | R/W | 0b00    |
|        | 11:10 | P5_TAG_CONTROL[1:0] | Same as P0_TAG_CONTROL[1:0]   | R/W | 0b00    |
|        | 13:12 | P6_TAG_CONTROL[1:0] | Same as P0_TAG_CONTROL[1:0]   | R/W | 0b00    |
|        | 15:14 | P7_TAG_CONTROL[1:0] | Same as P0_TAG_CONTROL[1:0]   | R/W | 0b00    |

### 10.3.3. 0x0007: Port Mirror Control Register (PMCR)

**Table 38. 0x0007: Port Mirror Control Register (PMCR)**

| Reg.   | Bits  | Name              | Description  | R/W | Default |
|--------|-------|-------------------|--|-----|---------|
| 0x0007 | 3:0   | SOURCE_PORT[3:0]  | Select the source port to be mirrored.   | R/W | 0x0     |
|        | 7:4   | MONITOR_PORT[3:0] | Select the monitor port.   | R/W | 0x0     |
|        | 8     | MIRROR_RX         | Enable the mirror function on RX of the source port.<br>0b0: Disable<br>0b1: Enable  | R/W | 0b0     |
|        | 9     | MIRROR_TX         | Enable the mirror function on TX of the source port.<br>0b0: Disable<br>0b1: Enable  | R/W | 0b0     |
|        | 10    | MIRROR_SPC        | Enable forwarding of RX pause frames to mirror port.<br>0b0: Disable<br>0b1: Enable  | R/W | 0b0     |
|        | 11    | MIRROR_ISO        | Enable isolation of TX traffic on the monitor port.<br>0b0: Normal operation<br>0b1: The monitor port will accept only packets from the source port. Other packets destined to the monitor port will be dropped. | R/W | 0b0     |
|        | 14:12 | Reserved          |  |     | 0b000   |
|        | 15    | Internal Use      | N/A  | R/W | 0b0     |

### 10.3.4. 0x0009 ~ 0x000E: QoS Control Register 0-5 (QCR0-5)

**Table 39. 0x0009 ~ 0x000E: QoS Control Register 0-5 (QCR0-5)**

| Reg.   | Bits | Name              | Description  | R/W | Default |
|--------|------|-------------------|--|-----|---------|
| 0x0009 | 0    | EN_QOS            | Enable the QOS function.<br>0b0: Disable all QOS functions<br>0b1: Enable QOS functions  | R/W | 0b0     |
|        | 1    | Internal Use      | N/A  | R/W | 0b0     |
|        | 2    | EN_PORT_PRI       | Enable port priority QOS.<br>When the bit is set, the PORT_PRI register will be used to classify the priority of the packets.<br>0b0: Disable<br>0b1: Enable<br><i>Note: EN_QOS in Register QCR0 (0x0009) must be enabled first.</i>   | R/W | 0b0     |
|        | 3    | EN_DS_PRI         | Enable IP Differential Service based priority classification.<br>When this bit is set, the TOS[63:0] field of IP packets will be used to classify the priority of the packets.<br>0b0: Disable<br>0b1: Enable<br><i>Note: EN_QOS in Register QCR0 (0x0009) must be enabled first.</i>  | R/W | 0b0     |
|        | 4    | EN_1Q_PRI         | Enable 802.1Q VLAN tag base priority classification.<br>When the bit is set, the VLAN tag is compared with PRI_THRESHOLD[2:0]. If the priority field in the VLAN tag > PRI_THRESHOLD then the packet is a high priority packet. Other cases are classified as low priority packets.<br>0b0: Disable<br>0b1: Enable<br><i>Note: EN_QOS in Register QCR0 (0x0009) must be enabled first.</i> | R/W | 0b0     |
|        | 7:6  | QWEIGHT[1:0]      | The ratio of high priority packet and low priority packet to send when QOS is enabled.<br>0b00: 4:1<br>0b01: 8:1<br>0b10: 16:1<br>0b11: Unlimited  | R/W | 0b00    |
|        | 15:8 | VLAN_PRI_TAB[7:0] | Sets the VLAN tag user priority field to high/low priority.<br>For example, if<br>VLAN_PRI_TAB[7:0]=0b10101010, that means that packets with VLAN tag<br>USER_PRIORITY[2:0]=0x1, 0x3, 0x5, 0x7 are high priority packets.<br>0b0: Low priority<br>0b1: High priority   | R/W | 0xF0    |

| Reg.   | Bits | Name          | Description  | R/W | Default |
|--------|------|---------------|--|-----|---------|
| 0x000A | 8:0  | PORT_PRI[8:0] | The priority of the ports when EN_PORT_PRI is set.<br>0b0: Low priority<br>0b1: High priority  | R/W | 0x000   |
|        | 15:9 | Reserved      |  |     | 0x00    |
| 0x000B | 15:0 | TOS[15:0]     | The IP Differential Service table.<br>TOS[0] indicates the priority of Differential Service code 000000                                  | R/W | 0x0000  |
| 0x000C | 15:0 | TOS[31:16]    | TOS[1] indicates the priority of Differential Service code 000001  | R/W | 0x0000  |
| 0x000D | 15:0 | TOS[47:32]    | TOS[32] indicates the priority of Differential Service code 100000<br>TOS[63] indicates the priority of Differential Service code 111111 | R/W | 0x0000  |
| 0x000E | 15:0 | TOS[63:48]    | Etc....<br>0b0: Low priority<br>0b1: High priority   | R/W | 0x0000  |

### 10.3.5. 0x000F ~ 0x0010: MAC Control Packet Control Register 0-1 (MCPCR0-1)

**Table 40. 0x000F ~ 0x0010: MAC Control Packet Control Register 0-1 (MCPCR0-1)**

| Reg.   | Bits | Name                | Description   | R/W | Default        |
|--------|------|---------------------|---|-----|----------------|
| 0x000F | 15:0 | MLTID_ST[7:0][1:0]  | The forwarding control for well-known multicast addresses (0180C2000000~0180C200000F).<br>{MLTID_ST[n][1:0]} indicates forwarding of 0180C200000n addressed packets.  | R/W | 0x5541 (strap) |
| 0x0010 | 15:0 | MLTID_ST[15:8][1:0] | For n=1, 0180C2000001,<br>MCPCR0[3:2]=MLTID_ST[1][1:0], Pause frames are always filtered when configured as 0b01 (Forward).<br>For n =2, 0180C2000002,<br>MCPCR0[5:4]=MLTID_ST[1][1:0], packets are always filtered when configured as 0b01 (Forward).<br>MLTD_ST[n][1:0]=0b00: Drop<br>MLTD_ST[n][1:0]=0b01: Forward<br>MLTD_ST[n][1:0]=Others: Reserved | R/W | 0x5555 (strap) |

### 10.3.6. 0x0011 ~ 0x0015: Port Advertising Ability Control Register 0-4 (PAACR0-4)

**Table 41. 0x0011 ~ 0x0015: Port Advertising Ability Control Register 0-4 (PAACR0-4)**

| Reg.   | Bits | Name                              | Description  | R/W | Default |
|--------|------|-----------------------------------|--|-----|---------|
| 0x0011 | 0    | Port0_Ability[0]<br>(Port0_AN)    | Enables auto negotiation.<br>This bit will be reflected in PHY register 0.12.<br>0b0: Disable Auto negotiation<br>0b1: Enable Auto negotiation   | R/W | 0b1     |
|        | 1    | Port0_Ability[1]<br>(Port0_10H)   | Enables 10M half duplex mode ability.<br>This bit will be reflected in PHY register 4.5<br>0b0: Disable 10M half duplex mode ability<br>0b1: Enable 10M half duplex mode ability       | R/W | 0b1     |
|        | 2    | Port0_Ability[2]<br>(Port0_10F)   | Enables 10M full duplex mode ability.<br>This bit will be reflected in PHY register 4.6<br>0b0: Disable 10M full duplex mode ability<br>0b1: Enable 10M full duplex mode ability       | R/W | 0b1     |
|        | 3    | Port0_Ability[3]<br>(Port0_100H)  | Enables 100M half duplex mode ability.<br>This bit will be reflected in PHY register 4.7<br>0b0: Disable 100M half duplex mode ability<br>0b1: Enable 100M half duplex mode ability    | R/W | 0b1     |
|        | 4    | Port0_Ability[4]<br>(Port0_100F)  | Enables 100M full duplex mode ability<br>This bit will be reflected in PHY register 4.8<br>0b0: Disable 100M full duplex mode ability<br>0b1: Enable 100M full duplex mode ability     | R/W | 0b1     |
|        | 5    | Port0_Ability[5]<br>(Port0_1000F) | Enables 1000M full duplex mode ability.<br>This bit will be reflected in PHY register 9.9<br>0b0: Disable 1000M full duplex mode ability<br>0b1: Enable 1000M full duplex mode ability | R/W | 0b1     |
|        | 6    | Port0_Ability[6] (Port0_FC)       | Enables flow control ability.<br>This bit will be reflected in PHY register 4.10   | R/W | 0b1     |
|        | 7    | Port0_Ability[7]<br>(Port0_ASYFC) | Enables flow control ability.<br>This bit will be reflected in PHY register 4.11   | R/W | 0b1     |
|        | 15:8 | Port1_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
| 0x0012 | 7:0  | Port2_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
|        | 15:8 | Port3_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
| 0x0013 | 7:0  | Port4_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
|        | 15:8 | Port5_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
| 0x0014 | 7:0  | Port6_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
|        | 15:8 | Port7_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
| 0x0015 | 7:0  | Port8_Ability[7:0]                | Same as Port0_Ability[7:0]   | R/W | 0xFF    |
|        | 15:8 | Reserved                          |  |     | 0x00    |

### 10.3.7. 0x0016/0018/.../0034: VLAN ID Configuration Register 0-15 (VIDCR0-15)

**Table 42. 0x0016/0018/.../0034: VLAN ID Configuration Register 0-15 (VIDCR0-15)**

| Reg.   | Bits  | Name        | Description               | R/W | Default |
|--------|-------|-------------|---------------------------|-----|---------|
| 0x0016 | 11:0  | VID0[11:0]  | The VID of VLAN group 0.  | R/W | 0x100   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0018 | 11:0  | VID1[11:0]  | The VID of VLAN group 1.  | R/W | 0x101   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x001A | 11:0  | VID2[11:0]  | The VID of VLAN group 2.  | R/W | 0x102   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x001C | 11:0  | VID3[11:0]  | The VID of VLAN group 3.  | R/W | 0x103   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x001E | 11:0  | VID4[11:0]  | The VID of VLAN group 4.  | R/W | 0x104   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0020 | 11:0  | VID5[11:0]  | The VID of VLAN group 5.  | R/W | 0x105   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0022 | 11:0  | VID6[11:0]  | The VID of VLAN group 6.  | R/W | 0x106   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0024 | 11:0  | VID7[11:0]  | The VID of VLAN group 7.  | R/W | 0x107   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0026 | 11:0  | VID8[11:0]  | The VID of VLAN group 8.  | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0028 | 11:0  | VID9[11:0]  | The VID of VLAN group 9.  | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x002A | 11:0  | VID10[11:0] | The VID of VLAN group 10. | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x002C | 11:0  | VID11[11:0] | The VID of VLAN group 11. | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x002E | 11:0  | VID12[11:0] | The VID of VLAN group 12. | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0030 | 11:0  | VID13[11:0] | The VID of VLAN group 13. | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0032 | 11:0  | VID14[11:0] | The VID of VLAN group 14. | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |
| 0x0034 | 11:0  | VID15[11:0] | The VID of VLAN group 15. | R/W | 0x000   |
|        | 15:12 | Reserved    |                           |     | 0x0     |

### 10.3.8. 0x0017/0019/.../0035: VLAN Member Configuration Register 0-15 (VMCR0-15)

**Table 43. 0x0017/0019/.../0035: VLAN Member Configuration Register 0-15 (VMCR0-15)**

| Reg.   | Bits | Name          | Description                           | R/W | Default |
|--------|------|---------------|---------------------------------------|-----|---------|
| 0x0017 | 8:0  | Member0[8:0]  | The VLAN member set of VLAN group 0.  | R/W | 0x081   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0019 | 8:0  | Member1[8:0]  | The VLAN member set of VLAN group 1.  | R/W | 0x082   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x001B | 8:0  | Member2[8:0]  | The VLAN member set of VLAN group 2.  | R/W | 0x084   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x001D | 8:0  | Member3[8:0]  | The VLAN member set of VLAN group 3.  | R/W | 0x088   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x001F | 8:0  | Member4[8:0]  | The VLAN member set of VLAN group 4.  | R/W | 0x090   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0021 | 8:0  | Member5[8:0]  | The VLAN member set of VLAN group 5.  | R/W | 0x0A0   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0023 | 8:0  | Member6[8:0]  | The VLAN member set of VLAN group 6.  | R/W | 0x0C0   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0025 | 8:0  | Member7[8:0]  | The VLAN member set of VLAN group 7.  | R/W | 0x0FF   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0027 | 8:0  | Member8[8:0]  | The VLAN member set of VLAN group 8.  | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0029 | 8:0  | Member9[8:0]  | The VLAN member set of VLAN group 9.  | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x002B | 8:0  | Member10[8:0] | The VLAN member set of VLAN group 10. | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x002D | 8:0  | Member11[8:0] | The VLAN member set of VLAN group 11. | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x002F | 8:0  | Member12[8:0] | The VLAN member set of VLAN group 12. | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0031 | 8:0  | Member13[8:0] | The VLAN member set of VLAN group 13. | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0033 | 8:0  | Member14[8:0] | The VLAN member set of VLAN group 14. | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |
| 0x0035 | 8:0  | Member15[8:0] | The VLAN member set of VLAN group 15. | R/W | 0x000   |
|        | 15:9 | Reserved      |                                       |     | 0x00    |

### 10.3.9. 0x0036 ~ 0x0037: LED Control Register 0-1 (LCR0-1)

**Table 44. 0x0036 ~ 0x0037: LED Control Register 0-1 (LCR0-1)**

| Reg.   | Bits  | Name            | Description  | R/W | Default |
|--------|-------|-----------------|--|-----|---------|
| 0x0036 | 1:0   | LED_MODE[1:0]   | LED mode configuration.<br>0b00: DUPLEX/COL, LINK/ACT, 1000M, 100M/10M<br>0b01: DUPLEX/COL, 1000M LINK/ACT, 100M LINK/ACT, 10M LINK/ACT.<br>0b10: Bicolor LED (1000M+Link/Act, 100M/10M+Link/ACT), NC, NC, NC.<br>0b11: Serial LED mode. | R/W | 0b00    |
|        | 2     | LED_BLINK_TIME  | LED blink time configuration.<br>0b0: 43 msec.<br>0b1: 120 msec.   | R/W | 0b0     |
|        | 3     | LED_RESET_BLINK | LED behavior at power on reset.<br>0b0: LED does not blink during power on reset<br>0b1: LED blinks during power on reset  | R/W | 0b1     |
|        | 5:4   | GPLED0[1:0]     | General purpose LED behavior configuration.<br>These registers are only valid when LED_MODE=0b11.  | R/W | 0b00    |
|        | 7:5   | GPLED1[1:0]     |  | R/W | 0b00    |
|        | 9:8   | GPLED2[1:0]     |  | R/W | 0b00    |
|        | 11:10 | GPLED3[1:0]     |  | R/W | 0b00    |
|        |       | 12              | Internal Use   | N/A | R/W     |
|        | 15:13 | Reserved        |  |     | 0b000   |
| 0x0037 | 3:0   | Internal Use    | N/A  | R/W | 0x5     |
|        | 7:4   | Internal Use    |  | R/W | 0x0     |
|        | 11:8  | Internal Use    |  | R/W | 0x3     |
|        | 15:12 | Internal Use    |  | R/W | 0x4     |

### 10.3.10. 0x0038 ~ 0x003C: MIB Counter Control Register 0-4 (MCCR0-4)

**Table 45. 0x0038 ~ 0x003C: MIB Counter Control Register 0-4 (MCCR0-4)**

| Reg.   | Bits | Name           | Description   | R/W | Default |
|--------|------|----------------|---|-----|---------|
| 0x0038 | 1:0  | MIB0_SELA[1:0] | Defines the MIB counter CNTA of port 0.<br>0b00: TX byte count<br>0b01: TX packet count<br>Others: Reserved | R/W | 0b01    |
|        | 3:2  | MIB0_SELB[1:0] | Defines the MIB counter CNTB of port 0.<br>0b00: RX byte count<br>0b01: RX packet count<br>Others: Reserved | R/W | 0b01    |



| Reg.   | Bits  | Name            | Description   | R/W | Default |
|--------|-------|-----------------|---|-----|---------|
|        | 5:4   | MIB0_SELCA[1:0] | Defines the MIB counter CNTC of port 0.<br>0b00: RX error packet count<br>0b01: RX drop packet count<br>0b10: Collision count<br>0b11: Reserved | R/W | 0b00    |
|        | 7:6   | Reserved        |   |     | 0b00    |
|        | 9:8   | MIB1_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 11:10 | MIB1_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 13:12 | MIB1_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 15:14 | Reserved        |   |     | 0b00    |
| 0x0039 | 1:0   | MIB2_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 3:2   | MIB2_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 5:4   | MIB2_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 7:6   | Reserved        |   |     | 0b00    |
|        | 9:8   | MIB3_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 11:10 | MIB3_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 13:12 | MIB3_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 15:14 | Reserved        |   |     | 0b00    |
| 0x003A | 1:0   | MIB4_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 3:2   | MIB4_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 5:4   | MIB4_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 7:6   | Reserved        |   |     | 0b00    |
|        | 9:8   | MIB5_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 11:10 | MIB5_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 13:12 | MIB5_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 15:14 | Reserved        |   |     | 0b00    |
| 0x003B | 1:0   | MIB6_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 3:2   | MIB6_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 5:4   | MIB6_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 7:6   | Reserved        |   |     | 0b00    |
|        | 9:8   | MIB7_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 11:10 | MIB7_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 13:12 | MIB7_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 15:14 | Reserved        |   |     | 0b00    |
| 0x003C | 1:0   | MIB8_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b01    |
|        | 3:2   | MIB8_SELCB[1:0] | Same as MIB0_SELCB[1:0].  | R/W | 0b01    |
|        | 5:4   | MIB8_SELCA[1:0] | Same as MIB0_SELCA[1:0].  | R/W | 0b00    |
|        | 15:6  | Reserved        |   |     | 0b00    |

### 10.3.11. 0x003D ~ 0x003E: RX Spanning Tree Status Register 0-1 (RSTSR0-1)

**Table 46. 0x003D ~ 0x003E: RX Spanning Tree Status Register 0-1 (RSTSR0-1)**

| Reg.   | Bits  | Name         | Description  | R/W | Default |
|--------|-------|--------------|--|-----|---------|
| 0x003D | 1:0   | P0RXSTS[1:0] | 0b00: Disable<br>0b01: Blocking/Listening<br>0b10: Learning<br>0b11: Normal receiving. | R/W | 0b11    |
|        | 3:2   | P1RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
|        | 5:4   | P2RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
|        | 7:6   | P3RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
|        | 9:8   | P4RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
|        | 11:10 | P5RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
|        | 13:12 | P6RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
| 0x003E | 15:14 | P7RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
|        | 1:0   | P8RXSTS[1:0] | Same as P0RXSTS[1:0]   | R/W | 0b11    |
|        | 15:2  | Reserved     |  |     | 0x0000  |

### 10.3.12. 0x003F: TX Spanning Tree Status Register (TSTSR)

**Table 47. 0x003F: TX Spanning Tree Status Register (TSTSR)**

| Reg.   | Bits | Name       | Description  | R/W | Default |
|--------|------|------------|--|-----|---------|
| 0x003F | 8:0  | TXSTS[8:0] | 0b0: Stop forwarding for port n<br>0b1: Normal forwarding for port n | R/W | 0x1FF   |
|        | 15:9 | Reserved   |  |     | 0x00    |

### 10.3.13. 0x0046 ~ 0x0048: Switch MAC Address Register 0-3 (SMAR0-3)

**Table 48. 0x0046 ~ 0x0048: Switch MAC Address Register 0-3 (SMAR0-3)**

| Reg.   | Bits  | Name              | Description   | R/W | Default |
|--------|-------|-------------------|---|-----|---------|
| 0x0046 | 15:0  | SWITCH_MAC[15:0]  | Switch MAC address configuration.<br>For example, if the Switch MAC Address=12-34-56-78-9A-BC.<br>SWITCH_MAC[15:0]=0x3412<br>SWITCH_MAC[31:16]=0x7856<br>SWITCH_MAC[47:32]=0xBC9A | R/W | 0x0000  |
| 0x0047 | 31:16 | SWITCH_MAC[31:16] |   | R/W | 0x0000  |
| 0x0048 | 47:32 | SWITCH_MAC[47:32] |   | R/W | 0x0000  |

### 10.3.14. 0x004D ~ 0x004E: Switch IP Address Register 0-1 (SIAR0-1)

**Table 49. 0x004D ~ 0x004E: Switch IP Address Register 0-1 (SIAR0-1)**

| Reg.   | Bits | Name         | Description  | R/W | Default |
|--------|------|--------------|--|-----|---------|
| 0x004D | 15:0 | SW_IP[15:0]  | The IP address of the switch. The default IP is 192.168.1.1<br>For example, if the Switch IP Address=192.168.1.2=C0.A8.01.02.<br>SWITCH_IP[31:16]=0xC0A8.<br>SWITCH_IP[15:0]=0x0101. | R/W | 0x0101  |
| 0x004E | 15:0 | SW_IP[31:16] |  | R/W | 0xC0A8  |

### 10.3.15. 0x0050: Port 8 GMII Control Register (P8GCR)

**Table 50. 0x0050: Port 8 GMII Control Register (P8GCR)**

| Reg.   | Bits | Name            | Description   | R/W | Default            |
|--------|------|-----------------|---|-----|--------------------|
| 0x0050 | 2:0  | GPIF_MODE[2:0]  | General Purpose Interface mode configuration bit 2-0:<br>Configures the General Purpose interface as GMII/RGMII/MII PHY when GPIF_MODE[4:3]=0b11.<br><i>Note that MII PHY mode only supports 100Mbps mode.</i><br>0b000: GMII/MII MAC Mode<br>0b001: RGMII<br>0b100: MII PHY Mode<br>Others: Reserved   | R/W | 0b000              |
|        | 3    | Internal Use    |   | R/W | 0b0                |
|        | 4    | Internal Use    |   | R/W | 0b0                |
|        | 5    | Internal Use    |   | R/W | 0b0                |
|        | 6    | Internal Use    |   | R/W | 0b0                |
|        | 7    | P8_PHY_LINK     | Configures the link status of port8 when GPIF_MODE[2:0]=0b100.<br>0b0: Link down<br>0b1: Link up  | R/W | 0b0                |
|        | 9:8  | P8_PHY_XFC[1:0] | Enables flow control of port8 when GPIF_MODE[2:0]=0b100.<br>0b00 – TX/RX 802.3x flow control are disabled.<br>0b01 – TX 802.3x flow control is disabled and RX 802.3x flow control is enabled.<br>0b10 –TX 802.3x flow control is enabled and RX 802.3x flow control is disabled.<br>0b10: TX 802.3x flow control is enabled and RX 802.3x flow control is disabled.<br>0b11 – TX/RX 802.3x flow control are enabled. | R/W | 0b11               |
|        | 10   | P8_PHY_SPD      | Configures the speed of port8 when GPIF_MODE[2:0]=0b100.<br>0b00: 10M<br>0b01: 100M   | R/W | 0b0<br>(strapping) |
|        | 11   | Internal Use    |   | R/W | 0b0                |

| Reg. | Bits  | Name           | Description  | R/W | Default             |
|------|-------|----------------|--|-----|---------------------|
|      | 12    | P8RXC_DELAY    | RGMII timing compensation. The compensation is only valid when GMII_MODE= 0b001.<br>0b0: Disable<br>0b1: To add a 1.5ns delay on P8RXC | R/W | 0b1<br>(strapping)  |
|      | 13    | P8TXC_DELAY    | RGMII timing compensation. The compensation is only valid when GMII_MODE= 0b001.<br>0b0: Disable<br>0b1: To add a 1.5ns delay on P8TXC | R/W | 0b1<br>(strapping)  |
|      | 15:14 | GPIF_MODE[4:3] | 0b11: MII/GMII/RGMII mode<br>Others: reserved.   | R/W | 0b11<br>(strapping) |

### 10.3.16. 0x0058 ~ 0x5A: Port VLAN Index Control Register 0-2 (PVICR0-2)

**Table 51. 0x0058 ~ 0x005A: Port VLAN Index Control Register 0-2 (PVICR0-2)**

| Reg.   | Bits  | Name        | Description  | R/W | Default |
|--------|-------|-------------|--|-----|---------|
| 0x0058 | 3:0   | P0PVID[3:0] | When EN_VLAN_TBL=0, P0PVID[3:0] can be configured from 0x0 to 0xF.<br>When EN_VLAN_TBL=1, P0PVID[3:0] is fixed as 0x0 (used to point to the VID of register VIDCR0 (0x0016)). The switch uses this VID as an index to find the member set in the 4096 VLAN tables.           | R/W | 0x0     |
|        | 7:4   | P1PVID[3:0] | When EN_VLAN_TBL=0, P1PVID[3:0] can be configured from 0x0 to 0xF.<br>When EN_VLAN_TBL=1, P1PVID[3:0] is fixed as 0x1 (used to point to the VID of register VIDCR1 (0x0018)). The switch uses this VID as an index to find the member set in the 4096 VLAN tables.           | R/W | 0x1     |
|        | 11:8  | P2PVID[3:0] | When EN_VLAN_TBL=0, P2PVID[3:0] can be configured from 0x0 to 0xF.<br>When EN_VLAN_TBL=1, P2PVID[3:0] is fixed as 0x2 (used to point to the VID of register VIDCR2 (0x001A)). The switch uses this VID as an index to find the member set in the 4096 VLAN tables.           | R/W | 0x2     |
|        | 15:12 | P3PVID[3:0] | When EN_VLAN_TBL=0, P3PVID[3:0] could be configured from 0x0 to 0xF.<br>When EN_VLAN_TBL=1, P3PVID[3:0] is fixed as 0x3. Which is used to point to the VID of register VIDCR3 (0x001C). The switch uses this VID as an index to find the member set in the 4096 VLAN tables. | R/W | 0x3     |
| 0x0059 | 3:0   | P4PVID[3:0] | Same as P0PVID[3:0]  | R/W | 0x4     |
|        | 7:4   | P5PVID[3:0] | Same as P0PVID[3:0]  | R/W | 0x5     |
|        | 11:8  | P6PVID[3:0] | Same as P0PVID[3:0]  | R/W | 0x6     |
|        | 15:12 | P7PVID[3:0] | Same as P0PVID[3:0]  | R/W | 0x7     |

| Reg.   | Bits | Name        | Description         | R/W | Default |
|--------|------|-------------|---------------------|-----|---------|
| 0x005A | 3:0  | P8PVID[3:0] | Same as POPVID[3:0] | R/W | 0x8     |
|        | 15:4 | Reserved    |                     | R/W | 0x000   |

## 10.4. Registers Description Part II

### 10.4.1. 0x0100: Reset Control Register (RCR)

Table 52. 0x0100: Reset Control Register (RCR)

| Reg.   | Bits | Name       | Description   | R/W  | Default |
|--------|------|------------|---|------|---------|
| 0x0100 | 0    | CHIP_RESET | Reset the system to the power-on initial state.<br>- Download configuration from strap pin and EEPROM<br>- Start embedded SRAM BIST (Build In Self Test)<br>- Clear all the Lookup and VLAN tables<br>- Reset all registers to default values<br>- Restart auto-negotiation process<br>0b0: Normal<br>0b1: Start chip reset | W/SC | 0b0     |
|        | 1    | SOFT_RESET | Soft Reset.<br>A soft reset will reset the system similar to a power-on reset except that the user configuration will not be cleared:<br>- Restart the auto-negotiation process<br>- Clear FIFO and re-start packet buffer link list<br>0b0: Normal<br>0b1: Start soft reset  | W/SC | 0b0     |
|        | 2    | MIB_RESET  | Reset the MIB counter.<br>0b0: Normal<br>0b1: Reset the MIB counter   | W/SC | 0b0     |
|        | 15:3 | Reserved   |   |      | 0x0000  |

### 10.4.2. 0x0104: Chip Version Control Register (CVCR)

Table 53. 0x0104: Chip Version Control Register (CVCR)

| Reg.   | Bits | Name          | Description  | R/W | Default |
|--------|------|---------------|--|-----|---------|
| 0x0104 | 3:0  | CHIP_VER[3:0] | Chip version indication.<br>This register shows the version number of this chip. | RO  | 0x1     |
|        | 15:4 | Reserved      |  |     | 0x000   |

### 10.4.3. 0x010F: Enable VLAN Table Control Register (EVTCR)

**Table 54. 0x010F: Enable VLAN Table Control Register (EVTCR)**

| Reg.   | Bits | Name        | Description  | R/W | Default |
|--------|------|-------------|--|-----|---------|
| 0x010F | 0    | EN_VLAN_TBL | Enables 4096 VLAN tables.<br>0b0: Disable<br>0b1: Enable | R/W | 0b0     |
|        | 15:1 | Reserved    |  |     | 0x0000  |

### 10.4.4. 0x0118 ~ 0x011C: PHY Access Control Register 0-4 (PHYACR0-4)

**Table 55. 0x0118 ~ 0x011C: PHY Access Control Register 0-4 (PHYACR0-4)**

| Reg.   | Bits | Name               | Description   | R/W | Default |
|--------|------|--------------------|---|-----|---------|
| 0x0118 | 0    | PHY_EXEC           | Command to access the PHY register according to PHY_RW, PHY_ADD, PHY_REG, or PHY_DATA_OUT. This bit is self-cleared once the access is complete.<br>0b0: Access complete<br>0b1: Start to access PHY register | R/W | 0b0     |
|        | 1    | PHY_RW             | PHY register read/write command.<br>0b1: The access is a write access.<br>0b0: The access is a read access.   | R/W | 0b0     |
|        | 15:2 | Reserved           |   |     | 0x0000  |
| 0x0119 | 4:0  | PHY_ADDR[4:0]      | PHY address to be accessed.   | R/W | 0x00    |
|        | 15:5 | Reserved           |   |     | 0x000   |
| 0x011A | 4:0  | PHY_REG[4:0]       | PHY register to be accessed.  | R/W | 0x00    |
|        | 15:5 | Reserved           |   |     | 0x000   |
| 0x011B | 15:0 | PHY_DATA_IN[15:0]  | Data read from the PHY register.<br>This register is only valid when the access is a write access.  | R/W | 0x0000  |
| 0x011C | 15:0 | PHY_DATA_OUT[15:0] | Data to write to the PHY register.<br>This register is only valid when the access is a write access.  | RO  | 0x0000  |

### 10.4.5. 0x0120 ~ 0x0155: Port *n* MIB Counter (P*n*MIB\_CNTA, P*n*MIB\_CNTB, and P*n*MIB\_CNTC; *n*=0 - 8)

**Table 56. 0x0120 ~ 0x0155: Port *n* MIB Counter (P*n*MIB\_CNTA, P*n*MIB\_CNTB, and P*n*MIB\_CNTC; *n*=0 - 8)**

| Reg.  | Bits | Name             | Description                        | R/W | Default |
|---|------|------------------|------------------------------------|-----|---------|
| <b>Port 0 MIB Counter A 0-1 (P0MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x0120  | 15:0 | MIB0_CNTA[15:0]  | LSB of Port 0 MIB counter group A. | RO  | 0x0000  |
| 0x0121  | 15:0 | MIB0_CNTA[31:16] | MSB of Port 0 MIB counter group A. | RO  | 0x0000  |
| <b>Port 0 MIB Counter B 0-1 (P0MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x0122  | 15:0 | MIB0_CNTB[15:0]  | LSB of Port 0 MIB counter group B. | RO  | 0x0000  |

| Reg.  | Bits | Name             | Description                        | R/W | Default |
|---|------|------------------|------------------------------------|-----|---------|
| 0x0123  | 15:0 | MIB0_CNTB[31:16] | MSB of Port 0 MIB counter group B. | RO  | 0x0000  |
| <b>Port 0 MIB Counter C 0-1 (P0MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x0124  | 15:0 | MIB0_CNTC[15:0]  | LSB of Port 0 MIB counter group C. | RO  | 0x0000  |
| 0x0125  | 15:0 | MIB0_CNTC[31:16] | MSB of Port 0 MIB counter group C. | RO  | 0x0000  |
| <b>Port 1 MIB Counter A 0-1 (P1MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x0126  | 15:0 | MIB1_CNTA[15:0]  | LSB of Port 1 MIB counter group A. | RO  | 0x0000  |
| 0x0127  | 15:0 | MIB1_CNTA[31:16] | MSB of Port 1 MIB counter group A. | RO  | 0x0000  |
| <b>Port 1 MIB Counter B 0-1 (P1MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x0128  | 15:0 | MIB1_CNTB[15:0]  | LSB of Port 1 MIB counter group B. | RO  | 0x0000  |
| 0x0129  | 15:0 | MIB1_CNTB[31:16] | MSB of Port 1 MIB counter group B. | RO  | 0x0000  |
| <b>Port 1 MIB Counter C 0-1 (P1MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x012A  | 15:0 | MIB0_CNTC[15:0]  | LSB of Port 1 MIB counter group C. | RO  | 0x0000  |
| 0x012B  | 15:0 | MIB0_CNTC[31:16] | MSB of Port 1 MIB counter group C. | RO  | 0x0000  |
| <b>Port 2 MIB Counter A 0-1 (P2MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x012C  | 15:0 | MIB2_CNTA[15:0]  | LSB of Port 2 MIB counter group A. | RO  | 0x0000  |
| 0x012D  | 15:0 | MIB2_CNTA[31:16] | MSB of Port 2 MIB counter group A. | RO  | 0x0000  |
| <b>Port 2 MIB Counter B 0-1 (P2MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x012E  | 15:0 | MIB2_CNTB[15:0]  | LSB of Port 2 MIB counter group B. | RO  | 0x0000  |
| 0x012F  | 15:0 | MIB2_CNTB[31:16] | MSB of Port 2 MIB counter group B. | RO  | 0x0000  |
| <b>Port 2 MIB Counter C 0-1 (P2MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x0130  | 15:0 | MIB2_CNTC[15:0]  | LSB of Port 2 MIB counter group C. | RO  | 0x0000  |
| 0x0131  | 15:0 | MIB2_CNTC[31:16] | MSB of Port 2 MIB counter group C. | RO  | 0x0000  |
| <b>Port 3 MIB Counter A 0-1 (P3MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x0132  | 15:0 | MIB3_CNTA[15:0]  | LSB of Port 3 MIB counter group A. | RO  | 0x0000  |
| 0x0133  | 15:0 | MIB3_CNTA[31:16] | MSB of Port 3 MIB counter group A. | RO  | 0x0000  |
| <b>Port 3 MIB Counter B 0-1 (P3MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x0134  | 15:0 | MIB3_CNTB[15:0]  | LSB of Port 3 MIB counter group B. | RO  | 0x0000  |
| 0x0135  | 15:0 | MIB3_CNTB[31:16] | MSB of Port 3 MIB counter group B. | RO  | 0x0000  |
| <b>Port 3 MIB Counter C 0-1 (P3MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x0136  | 15:0 | MIB3_CNTC[15:0]  | LSB of Port 3 MIB counter group C. | RO  | 0x0000  |
| 0x0137  | 15:0 | MIB3_CNTC[31:16] | MSB of Port 3 MIB counter group C. | RO  | 0x0000  |
| <b>Port 4 MIB Counter A 0-1 (P4MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x0138  | 15:0 | MIB4_CNTA[15:0]  | LSB of Port 4 MIB counter group A. | RO  | 0x0000  |
| 0x0139  | 15:0 | MIB4_CNTA[31:16] | MSB of Port 4 MIB counter group A. | RO  | 0x0000  |
| <b>Port 4 MIB Counter B 0-1 (P4MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x013A  | 15:0 | MIB4_CNTB[15:0]  | LSB of Port 4 MIB counter group B. | RO  | 0x0000  |
| 0x013B  | 15:0 | MIB4_CNTB[31:16] | MSB of Port 4 MIB counter group B. | RO  | 0x0000  |
| <b>Port 4 MIB Counter C 0-1 (P4MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x013C  | 15:0 | MIB4_CNTC[15:0]  | LSB of Port 4 MIB counter group C. | RO  | 0x0000  |
| 0x013D  | 15:0 | MIB4_CNTC[31:16] | MSB of Port 4 MIB counter group C. | RO  | 0x0000  |
| <b>Port 5 MIB Counter A 0-1 (P5MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x013E  | 15:0 | MIB5_CNTA[15:0]  | LSB of Port 5 MIB counter group A. | RO  | 0x0000  |
| 0x013F  | 15:0 | MIB5_CNTA[31:16] | MSB of Port 5 MIB counter group A. | RO  | 0x0000  |

| Reg.  | Bits | Name             | Description                        | R/W | Default |
|---|------|------------------|------------------------------------|-----|---------|
| <b>Port 5 MIB Counter B 0-1 (P5MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x0140  | 15:0 | MIB5_CNTB[15:0]  | LSB of Port 5 MIB counter group B. | RO  | 0x0000  |
| 0x0141  | 15:0 | MIB5_CNTB[31:16] | MSB of Port 5 MIB counter group B. | RO  | 0x0000  |
| <b>Port 5 MIB Counter C 0-1 (P5MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x0142  | 15:0 | MIB5_CNTC[15:0]  | LSB of Port 5 MIB counter group C. | RO  | 0x0000  |
| 0x0143  | 15:0 | MIB5_CNTC[31:16] | MSB of Port 5 MIB counter group C. | RO  | 0x0000  |
| <b>Port 6 MIB Counter A 0-1 (P6MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x0144  | 15:0 | MIB6_CNTA[15:0]  | LSB of Port 6 MIB counter group A. | RO  | 0x0000  |
| 0x0145  | 15:0 | MIB6_CNTA[31:16] | MSB of Port 6 MIB counter group A. | RO  | 0x0000  |
| <b>Port 6 MIB Counter B 0-1 (P6MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x0146  | 15:0 | MIB6_CNTB[15:0]  | LSB of Port 6 MIB counter group B. | RO  | 0x0000  |
| 0x0147  | 15:0 | MIB6_CNTB[31:16] | MSB of Port 6 MIB counter group B. | RO  | 0x0000  |
| <b>Port 6 MIB Counter C 0-1 (P6MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x0148  | 15:0 | MIB6_CNTC[15:0]  | LSB of Port 6 MIB counter group C. | RO  | 0x0000  |
| 0x0149  | 15:0 | MIB6_CNTC[31:16] | MSB of Port 6 MIB counter group C. | RO  | 0x0000  |
| <b>Port 7 MIB Counter A 0-1 (P7MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x014A  | 15:0 | MIB7_CNTA[15:0]  | LSB of Port 7 MIB counter group A. | RO  | 0x0000  |
| 0x014B  | 15:0 | MIB7_CNTA[31:16] | MSB of Port 7 MIB counter group A. | RO  | 0x0000  |
| <b>Port 7 MIB Counter B 0-1 (P7MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x014C  | 15:0 | MIB7_CNTB[15:0]  | LSB of Port 7 MIB counter group B. | RO  | 0x0000  |
| 0x014D  | 15:0 | MIB7_CNTB[31:16] | MSB of Port 7 MIB counter group B. | RO  | 0x0000  |
| <b>Port 7 MIB Counter C 0-1 (P7MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x014E  | 15:0 | MIB7_CNTC[15:0]  | LSB of Port 7 MIB counter group C. | RO  | 0x0000  |
| 0x014F  | 15:0 | MIB7_CNTC[31:16] | MSB of Port 7 MIB counter group C. | RO  | 0x0000  |
| <b>Port 8 MIB Counter A 0-1 (P8MIB_CNTA0-1)</b> |      |                  |                                    |     |         |
| 0x0150  | 15:0 | MIB8_CNTA[15:0]  | LSB of Port 8 MIB counter group A. | RO  | 0x0000  |
| 0x0151  | 15:0 | MIB8_CNTA[31:16] | MSB of Port 8 MIB counter group A. | RO  | 0x0000  |
| <b>Port 8 MIB Counter B 0-1 (P8MIB_CNTB0-1)</b> |      |                  |                                    |     |         |
| 0x0152  | 15:0 | MIB8_CNTB[15:0]  | LSB of Port 8 MIB counter group B. | RO  | 0x0000  |
| 0x0153  | 15:0 | MIB8_CNTB[31:16] | MSB of Port 8 MIB counter group B. | RO  | 0x0000  |
| <b>Port 8 MIB Counter C 0-1 (P8MIB_CNTC0-1)</b> |      |                  |                                    |     |         |
| 0x0154  | 15:0 | MIB8_CNTC[15:0]  | LSB of Port 8 MIB counter group C. | RO  | 0x0000  |
| 0x0155  | 15:0 | MIB8_CNTC[31:16] | MSB of Port 8 MIB counter group C. | RO  | 0x0000  |

#### 10.4.6. 0x0159 ~ 0x015D: Port Status Register 0-4 (PSR0-4)

Table 57. 0x0159 ~ 0x015D: Port Status Register 0-4 (PSR0-4)

| Reg.   | Bits | Name       | Description  | R/W | Default |
|--------|------|------------|--|-----|---------|
| 0x0159 | 1:0  | POSPD[1:0] | Indicates the current speed of the port.<br>0b00: 10M<br>0b01: 100M<br>0b10: 1000M<br>0b11: Reserved | RO  | 0b00    |



| Reg.   | Bits | Name                            | Description  | R/W | Default |
|--------|------|---------------------------------|--|-----|---------|
|        | 2    | P0DUP                           | Indicates the current duplex status of the port.<br>0b0: Half duplex<br>0b1: Full duplex | RO  | 0b0     |
|        | 3    | Reserved                        |  |     | 0b0     |
|        | 4    | P0LINK                          | Indicates the current link status.<br>0b0: Link down<br>0b1: Link up                     | RO  | 0b0     |
|        | 5    | P0TXPAUSE                       | Indicates the pause frame transmit ability of the port.<br>0b0: Inactive<br>0b1: Active  | RO  | 0b1     |
|        | 6    | P0RXPAUSE                       | Indicates the pause frame response ability of the port.<br>0b0: Inactive<br>0b1: Active  | RO  | 0b1     |
|        | 7    | P0NWAY                          | Indicates auto-negotiation enabled or disabled.<br>0b0: Disable<br>0b1: Enable           | RO  | 0b1     |
|        | 9:8  | P1SPD[1:0]                      | Same as P0SPD[1:0]   | RO  | 0b00    |
|        | 10   | P1DUP                           | Same as P0DUP  | RO  | 0b0     |
|        | 11   | Reserved                        |  |     | 0b0     |
|        | 12   | P1LINK                          | Same as P0LINK   | RO  | 0b1     |
|        | 13   | P1TXPAUSE                       | Same as P0TXPAUSE  | RO  | 0b1     |
|        | 14   | P1RXPAUSE                       | Same as P0RXPAUSE  | RO  | 0b1     |
|        | 15   | P1NWAY                          | Same as P0NWAY   | RO  | 0b0     |
| 0x015A | 7:0  | Port 2 Property Status Register | Same as Port 0 Property Status Register  | RO  | 0xE0    |
|        | 15:8 | Port 3 Property Status Register | Same as Port 0 Property Status Register  | RO  | 0xE0    |
| 0x015B | 7:0  | Port 4 Property Status Register | Same as Port 0 Property Status Register  | RO  | 0xE0    |
|        | 15:8 | Port 5 Property Status Register | Same as Port 0 Property Status Register  | RO  | 0xE0    |
| 0x015C | 7:0  | Port 6 Property Status Register | Same as Port 0 Property Status Register  | RO  | 0xE0    |
|        | 15:8 | Port 7 Property Status Register | Same as Port 0 Property Status Register  | RO  | 0xE0    |
| 0x015D | 7:0  | Port 8 Property Status Register | Same as Port 0 Property Status Register  | RO  | 0xEE    |
|        | 15:8 | Reserved                        |  |     | 0x00    |

### 10.4.7. 0x0170: EEPROM Status Register (EEPSR)

**Table 58. 0x0170: EEPROM Status Register (EEPSR)**

| Reg.   | Bits | Name             | Description  | R/W | Default |
|--------|------|------------------|--|-----|---------|
| 0x0170 | 0    | EEPROM_EXISTENCE | Indicates the existence of EEPROM.<br>0b0: EEPROM does not exist<br>0b1: EEPROM exists | RO  | 0b0     |
|        | 1    | Internal Use     | N/A  | RO  | 0b0     |
|        | 2    | EEPROM_RDY       | Indicates the EEPROM SMI access is ready.  | RO  | 0b1     |
|        | 15:3 | Reserved         |  |     | 0x0000  |

### 10.4.8. 0x0180 ~ 0x018A: Lookup and VLAN Table Engine Access Control

**Table 59. 0x0180 ~ 0x018A: Lookup and VLAN Table Engine Access Control**

| Reg.  | Bits  | Name           | Description  | R/W    | Default |
|---|-------|----------------|--|--------|---------|
| <b>Lookup &amp; VLAN Table Access Control Register (LVTACR)</b>     |       |                |  |        |         |
| 0x0180  | 0     | TABLE_EXEC     | 0b0: No operation<br>0b1: Start to access. Self-cleared when the access is done                          | R/W    | 0b0     |
|   | 7:1   | Reserved       |  |        | 0x00    |
|   | 9:8   | TABLE_CMD[1:0] | 0b00: Look-up Table Read<br>0b01: Look-up Table Write<br>0b10: VLAN Table Read<br>0b11: VLAN Table Write | R/W    | 0b00    |
|   | 15:10 | Reserved       |  |        | 0x00    |
| 0x0181  | 15:0  | Reserved       |  |        | 0x0000  |
| <b>Lookup &amp; VLAN Table Data Input Register 0-3 (LVTDIR0-3)</b>  |       |                |  |        |         |
| 0x0182  | 15:0  | WD[15:0]       | Write Data Buffer [69:0]   | R/W    | 0x0000  |
| 0x0183  | 15:0  | WD[31:16]      |  | R/W    | 0x0000  |
| 0x0184  | 15:0  | WD[47:32]      |  | R/W    | 0x0000  |
| 0x0185  | 15:0  | WD[63:48]      |  | R/W    | 0x0000  |
| 0x0186  | 5:0   | WD[69:64]      |  | R/W    | 0x00    |
|   | 15:6  | Reserved       |  | 0x0000 |         |
| 0x0187  | 15:0  | Reserved       |  | 0x0000 |         |
| <b>Lookup &amp; VLAN Table Data Output Register 0-2 (LVTDOR0-2)</b> |       |                |  |        |         |
| 0x0188  | 15:0  | RD[15:0]       |  | R/W    | 0x0000  |
| 0x0189  | 15:0  | RD[31:16]      |  | R/W    | 0x0000  |
| 0x018A  | 15:0  | RD[47:32]      |  | R/W    | 0x0000  |

## 11. Electrical Characteristics

### 11.1. Absolute Maximum Ratings

**WARNING:** Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 60. Absolute Maximum Ratings**

| Parameter                    | Min  | Max | Units |
|------------------------------|------|-----|-------|
| Storage Temperature          | -55  | 150 | °C    |
| Vcc Supply Referenced to GND | -0.5 | 4.0 | V     |
| Digital Input Voltage        | -0.5 | VDD | V     |
| DC Output Voltage            | -0.5 | VDD | V     |

### 11.2. Operating Range

**Table 61. Operating Range**

| Parameter                          | Min  | Typical | Max  | Units |
|------------------------------------|------|---------|------|-------|
| Ambient Operating Temperature (Ta) | 0    | N/A     | 70   | °C    |
| 3.3V Vcc Supply Voltage Range      | 3.15 | 3.3     | 3.45 | V     |
| 1.8V Vcc Supply Voltage Range      | 1.71 | 1.8     | 1.89 | V     |
| 1.5V Vcc Supply Voltage Range      | 1.43 | 1.5     | 1.57 | V     |

### 11.3. Thermal Characteristics

TBD

### 11.4. DC Characteristics

**Table 62. DC Characteristics**

| Parameter                             | SYM               | Condition | Min | Typical | Max | Units |
|---------------------------------------|-------------------|-----------|-----|---------|-----|-------|
| <b>System Idle</b>                    |                   |           |     |         |     |       |
| Power Supply Current for 3.3V         | I <sub>CC33</sub> |           |     | 20      |     | mA    |
| Power Supply Current for 1.8V         | I <sub>CC18</sub> |           |     | 240     |     | mA    |
| Power Supply Current for 1.5V         | I <sub>CC15</sub> |           |     | 170     |     | mA    |
| Total Power Consumption for all Ports | PS                |           |     | 753     |     | mW    |
| <b>1000M Active</b>                   |                   |           |     |         |     |       |
| Power Supply Current for 3.3V         | I <sub>CC33</sub> |           |     | 50      |     | mA    |

| Parameter                             | SYM               | Condition | Min | Typical | Max | Units |
|---------------------------------------|-------------------|-----------|-----|---------|-----|-------|
| Power Supply Current for 1.8V         | I <sub>CC18</sub> |           |     | 240     |     | mA    |
| Power Supply Current for 1.5V         | I <sub>CC15</sub> |           |     | 280     |     | mA    |
| Total Power Consumption for all Ports | PS                |           |     | 1017    |     | mW    |
| <b>100M Active</b>                    |                   |           |     |         |     |       |
| Power Supply Current for 3.3V         | I <sub>CC33</sub> |           |     | 50      |     | mA    |
| Power Supply Current for 1.8V         | I <sub>CC18</sub> |           |     | 240     |     | mA    |
| Power Supply Current for 1.5V         | I <sub>CC15</sub> |           |     | 170     |     | mA    |
| Total Power Consumption for all Ports | PS                |           |     | 852     |     | mW    |
| <b>10M Active</b>                     |                   |           |     |         |     |       |
| Power Supply Current for 3.3V         | I <sub>CC33</sub> |           |     | 50      |     | mA    |
| Power Supply Current for 1.8V         | I <sub>CC18</sub> |           |     | 240     |     | mA    |
| Power Supply Current for 1.5V         | I <sub>CC15</sub> |           |     | 170     |     | mA    |
| Total Power Consumption for all Ports | PS                |           |     | 852     |     | mW    |
| <b>VDDIO = 3.3V</b>                   |                   |           |     |         |     |       |
| TTL Input High Voltage                | V <sub>ih</sub>   |           | 2.0 |         |     | V     |
| TTL Input Low Voltage                 | V <sub>il</sub>   |           |     |         | 0.8 | V     |
| Output High Voltage                   | V <sub>oh</sub>   |           | 2.4 |         |     | V     |
| Output Low Voltage                    | V <sub>ol</sub>   |           |     |         | 0.4 | V     |
| <b>VDDIO = 2.5V</b>                   |                   |           |     |         |     |       |
| TTL Input High Voltage                | V <sub>ih</sub>   |           |     | TBD     |     | V     |
| TTL Input Low Voltage                 | V <sub>il</sub>   |           |     | TBD     |     | V     |
| Output High Voltage                   | V <sub>oh</sub>   |           |     | TBD     |     | V     |
| Output Low Voltage                    | V <sub>ol</sub>   |           |     | TBD     |     | V     |

## 11.5. AC Characteristics

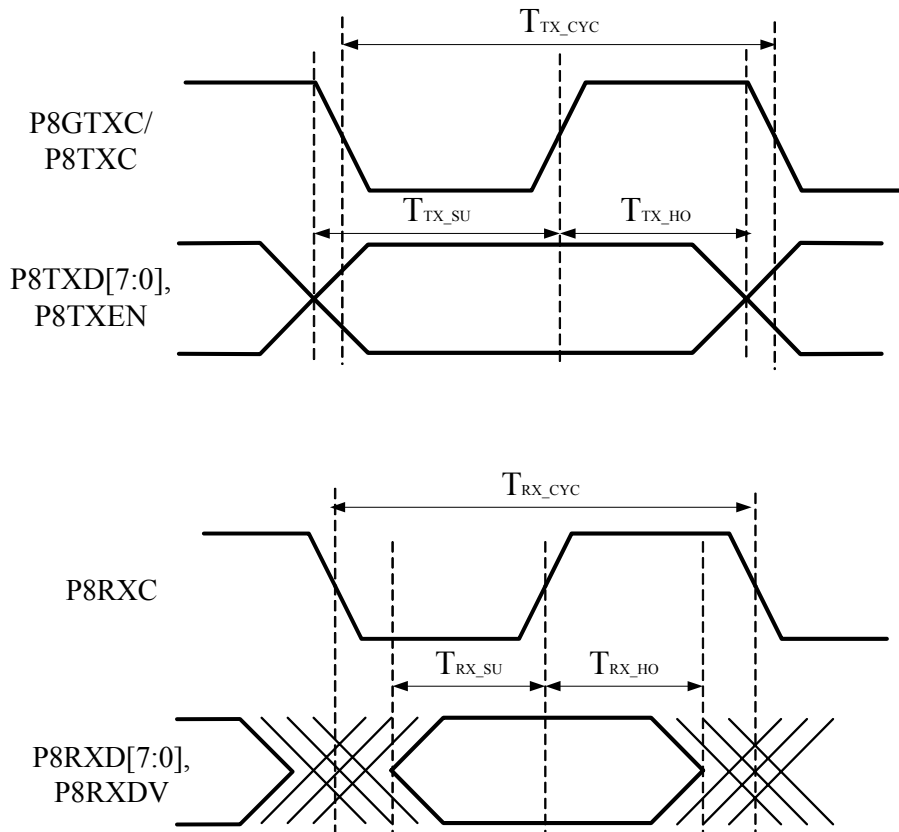
### 11.5.1. EEPROM SMI (SCK/SDA) Timing Characteristics

TBD

### 11.5.2. SMI (MDC/MDIO) Timing Characteristics

TBD

### 11.5.3. GMII/MII Timing Characteristics



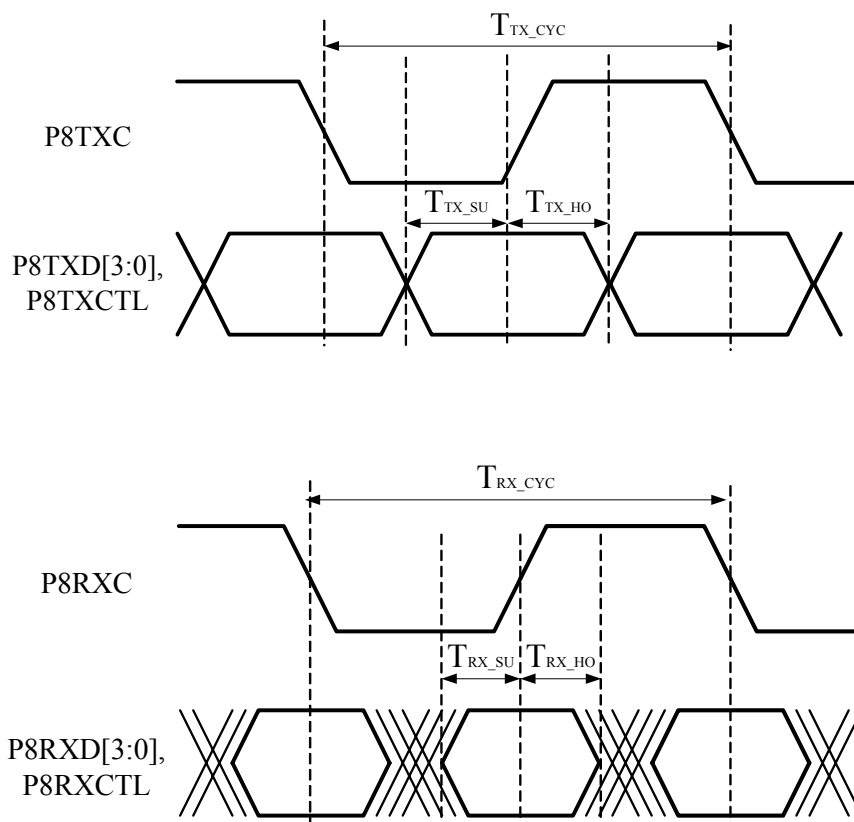
**Figure 25. GMII/MII Timing Characteristics**

**Table 63. GMII/MII Timing Characteristics**

| Parameter  | SYM               | Description/Condition              | I/O | Min | Typical | Max | Units |
|--|-------------------|------------------------------------|-----|-----|---------|-----|-------|
| 1000Base-T P8GTXC Output Cycle Time                | $T_{TX\_CYC}$     | P8GTXC 125MHz clock output.        | O   |     | TBD     |     | ns    |
| 1000Base-T P8RXC Input Cycle Time                  | $T_{RX\_CYC}$     | P8RXC 125MHz clock input.          | I   |     | TBD     |     | ns    |
| 1000Base-T P8TXD[7:0] and P8TXEN Output Setup Time | $T_{TX\_SU}$      |                                    | O   |     | TBD     |     | ns    |
| 1000Base-T P8TXD[7:0] and GTXCLT Output Hold Time  | $T_{TX\_HO}$      |                                    | O   |     | TBD     |     | ns    |
| 1000Base-T P8RXD[7:0] and P8RXCLT Input Setup Time | $T_{RX\_SU}$      |                                    | I   |     | TBD     |     | ns    |
| 1000Base-T P8RXD[7:0] and P8RXCLT Input Hold Time  | $T_{RX\_HO}$      |                                    | I   |     | TBD     |     | ns    |
| 100Base-T P8TXC and P8RXC Input Cycle Time         | $T_{TX\&RX\_CYC}$ | P8TXC and P8RXC 25MHz clock input. | I   |     | TBD     |     | ns    |

| Parameter   | SYM               | Description/Condition               | I/O | Min | Typical | Max | Units |
|---|-------------------|-------------------------------------|-----|-----|---------|-----|-------|
| 100Base-T P8TXD[3:0] and P8TXEN Output Setup Time | $T_{TX\_SU}$      |                                     | O   |     | TBD     |     | ns    |
| 100Base-T P8TXD[3:0] and GTXCLT Output Hold Time  | $T_{TX\_HO}$      |                                     | O   |     | TBD     |     | ns    |
| 100Base-T P8RXD[3:0] and P8RXCLT Input Setup Time | $T_{RX\_SU}$      |                                     | I   |     | TBD     |     | ns    |
| 100Base-T P8RXD[3:0] and P8RXCLT Input Hold Time  | $T_{RX\_HO}$      |                                     | I   |     | TBD     |     | ns    |
| 10Base-T P8TXC and P8RXC Input Cycle Time         | $T_{TX\&RX\_CYC}$ | P8TXC and P8RXC 2.5MHz clock input. | I   |     | TBD     |     | ns    |
| 10Base-T P8TXD[3:0] and P8TXEN Output Setup Time  | $T_{TX\_SU}$      |                                     | O   |     | TBD     |     | ns    |
| 10Base-T P8TXD[3:0] and GTXCLT Output Hold Time   | $T_{TX\_HO}$      |                                     | O   |     | TBD     |     | ns    |
| 10Base-T P8RXD[3:0] and P8RXCLT Input Setup Time  | $T_{RX\_SU}$      |                                     | I   |     | TBD     |     | ns    |
| 10Base-T P8RXD[3:0] and P8RXCLT Input Hold Time   | $T_{RX\_HO}$      |                                     | I   |     | TBD     |     | ns    |

### 11.5.4. RGMII Timing Characteristics

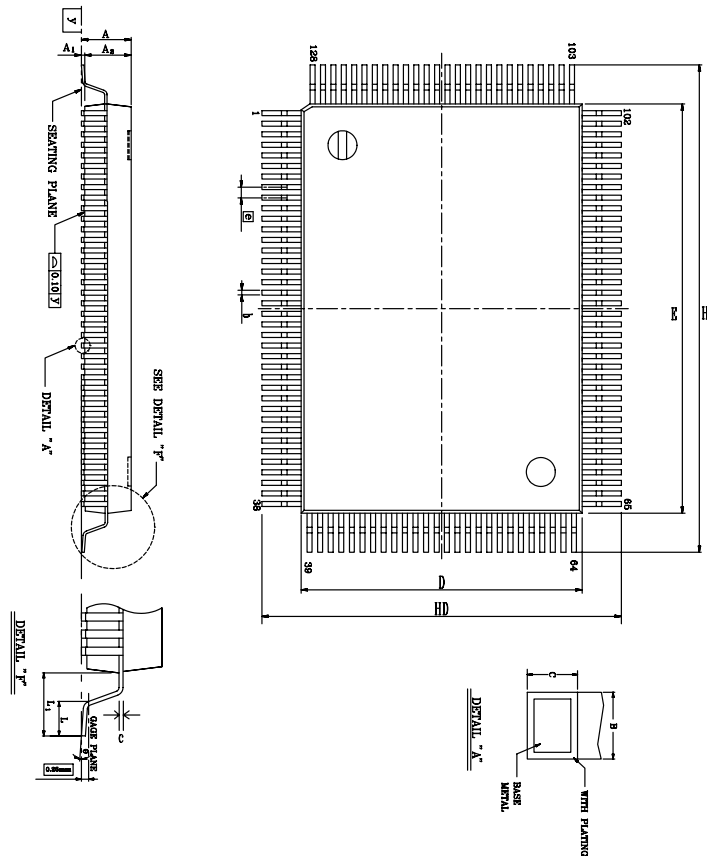


**Figure 26. RGMII Timing Characteristics**

**Table 64. RGMII Timing Characteristics**

| Parameter  | SYM                  | Description/Condition                  | I/O | Min | Typical | Max | Units |
|--|----------------------|--|-----|-----|---------|-----|-------|
| 1000Base-T P8TXC Output Cycle Time                                   | T <sub>TX_CYC</sub>  | P8TXC 125MHz clock output.             | O   |     | TBD     |     | ns    |
| 1000Base-T P8RXC Input Cycle Time                                    | T <sub>RX_CYC</sub>  | P8RXC 125MHz clock input.              | I   |     | TBD     |     | ns    |
| 1000Base-T P8TXD[3:0] and P8TXCLT Output Setup Time                  | T <sub>TX_SU</sub>   | Disable P8TXC delay (P8TXC_DELAY=0b0). | O   |     | TBD     |     | ns    |
| 1000Base-T P8TXD[3:0] and P8TXCLT Output Hold Time                   | T <sub>TX_HO</sub>   | Disable P8TXC delay (P8TXC_DELAY=0b0). | O   |     | TBD     |     | ns    |
| 1000Base-T P8TXD[3:0] and P8TXCLT Output Setup Time with P8TXC Delay | T <sub>TX_SU_D</sub> | Enable P8TXC delay (P8TXC_DELAY=0b1).  | O   |     | TBD     |     | ns    |
| 1000Base-T P8TXD[3:0], P8TXCLT Output Hold Time with P8TXC Delay     | T <sub>TX_HO_D</sub> | Enable P8TXC delay (P8TXC_DELAY=0b1).  | O   |     | TBD     |     | ns    |
| 1000Base-T P8RXD[3:0] and P8RXCLT Input Setup Time                   | T <sub>RX_SU</sub>   | Disable P8RXC delay (P8RXC_DELAY=0b0). | I   |     | TBD     |     | ns    |
| 1000Base-T P8RXD[3:0] and RXCLT Input Hold Time                      | T <sub>RX_HO</sub>   | Disable P8RXC delay (P8RXC_DELAY=0b0). | I   |     | TBD     |     | ns    |
| 1000Base-T P8RXD[3:0] and P8RXCLT Input Setup Time with P8RXC Delay  | T <sub>RX_SU_D</sub> | Enable P8RXC delay (P8RXC_DELAY=0b1).  | I   |     | TBD     |     | ns    |
| 1000Base-T P8RXD[3:0] and P8RXCLT Input Hold Time with P8RXC Delay   | T <sub>RX_HO_D</sub> | Enable P8RXC delay (P8RXC_DELAY=0b1).  | I   |     | TBD     |     | ns    |

## 12. Mechanical Dimensions



| Symbol | Dimensions in inches |         |       | Dimensions in mm |         |       |
|--------|----------------------|---------|-------|------------------|---------|-------|
|        | Min                  | Typical | Max   | Min              | Typical | Max   |
| A      | -                    | -       | 0.134 | -                | -       | 3.40  |
| A1     | 0.004                | 0.010   | 0.036 | 0.10             | 0.25    | 0.91  |
| A2     | 0.102                | 0.112   | 0.122 | 2.60             | 2.85    | 3.10  |
| b      | 0.005                | 0.009   | 0.013 | 0.12             | 0.22    | 0.32  |
| c      | 0.002                | 0.006   | 0.010 | 0.05             | 0.15    | 0.25  |
| D      | 0.541                | 0.551   | 0.561 | 13.75            | 14.00   | 14.25 |
| E      | 0.778                | 0.787   | 0.797 | 19.75            | 20.00   | 20.25 |
| e      | 0.010                | 0.020   | 0.030 | 0.25             | 0.5     | 0.75  |
| HD     | 0.665                | 0.677   | 0.689 | 16.90            | 17.20   | 17.50 |
| HE     | 0.902                | 0.913   | 0.925 | 22.90            | 23.20   | 23.50 |
| L      | 0.027                | 0.035   | 0.043 | 0.68             | 0.88    | 1.08  |
| L1     | 0.053                | 0.063   | 0.073 | 1.35             | 1.60    | 1.85  |
| y      | -                    | -       | 0.004 | -                | -       | 0.10  |
| θ      | 0°                   | -       | 12°   | 0°               | -       | 12°   |

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

|                                     |  |          |                  |
|-------------------------------------|--|----------|------------------|
| TITLE:<br>-CU L/F, FOOTPRINT 3.2 mm |  |          |                  |
| LEADFRAME MATERIAL:                 |  |          |                  |
| APPROVE                             |  | DOC. NO. |                  |
|                                     |  | VERSION  | 1.1              |
| CHECK                               |  | PAGE     |                  |
|                                     |  | DWG NO.  | Q128 - 1         |
|                                     |  | DATE     | 12 February 2003 |
| <b>REALTEK SEMICONDUCTOR CORP.</b>  |  |          |                  |



## 13. Ordering Information

**Table 65. Ordering Information**

| <b>Part Number</b> | <b>Package</b>                  | <b>Status</b> |
|--------------------|---------------------------------|---------------|
| RTL8366-GR         | 128-Pin PQFP in 'Green' Package |               |
| RTL8369-GR         | 128-Pin PQFP in 'Green' Package |               |

*Note: See page 9 and 10 for package identification information.*

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