

SILICON GATE CMOS

65,536 WORD x 18 BIT CMOS STATIC RAM

Description

The TC551864AJ is a 1,179,648 bits high speed static random access memory organized as 65,536 words by 18 bits using CMOS technology and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC551864AJ has a low power feature with device control using Chip Enable (\overline{CE}), and has an Output Enable input (\overline{OE}) for fast memory access. Also, it allows that lower and upper byte access by Data Byte Control (\overline{LB} , \overline{UB}). The TC551864AJ is suitable for use in various application systems where high speed is required such as cache memory, high speed storage, and so on. All inputs and outputs are directly TTL compatible.

The TC551864AJ is packaged in a 44-pin plastic SOJ with 400mil width for high density surface assembly.

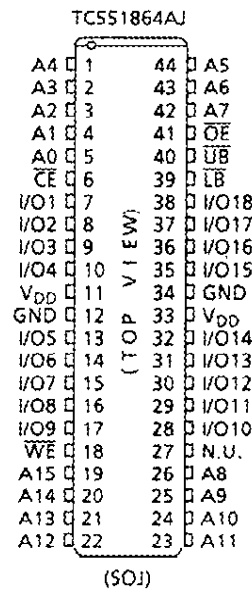
Features

- Fast access time
 - TC551864AJ -15 15ns (max.)
 - TC551864AJ -20 20ns (max.)
- Low power dissipation

Cycle Time	15	20	25	30	50	ns
Operation (max.)	260	220	200	180	150	mA

 - Standby: 1mA (max.)
- 5V single power supply: $5V \pm 10\%$
- Fully static operation
- All inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Data byte controls: \overline{LB} , (I/O1 ~ I/O9), \overline{UB} (I/O10 ~ I/O18)
- Package
 - TC551864AJ: SOJ44-P-400

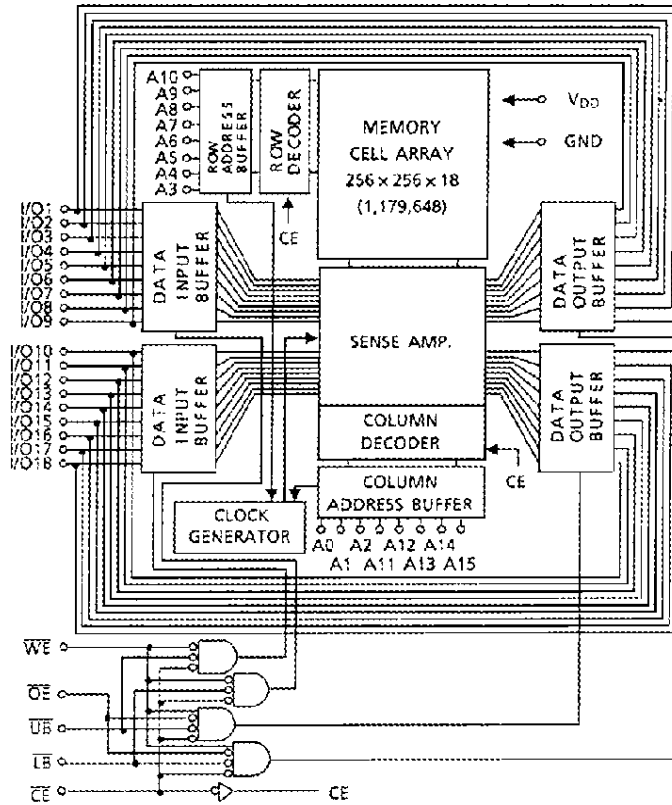
Pin Connection (Top View)



Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O18	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
V _{DD}	Power (+5V)
GND	Ground
N.U.	Not Usable (Input)

Block Diagram



Operating Mode

OPERATING MODE	\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 ~ I/O9	I/O10 ~ I/O18	POWER
Read	L	L	H	L	L	Output	Output	I_{DD0}
				H	L	High Impedance	Output	I_{DD0}
				L	H	Output	High Impedance	I_{DD0}
Write	L	*	L	L	L	Input	Input	I_{DD0}
				H	L	High Impedance	Input	I_{DD0}
				L	H	Input	High Impedance	I_{DD0}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DD0}
	L	*	*	H	H	High Impedance	High Impedance	I_{DD0}
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DD5}

*H or L

Note: N.U. pin must be kept open electrically or pulled down to GND level or less than 0.8V. Applying a voltage more than 0.8V to N.U. pin is prohibited.

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-2.0* ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 0.5	V
V _{IL}	Input Low Voltage	-0.5*	–	0.8	V

*-3V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I _{LI}	Input Leakage Current (Except N.U. Pin)	V _{IN} = 0 ~ V _{DD}	–	–	±10	μA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 ~ V _{DD}	–	–	±10	μA	
I _{I(N.U.)}	Input Current (N.U. Pin)	V _{IN} = 0 ~ 0.8V	-1	–	20	μA	
I _{OH}	Output High Voltage	V _{OH} = 2.4V	-4	–	–	mA	
I _{OL}	Output Low Voltage	V _{OL} = 0.4V	8	–	–	mA	
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA, Other Inputs = V _{IH} /V _{IL}	t _{cycle} = 15ns	–	–	260	mA
			t _{cycle} = 20ns	–	–	220	
			t _{cycle} = 25ns	–	–	200	
			t _{cycle} = 30ns	–	–	180	
			t _{cycle} = 50ns	–	–	150	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} /V _{IL}	–	–	30	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	–	–	1		

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C⁽¹⁾, V_{DD} = 5V±10%)**Read Cycle**

SYMBOL	PARAMETER	TC551864AJ -15		TC551864AJ -20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	15	–	20	–	ns
t _{ACC}	Address Access Time	–	15	–	20	
t _{CO}	\overline{CE} Access Time	–	15	–	12	
t _{OE}	\overline{OE} Access Time	–	8	–	10	
t _{BA}	\overline{UB} , \overline{LB} Access Time	–	8	–	10	
t _{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t _{COE}	Output Enable Time from \overline{CE}	5	–	5	–	
t _{OEE}	Output Enable Time from \overline{OE}	1	–	1	–	
t _{BE}	Output Enable Time from \overline{UB} , \overline{LB}	1	–	1	–	
t _{COD}	Output Disable Time from \overline{CE}	–	8	–	8	
t _{ODO}	Output Disable Time from \overline{OE}	–	8	–	8	
t _{BD}	Output Disable Time from \overline{UB} , \overline{LB}	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC551864AJ -15		TC551864AJ -20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	15	–	20	–	ns
t _{WP}	Write Pulse Width	9	–	10	–	
t _{CW}	Chip Enable to End of Write	12	–	13	–	
t _{BW}	\overline{UB} , \overline{LB} Enable to End of Write	12	–	13	–	
t _{AW}	Address Valid to End of Write	12	–	13	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{DS}	Data Setup Time	8	–	10	–	
t _{DH}	Data Hold Time	0	–	0	–	
t _{OEW}	Output Enable Time from \overline{WE}	1	–	1	–	
t _{ODW}	Output Disable Time from \overline{WE}	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

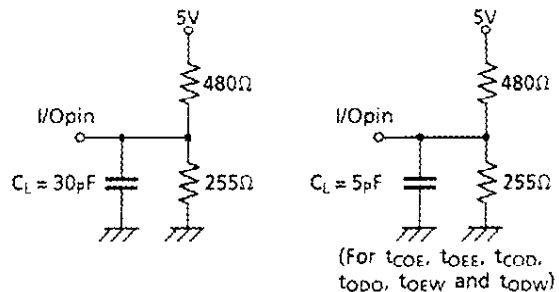
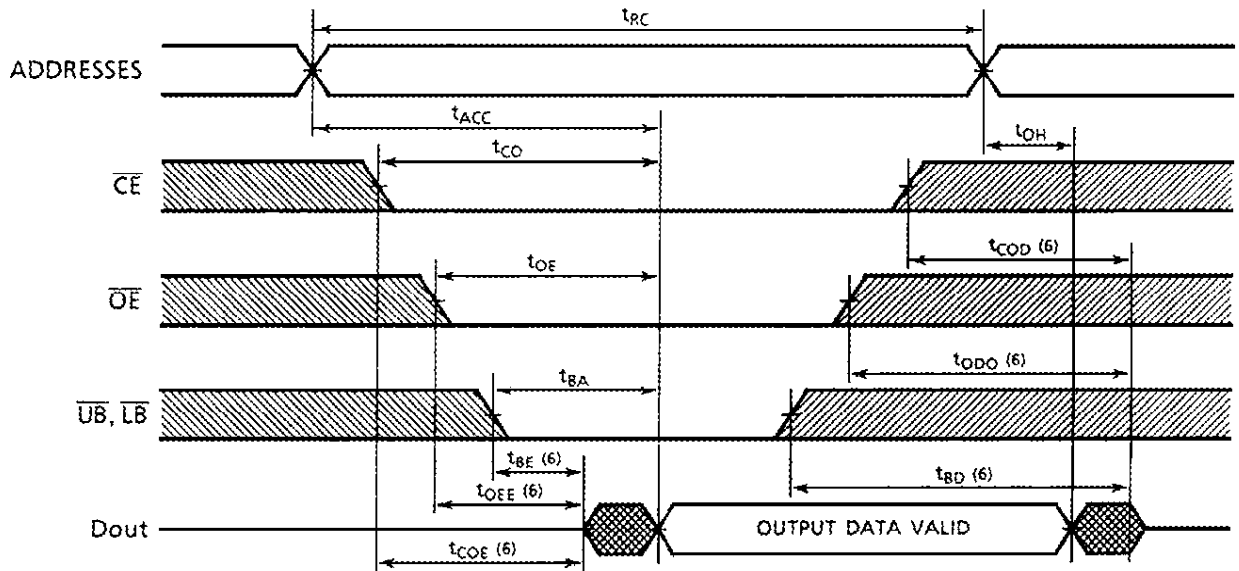


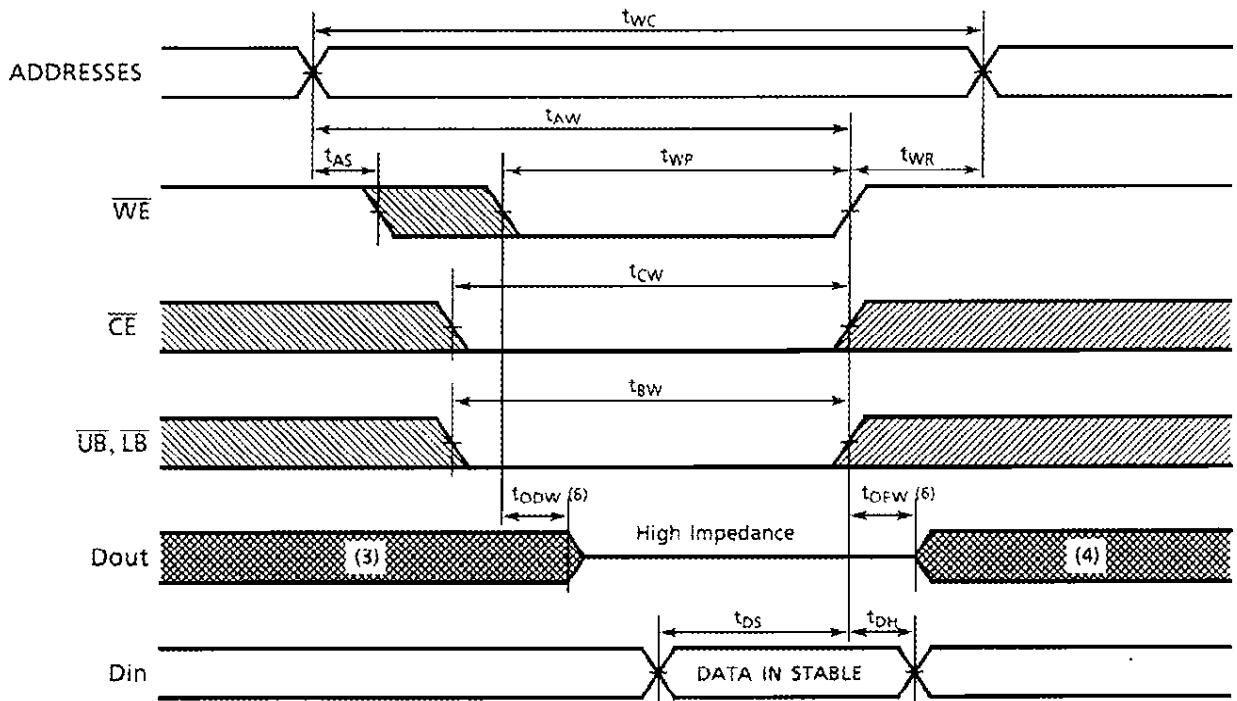
Figure 1.

Timing Waveforms

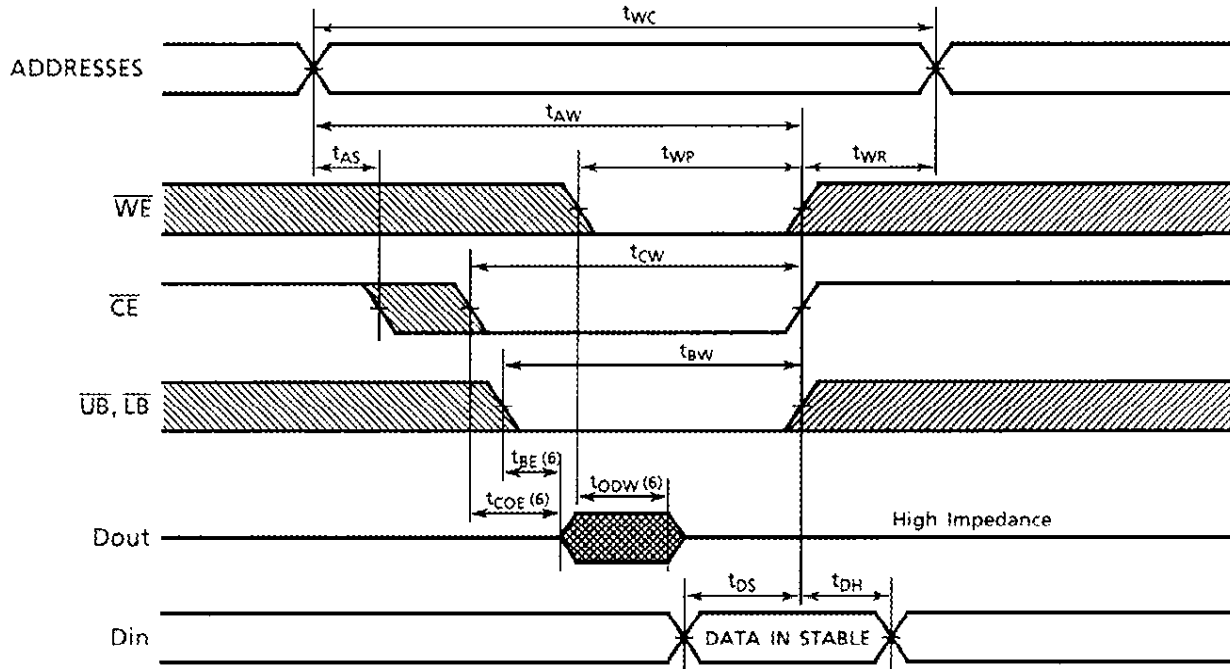
Read Cycle ⁽²⁾



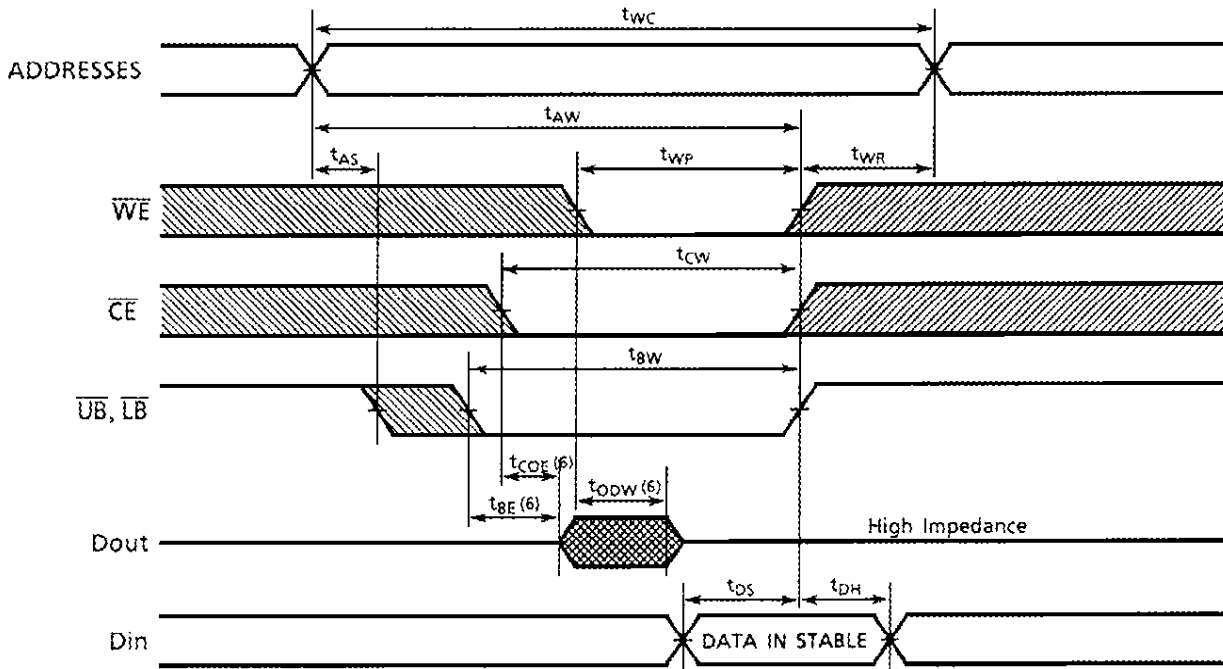
Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled)



Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled)

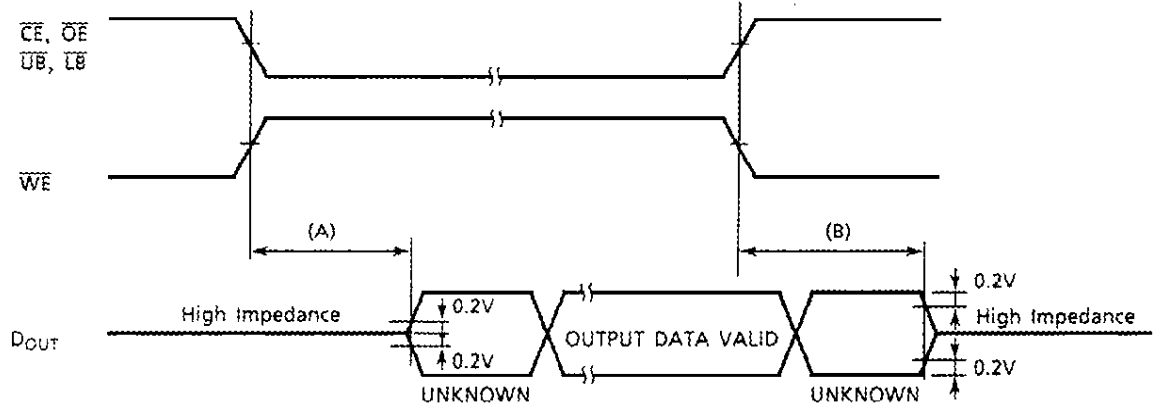


Write Cycle 3 ⁽⁵⁾ (\overline{UB} , \overline{LB} Controlled)



Notes:

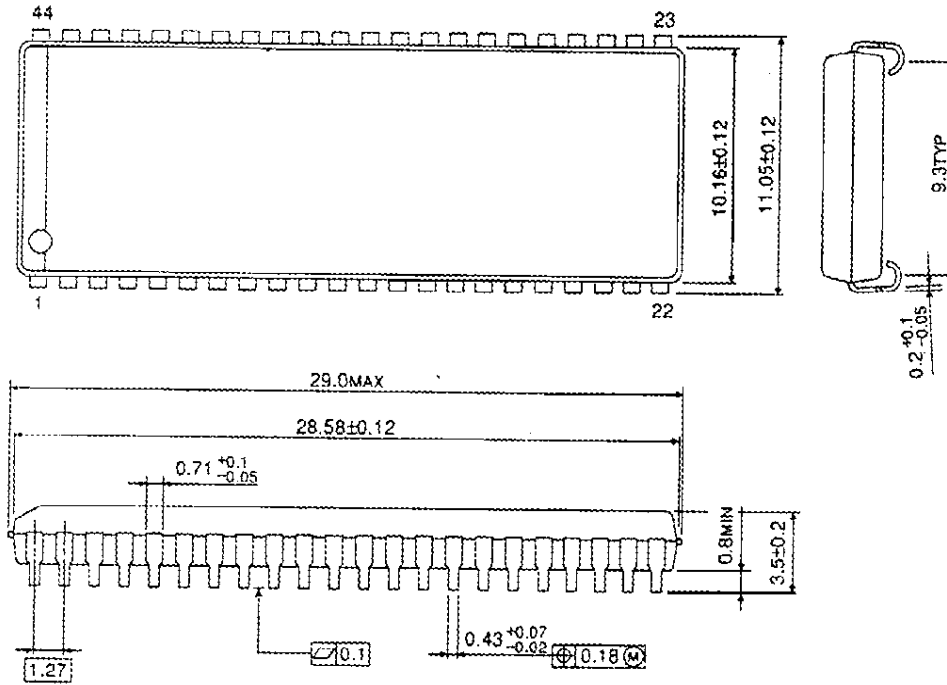
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is High for Read Cycle.
3. Assuming that \overline{CE} Low transition occurs coincident with or after the \overline{WE} Low transition, Outputs remain in a high impedance state.
4. Assuming that \overline{CE} High transition occurs coincident with or prior to the \overline{WE} High transition, Outputs remain in a high impedance state.
5. Assuming that \overline{OE} is High for Write Cycle, the Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Figure 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



Outline Drawings

Unit in mm

Plastic SOJ (SOJ44-P-400)



Weight: 1.64g (typ.)

1. This technical data may be controlled under U.S. Export Administration Regulations and may be subject to the approval of the U.S. Department of Commerce prior to export. Any export or re-export, directly or indirectly, in contravention of the U.S. Export Administration Regulations is strictly prohibited.
2. LIFE SUPPORT POLICY
Toshiba products described in this document are not authorized for use as critical components in life support systems without the written consent of the appropriate officer of Toshiba America, Inc. Life support systems are either systems intended for surgical implant in the body or systems which sustain life.
A critical component in any component of a life support system whose failure to perform may cause a malfunction of the life support system, or may affect its safety or effectiveness.
3. The information in this document has been carefully checked and is believed to be reliable; however no responsibility can be assumed for inaccuracies that may not have been caught. All information in this data book is subject to change without prior notice. Furthermore, Toshiba cannot assume responsibility for the use of any license under the patent rights of Toshiba or any third parties.

Back to Memory